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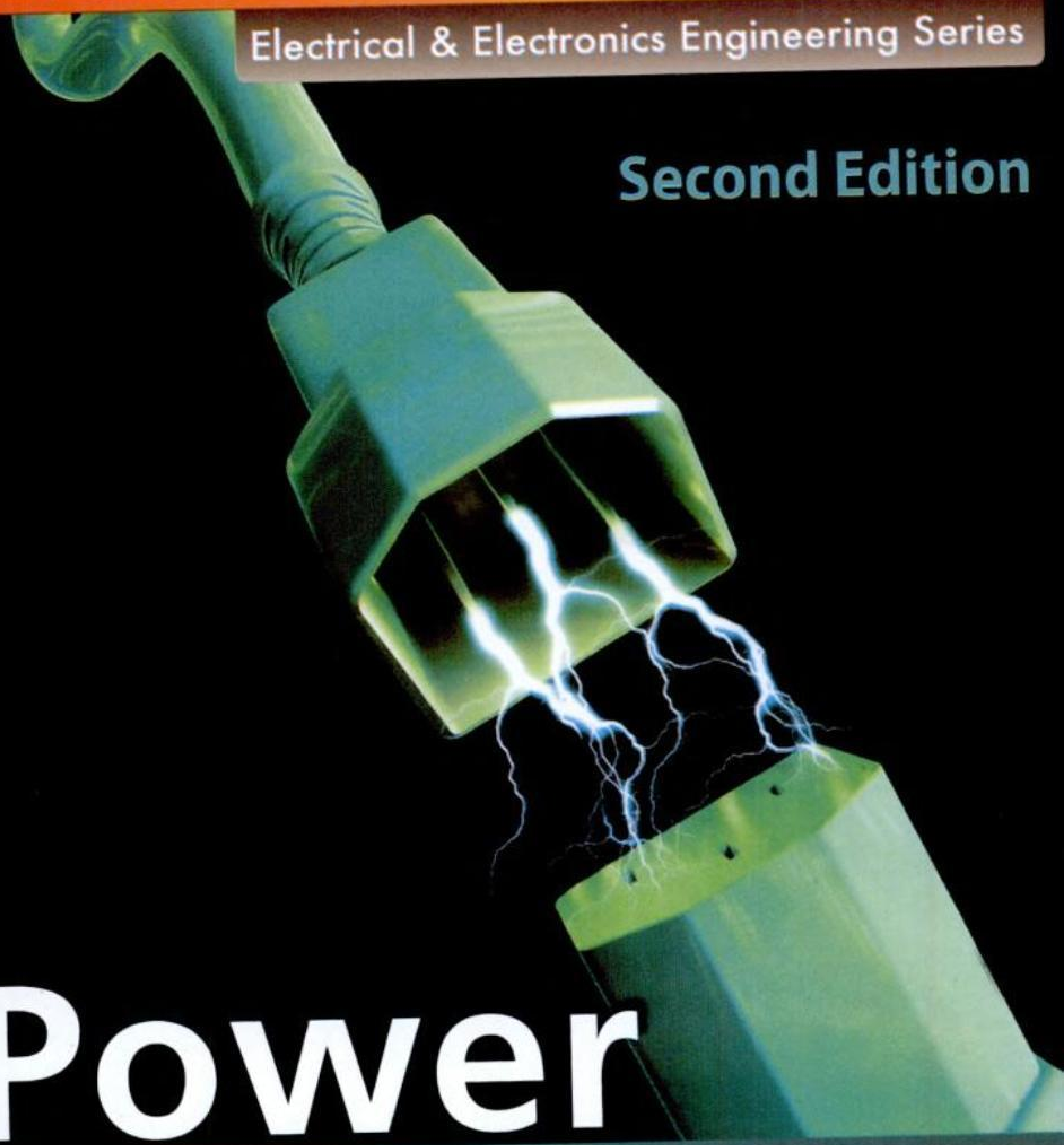
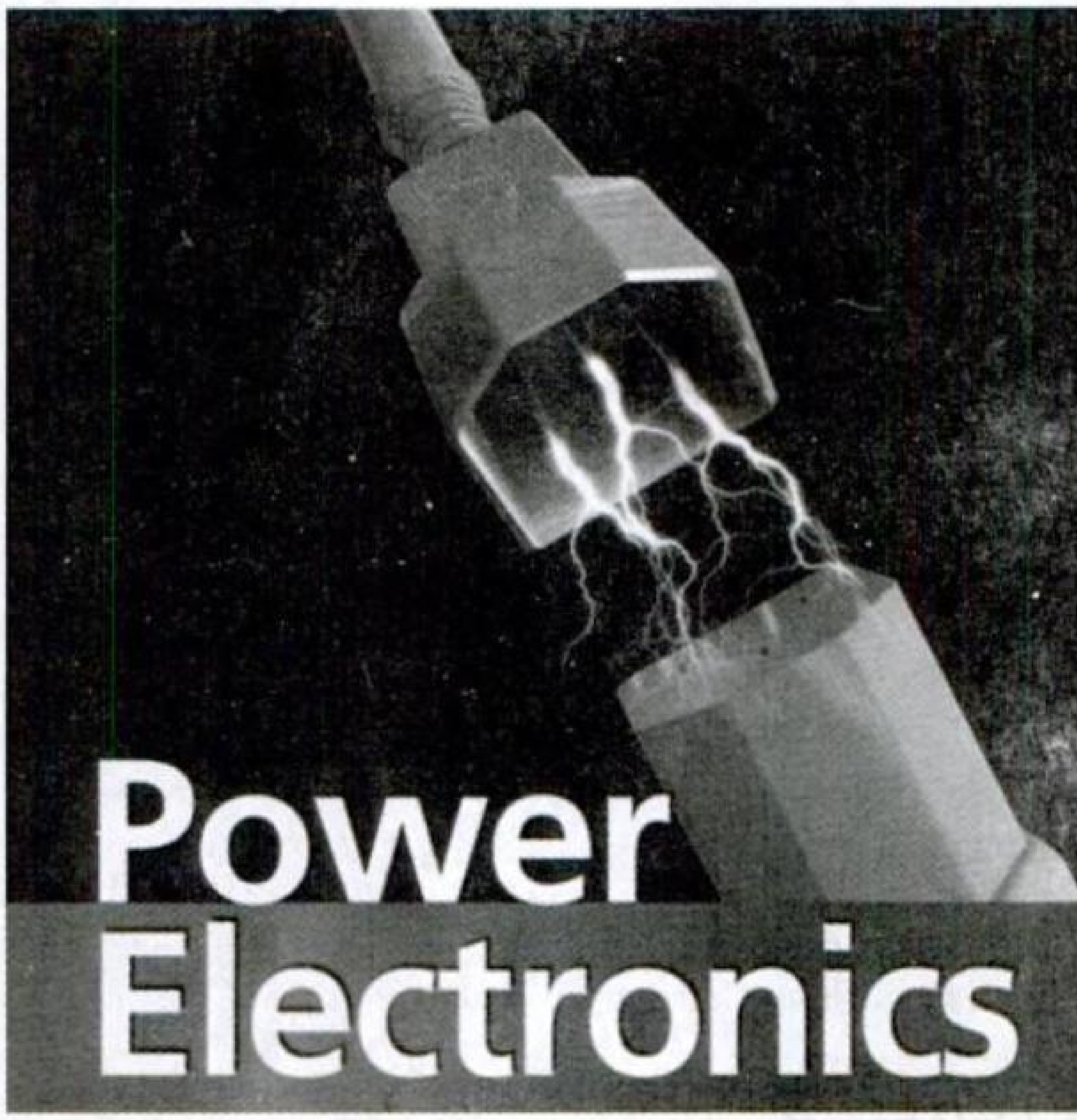
Second Edition



Power Electronics

M D Singh

K B Khanchandani



Second Edition

M D Singh

Former Principal
Laxmi Narayan College of Technology
Bhopal

K B Khanchandani

Professor, Department of Electronics and Telecommunication Engineering,
SSGM College of Engineering
Shegaon, Maharashtra

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Contents

Preface to the Second Edition

The field of electrical engineering is generally segmented into three major areas—electronics, power and control. Power electronics is a combination of these three areas. In broad terms, the function of power electronics is to process and control the electrical energy by supplying voltage and current in a form that is optimally suited to the load. The advent of power semiconductor devices, *thyristors,* in 1957, has been an exciting breakthrough in the art of electric power conversion and its control. Power electronics has undergone intense technological evolution during the last three decades. Starting with the conventional thyristor-type devices in early days, the recent availability of high-frequency, high-power, MOS-gated self-controlled devices are opening new frontiers in the field.

In modern power electronics equipment, there are essentially two types of semiconductor elements: the power semiconductors that can be considered as the muscles of the equipment, and the microelectronics control chips that provide power to the brain. Both the elements are digital in nature, except that one manipulates power upto gigawatts and the other handles only miliwatts. The close coordination of this end of the spectrum of electronics offers reduced size, cost advantages and high-level of performance.

The market demands on industry for productivity and quality are increasing. This has resulted in an increasing demand for automation in production processes and hence in the use of variable speed drives.

The use of electric cars, electric trams and electric subway trains can substantially reduce urban pollution problems. Power electronics permits generation of electric power from environmentally clean photovoltaic, fuel cells and wind energy sources. Widespread application of power electronics, with an eye for energy conservation and generation of power from environmentally clean sources, can help in solving problems like acid rains and greenhouse effects.

This textbook presents the basic tools for the analysis and design of power electronic circuits and provides methods and procedures suitable for a variety of power electronic applications. This text is suitable for undergraduate-level courses in power electronics and/or electrical machines and drives. It is also intended for practicing engineers who wish to gain knowledge of the recent developments in this rapidly expanding field.

In response to the comment and suggestions from students and teachers, several changes in the presentation of topics have been made and new topics have been included in this revised edition of the book.

The second edition offers several improvements over the first edition. Many sections have been rewritten to further simplify the presentation. Several chapters have been revised by adding new updated material. New problems have been formulated for many chapters.

The book consists of 16 chapters. Two chapters (Chapters 1 and 12) are newly added and the sequence of chapters has been modified for better flow of the content. The following is a brief description of the topics that are covered in each chapter with an emphasis on the revisions that have been made in the second edition.

Chapter 1 contains an overview of power electronics and its applications to make the reader aware of the meaning of power electronics and its importance.

Chapter 2 deals with the physical principle of thyristors, their structural details and switching characteristics. The section on turn-on switching characteristics has been completely revised.

Chapter 3 gives a brief description of gate triggering circuits. A new section on *microprocessor interfacing to power thyristors* has been added.

Chapter 4 contains series and parallel operations of thyristor.

Chapter 5 covers the various power semiconductor devices such as power MOSFETs, GTOs, IGBTs, SITs, SITHs, IGCTs, MCTs, MTOs and ETOs. Device structures and physical operations are described and typical terminal characteristics are shown. Many sections are completely revised. The section on power transistors along with solved examples has been moved over to the online learning centre (OLC) of the book. New sections and subsections on IGBTs and ETOs have been added.

Chapter 6 presents various phase-controlled rectifier circuits with their mathematical analysis and performance factors. A new section on power-factor improvement has been added. Many sections have been revised for better understanding. Sections on Firing Circuits for Line Commutated Converters and Triggering Circuits for Single-phase Fully Controlled Converters have been removed from the book. However, these are available on the OLC of the book.

Chapter 7 gives a detailed account of dual converters and their characteristics.

Chapter 8 is devoted to the discussion of the principles of choppers in D.C-to -D.C. conversion. A new section on *flyback converters* has been added. The section on chopper firing circuit has been removed and is available on the website.

Chapter 9 gives a comprehensive treatment of dc–ac inverters in which the various voltage-fed and current-fed inverter circuits are discussed and some typical forced-commutating circuits are investigated. A number of design examples are presented. Sections on three-phase bridge inverters with input circuit commutation and three-phase current source inverters are now available on the website.

Chapter 10 introduces the phase-controlled cycloconverters. The section on ring-connected cycloconverter circuits has been relegated to the website.

Chapter 11 presents a.c. regulators.

Chapter 12 deals with *resonant converters* where LC resonant circuits are utilized to improve the performance of converters. This chapter is newly added and covers the basic technology of resonant and soft-switching converters. Various forms of soft-switching techniques such as ZVS and ZCS are addressed.

Chapter 13 introduces the protection, cooling and mounting of power semi-conductor devices.

Chapter 14 discusses various schemes for D.C. motor speed control. The section on closed loop control of D.C. drives has been shifted to the website.

Chapter 15 introduces variable speed A.C. drives and briefly describes their benefits. It examines their classifications from different perspectives. The section on microprocessor controlled A.C. drive has been removed from the book and is available on the website.

Chapter 16 considers power electronics application circuits. Many sections in this chapter have been completely revised. Also, many new sections have been added.

Web Supplements

The Online Learning Centre of the book at (*http://www.mhhe.com/singh/pe2e*) has separate sections for students and instructors. Students' resource consists of PSPICE simulation examples and multiple-choice questions with answers. For instructors, the website offers the solutions manual wherein all the exercise problems in the book have been solved. It also has chapterwise PowerPoint slides which will help the teachers in preparing lectures and presentations.

M D Singh
K B Khanchandani

Preface to the First Edition

The field of electrical engineering is generally segmented into three major areas—electronics, power and control. Power electronics involves a combination of these three areas. In broad terms, the function of power electronics is to process and control the electrical energy by supplying voltage and current in a form that is optimally suited to the load. The advent of the power semiconductor device, *thyristor* in 1957, has been an exciting breakthrough in the art of electric power conversion and its control. Power electronics has undergone intense technological evolution during the last three decades. Starting with the conventional thyristor-type devices in the early days, the recent availability of high frequency, high power, MOS-gated self-controlled devices is opening new frontiers in power electronics.

In a modern power electronic equipment, there are essentially two types of semiconductor elements: the power semiconductors that can be considered as the muscle of the equipment, and the microelectronic control chips that provide the power to the brain. Both elements are digital in nature, except that one manipulates power up to gigawatts and the other handles only milliwatts. The close coordination of these end-of-the-spectrum electronics offers reduced size, cost advantages and high level of performance.

The market demands on industry for productivity and quality are increasing. This results in the increasing demand for automation in production processes and hence for the use of variable speed drives. Today, power electronics is an indispensable tool in any advanced country's industrial economy. Saving energy is an important aspect of power electronics applications.

The use of electric cars, electric trams and electric subway trains can substantially reduce urban pollution problems. Power electronics permits generation of electric power from environmentally clean photovoltaic, fuel cell and wind energy sources. Widespread application of power electronics, with an eye for energy conservation and generation of power from environmentally clean sources, can help in solving problems like acid rain and greenhouse effects.

This textbook is intended as an introduction to the basic theory and practice of modern power electronics, in particular it deals with the applications of power electronic techniques for d.c. and a.c. motor control. The text is suitable for degree-level and postgraduate courses in power electronics and/or electrical machines and drives. It is also intended for practicing engineers who wish to acquaint themselves with the recent developments in this rapidly expanding field.

The book consists of 14 chapters.

Chapter 1 deals with the physical principles of thyristors, their structural details and their switching characteristics. Chapter 2 gives a brief description of thyristor-firing circuits. Series and parallel operations of thyristors are discussed in Chapter 3.

Chapter 4 discusses all types of line-commutated phase-controlled converters with their mathematical analysis as well as performance factors and triggering circuits for these converters.

Chapter 5 is a comprehensive treatment of d.c.-a.c. inverters in which the various voltage-fed and current-fed inverter circuits are discussed, and some typical thyristor forced-commutating circuits are investigated.

Chapter 6 is devoted to the discussion of the principles of choppers in d.c. to d.c. conversion. Chapter 7 introduces the phase controlled cycloconverters. Chapter 8 gives a detailed account of dual converters and their characteristics. Chapter 9 deals with a.c. voltage controllers.

Chapter 10 discusses the various modern power semiconductor devices such as power transistors, power MOSFETs, GTOs, IGBTs, SITs and SITHs. Device structures and physical operations are described and typical terminal characteristics are shown.

Protection, cooling and mounting of SCRs is discussed in Chapter 11. Power electronics control of d.c. and a.c. motors is treated in Chapters 12 and 13 respectively. Chapter 14 considers power electronic application circuits.

Most importantly, it was the help and advice of Tata McGraw-Hill Publishing staff that made this whole project a reality. In particular, we wish to thank Ms Vibha Mahajan, Assistant Sponsoring Editor, Mini Narayanan, Copy Editor, and Anjali Razdan, Proofreader, of Tata McGraw-Hill. We are grateful to the authorities of SSGM College of Engineering, Shegaon, for providing all the facilities necessary for writing the book.

We would like to express our thanks for the many useful comments and suggestions provided by colleagues who reviewed this book during the course of its development, especially to Prof. J K Chatterjee of IIT Delhi and Dr Murugesh Mudaliar of BMS College of Engineering, Bangalore.

Finally, we would like to thank our family members for their love, patience and understanding during the preparation of the book.

M D Singh
K B Khanchandani

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We are fortunate to have received many useful comments and suggestions from students, which have helped in improving the technical content and clarity of the book. We are grateful to all of them.

We are indebted to many readers in the academia and industry worldwide for their invaluable feedback and for taking the trouble to draw our attention to the improvements required and the errors in the first edition.

Our special thanks goes to the reviewers of the first edition who have helped tremendously in shaping the revised edition.

Prof Ms. Prerna Gaur (NSIT, Delhi) and Dr. Yaduvir Singh (TIET, Patiala) we very much hope that the above reviewers and others will keep the feedback coming.

Most importantly, it was the help and the advice of McGraw-Hill Education (India) staff that made this whole project a reality. In particular, we wish to thank Vibha Mahajan, Shalini Jha, Mini Narayanan and Anjali Razdan for their support, encouragement and hard work in bringing out this book. We are grateful to the authorities of SSGM College of Engineering, Shegaon, for providing all the facilities for writing this book.

Finally, the authors are grateful to their families for their love, tolerance, patience and support throughout this very time-consuming project. Readers of the book are welcome to send their comments and feedback.

M D Singh
K B Khanchandani

Chapter 1

Power Electronic Systems: An Overview

LEARNING OBJECTIVES:

- To become familiar with the power-electronic systems.
- To understand the overall systems view of power electronic converters.
- To introduce various power semiconductor devices.
- To consider the applications of power electronics.
- To introduce the simulation techniques for power electronic circuits.

1.1 INTRODUCTION

Generally, the electrical engineering field may be divided into three areas of specialization:

• Electronics • Power • Control

Electronics essentially deals with the study of semiconductor devices and circuits for the processing of information at lower power levels. In this rapidly developing society, electronics has emerged as the most important branch of engineering. The power area deals with both rotating and static equipment for the generation, transmission, distribution and utilisation of vast quantities of electrical power. The transmission and distribution system is a very vital link between generation and utilisation of electrical power and the relative strength of this system indicates the quality of electric power in a country. In India, after successfully establishing capabilities of generating electric power through various sources like hydel, thermal, nuclear, gas etc. a policy decision has been taken to give the highest priority to the transmission and distribution system in the 90's.

The control area deals with the stability and response characteristics of closed-loop systems using feedback on either a continuous or sampled-data basis.

Power electronics deals with the use of electronics for the control and conversion of large amounts of electrical power. The design of power electronics equipment involves interactions between the source and the load, and utilises small-signal electronic control circuits as well as power semiconductor devices. Therefore, power electronics draws as well as depends upon all other areas of electrical engineering.

Power electronics constitute a vast, complex and interdisciplinary subject that has gone through rapid technological evolution during the last four decades. As the technology is advancing and apparatus cost is decreasing along with the improvement of reliability, their applications are expanding in industrial, commercial, residential, military, aerospace and utility environments. Many innovations in power semiconductor devices, converter topologies, analytical and simulation techniques, electrical machine drives, and control and estimation techniques are contributing to this advancement. The frontier of the technology has been further advanced by the artificial intelligence (AI) techniques, such as fuzzy logic and artificial neural networks, thus bringing more challenge to power electronic engineers.

In the global industrial automation, energy generation, conservation of the 21st century, the widespread impact of power electronics is inevitable. In this chapter, we will overview the power devices, converters and applications of power electronics.

1.2 HISTORY OF POWER ELECTRONICS DEVELOPMENT

Until 1956, the application of semiconductors was confined to low power circuits and electronic engineering was also called as light current engineering. In September 1956, four engineers of the Bell Telephone Laboratory, USA, published a paper entitled "*PNPN* transistor switches" in the proceedings of the Institute of Radio Engineers. This paper triggered intensive research on *PNPN* devices. In 1957, Gordon Hall of General Electric Company, USA, developed the three terminal *PNPN* silicon based semiconductor device called as *silicon controlled rectifier* (SCR). Continuous modifications and improvement in its design as well as fabrication techniques have made it more and more economical and suitable for various control purposes. Later on, many other power devices having characteristics similar to that of an SCR were developed. Actually, the origin of power electronics can be traced back to the time when mercury arc devices were employed for the rectification of a.c. to d.c. or the inversion of d.c. to a.c. However, the rapidly increasing usage of power electronics nowadays has resulted from the development of solid state power devices.

1.3 POWER ELECTRONIC SYSTEMS

Block diagram of the generalised power electronics system is shown in Fig. 1.1 Power source may be an ac supply system or a dc supply system. In India, 1-phase and 3-phase 50 Hz ac supplies are readily available in most locations. Very low power drives (systems employed for motion control are called drives) are generally fed from 1-phase source. Rest of the drives are powered from 3-phase source. Low and medium power motors (tens of kilowatts) are generally fed from 400 V supply; for high ratings, motors may be rated at 3.3 kV, 6.6 kV, 11 kV and higher. In case of aircraft and space applications, 400 Hz ac supply is generally used to achieve high power to weight ratio for motors. In main line traction, a high voltage supply is preferred because of economy. In India, 25 kV, 50 Hz supply is employed.

Some loads are powered from a battery, e.g. fork lift trucks and milk vans. Depending on size, battery voltage may have typical values of 6 V, 12 V, 24 V, 48 V and 110 V dc. Solar powered drives which are used in space and water pumping applications are fed from a low voltage dc supply. Presently, though these drives are very expensive but have a great future for rural water pumping and low power transport applications.

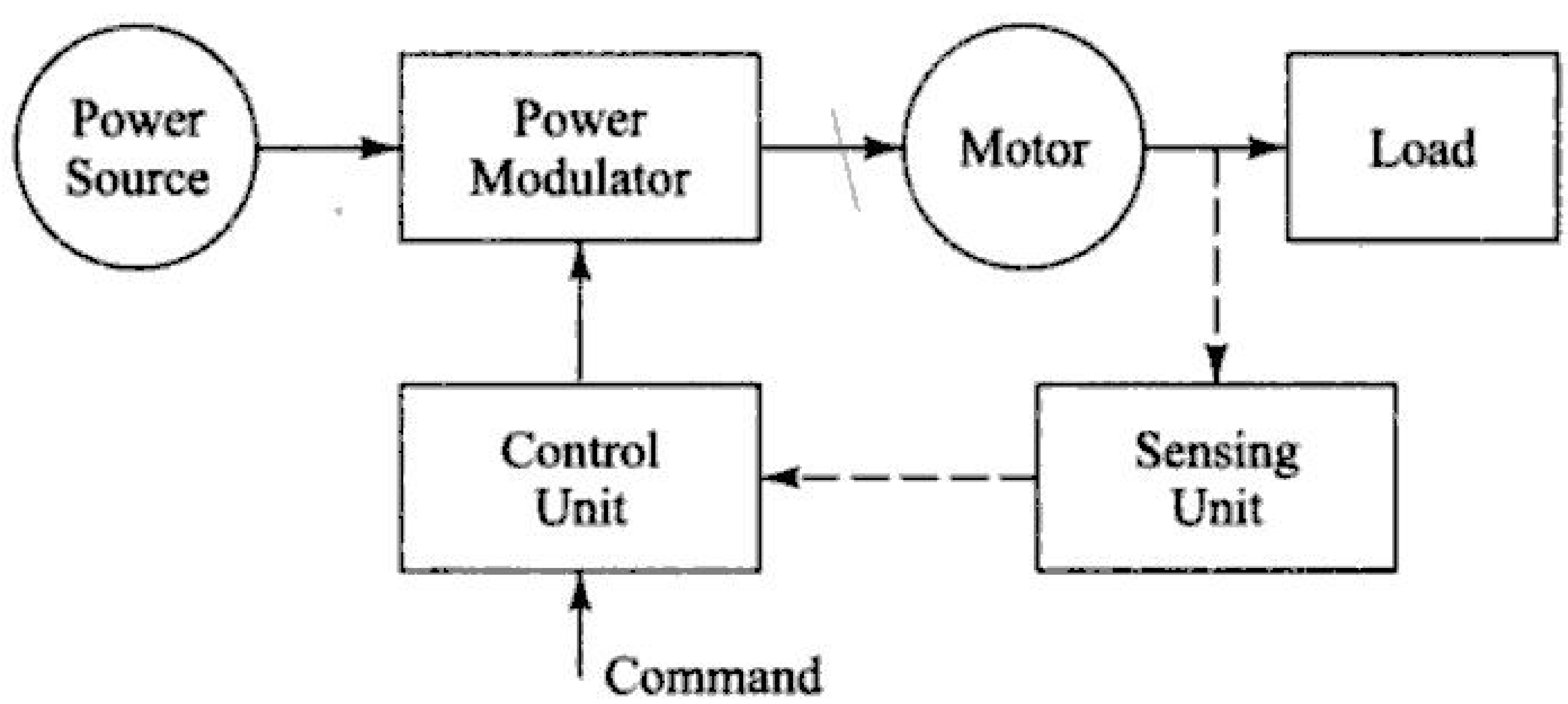


Fig. 1.1 *Block diagram of power electronic system*

Power modulator performs one or more of the following four functions:

(i) Converts electrical energy of the source as per the requirement of the load. For example, if the load is a dc motor, the modulator output must be adjustable direct voltage. In case the load is a 3-phase induction motor, the modulator may have adjustable voltage and frequency at its output terminals. When power modulator performs this function, it is known as converter.
(ii) Selects the mode of operation of the motor, i.e. motoring or braking.
(iii) Modulates flow of power from the source to the motor in such a manner that motor is imparted speed-torque characteristics required by the load.
(iv) During transient operations, such as starting, braking and speed reversal, it restricts source and motor currents within permissible values; excessive current drawn from source may overload it or may cause a voltage dip.

Motors commonly used in power electronic systems are:

(i) DC motors (shunt, series, compound and permanent magnet)
(ii) Induction motors (squirrel-cage, wound rotor and linear)
(iii) Synchronous motors (wound field and permanent magnet)
(iv) Brushless dc motors
(v) Stepper motors and
(vi) Switched reluctance motors

Power modulators are controlled by a control unit. Nature of the control unit for a particular system depends on the power modulator that is used. Control unit operates at much lower voltage and power levels. Sensing unit measures the load parameters, say speed in case of a rotating machine and compares it with the command. The difference of the two parameters processed by the control unit components now controls the turn-on of power semiconductor devices which are used in power modulators. As desired, the behaviour of the load circuit can be controlled over a wide range with the adjustment of the command.

1.4 POWER SEMICONDUCTOR DEVICES

The progress in power electronics today has been possible primarily due to advances in power semiconductor devices. Of course, apart from device evolution, the inventions in converter topologies, pulse-width modulation (PWM) techniques, control and estimation techniques, digital signal processors, application specific integrated circuits (ASICs), control hardware and software, etc. also have contributed to this advancement.

Modern era of solid-state power electronic began with the advent of thyristor (silicon controlled rectifiers) in the late 1957.

Gradually, various types of power semiconductor devices were developed and became commercially available since 1970.

Power semiconductor devices can be classified into three categories according to their degree of controllability. The categories are:

(i) Uncontrolled turn-on and off devices (e.g. diode).
(ii) Controlled turn-on and uncontrolled turn-off (e.g. SCR).
(iii) Controlled turn-on and off characteristics [e.g. Bipolar junction transistors (BJTs), MOSFETs, Gate-turn-off thyristors (GTOs), Static induction thyristor (SITH), Insulated-gate bipolar transistors (IGBTs), static induction transistors (SITs), mos-controlled thyristors (MCTs)].

The on and off states of diodes are controlled by power circuit. Thyristors are turned-on by a control signal and are turned-off by the power circuit whereas the controllable switches are turned-on and off by controlled signals. The devices which behave as controllable switches are BJT, MOSFET, GTO, SITH, IGBT, SIT and MCT.

BJT, MOSFET, IGBT and MCT can withstand unipolar voltage whereas thyristors and GTOs can withstand bipolar voltages. BJT, MOSFET, IGBT and SIT requires continuous signal for keeping them in turn-on state but SCR, GTO, SITH and MCT requires pulse-gate signal for turning them ON and once these devices are ON, gate-pulse is removed.

Triac and RCT (reverse conducting thyristor) possess bidirectional current capability whereas all other remaining devices (diode, SCR, GTO, BJT, MOSFET, IGBT, SIT, SITH, MCT) are unidirectional current devices.

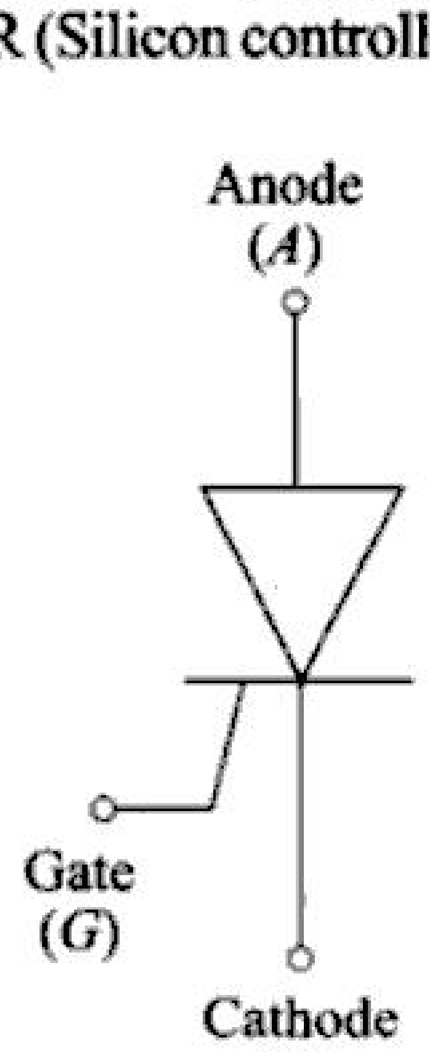
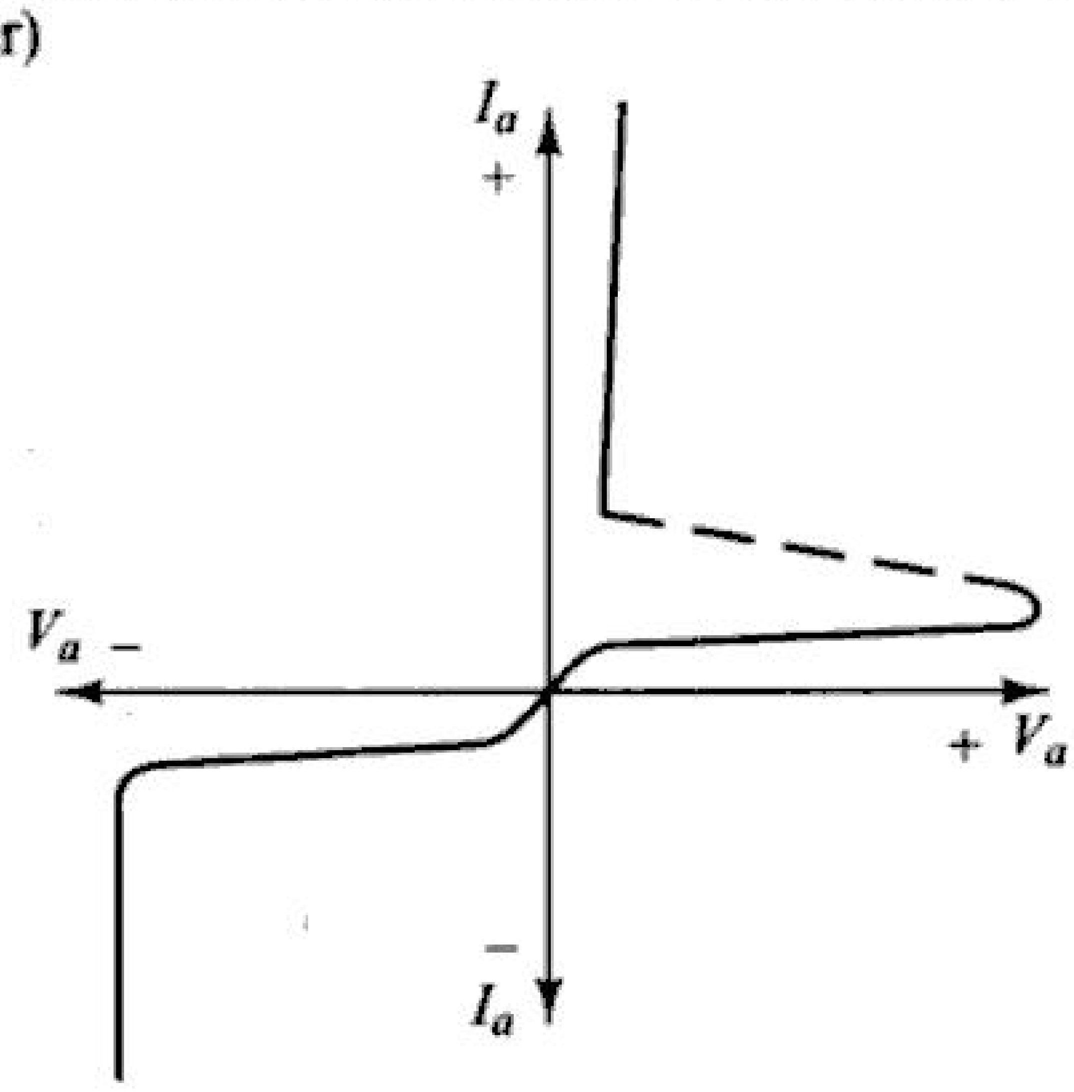
As the evolution of new and advanced devices continued, the voltage and current ratings and electrical characteristics of the existing devices began improving dramatically. In fact, the device evolution along with converter, control and system evolution was so spectacular in the last decade of 20th century, that we define it as the "decade of power electronics".

Thyristors are used for high power low frequency applications. Devices are available with 8000 V and 4000 A ratings. ABB recently introduced a monolithic ac switch that has the voltage ratings of 2.8 kV–6.5 kV and current ratings of 3000–6000 A. The advent of large GTOs push the thyristor voltage-fed inverter from the market. Currently, GTOs are available with 6000 V, 6000 A (Mitsubishi) ratings for large voltage-fed inverter applications.

Power MOSFET has grown in rating, but it's primary popularity is in high-frequency switching mode power supply and portable appliances. The BJT appeared and then fell into obsolescence due to the advent of IGBT at the higher end and power MOSFET at the lower end. The invention of IGBT is an important milestone in the history of power semiconductor devices. Commercial IGBTs are available with 3500 V, 1200 A, but upto 6.5 kV and 10 kV devices are under test in laboratory. Trench gate IGBT with reduced conduction drop is available upto 1200 V, 600A. IGBT intelligent power modules (IPM) from a number of vendors are available for 600 V, 50-300 A and 1200 V, 50-150 A to cover upto 150 hp ac drive applications.

Integrated Gate-Commutated Thyristor (IGCT) is basically a hard-driven GTO with built-in gate driver, and the device is available with 6000 V, 6000 A (10 kV devices are under test). Recently, ABB introduced reverse blocking IGCT (6000 V, 800 A) for use in current-fed inverter drives. Large band gap power semiconductor device with silicon carbide (SiC) that has high carrier mobility, high electrical and thermal conductivities and strong radiation hardness is showing high promise for next generation power devices. These devices can be fabricated for higher voltage, higher temperature, higher frequency and lower conduction drop. SiC diodes are commercially available, and other devices are expected in future. Table 1.1 lists some power devices and shows their respective V-I characteristics and symbolic representation. We will study all these devices in Chapter 5.

Table 1.1 Power devices, their characteristics and symbolic representation

Power devices	*Symbols*	*V-I characteristics*
(1) SCR (Silicon controlled rectifier)		

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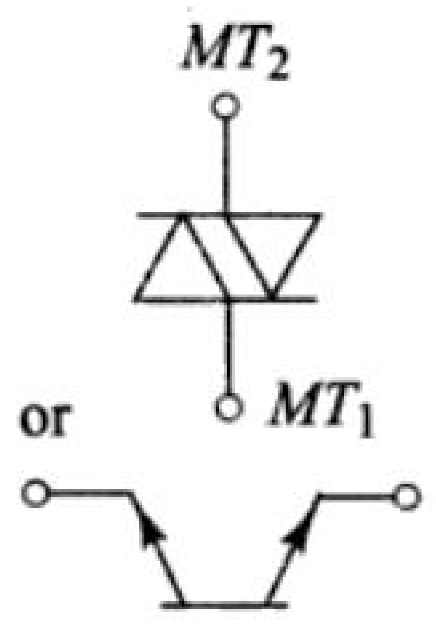
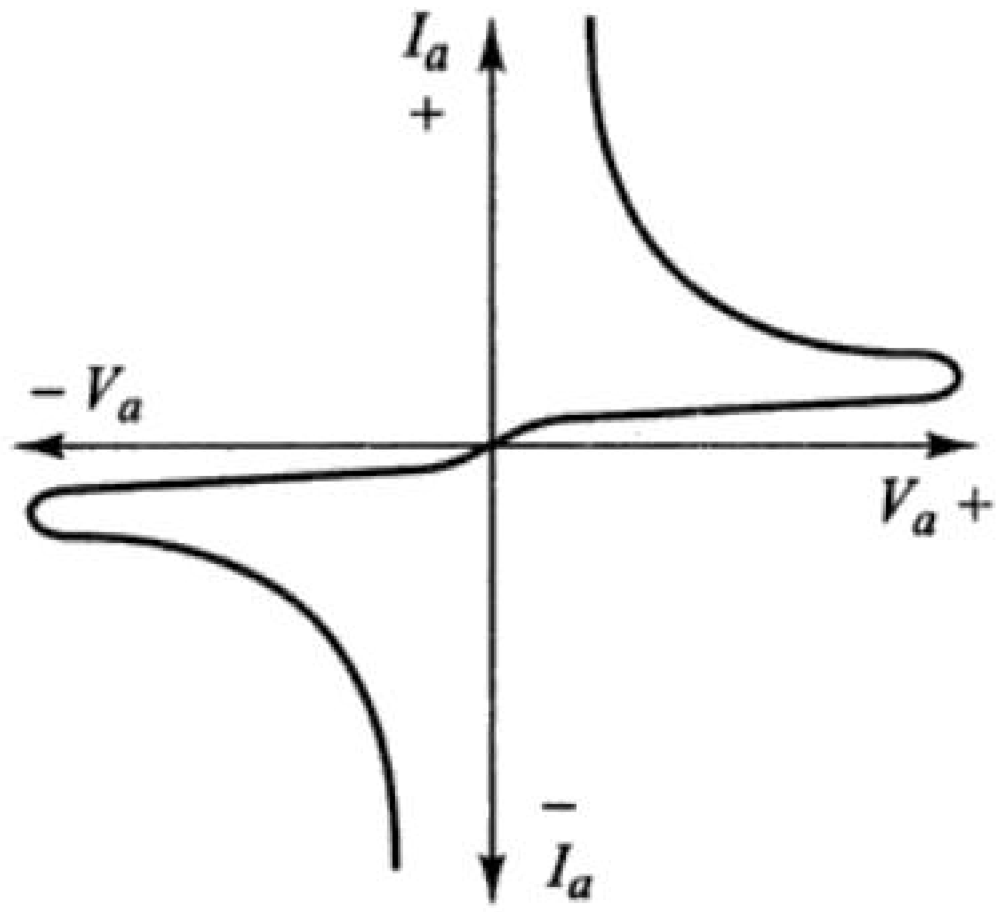
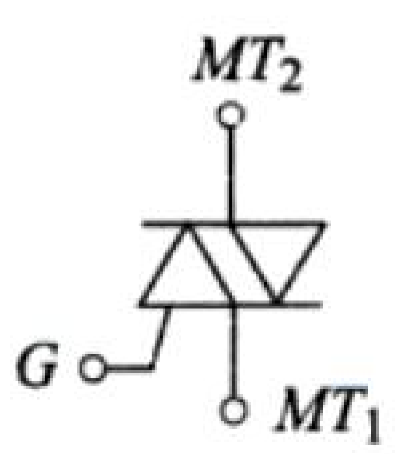
Power devices	Symbols	V-I characteristics

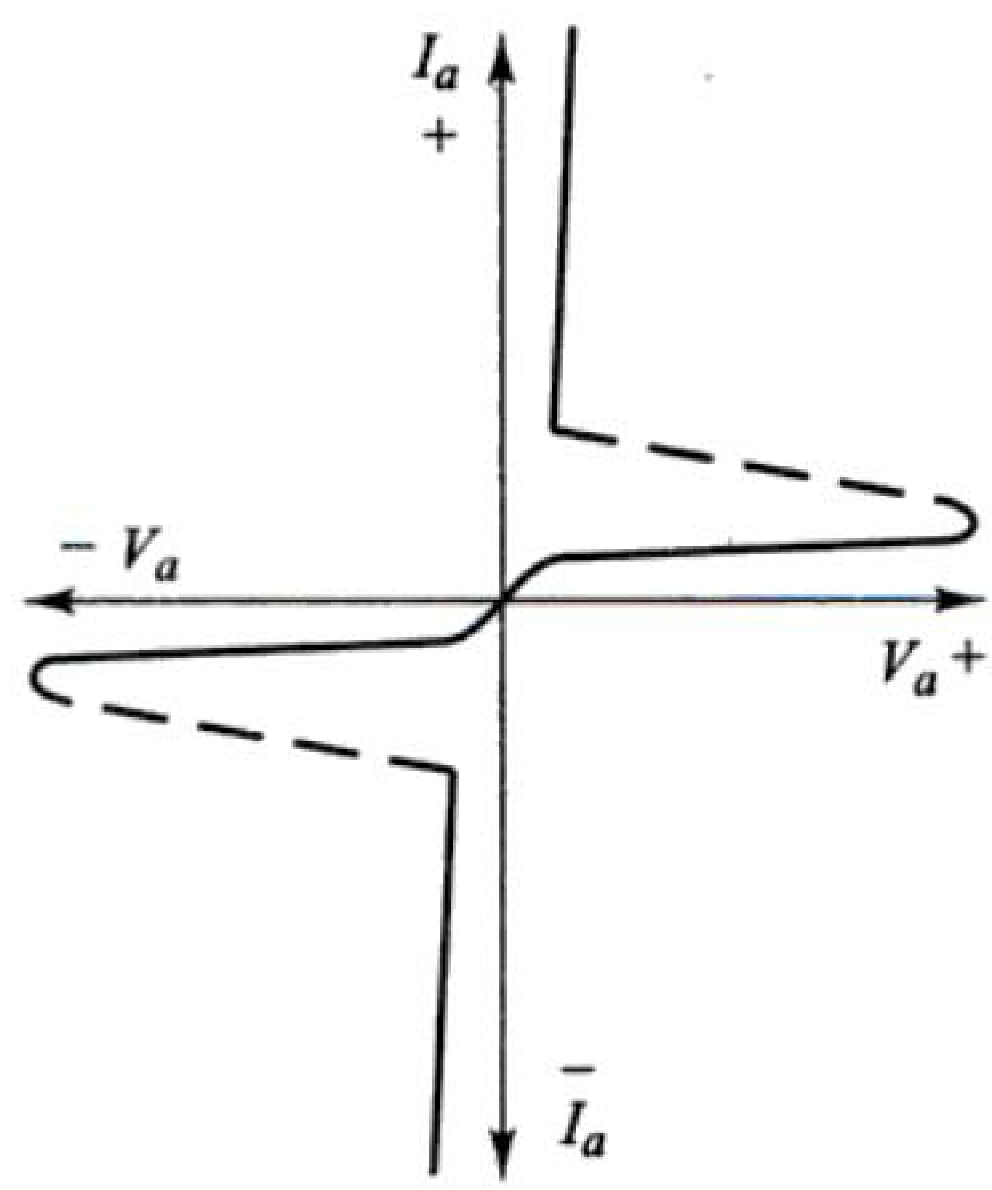
(2) DIAC (Bidirectional diode thyristor)



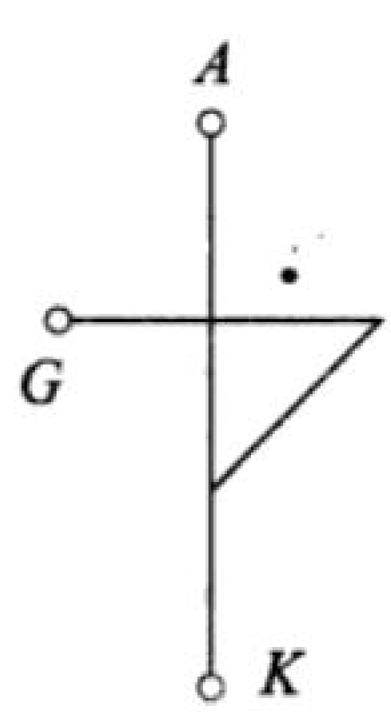


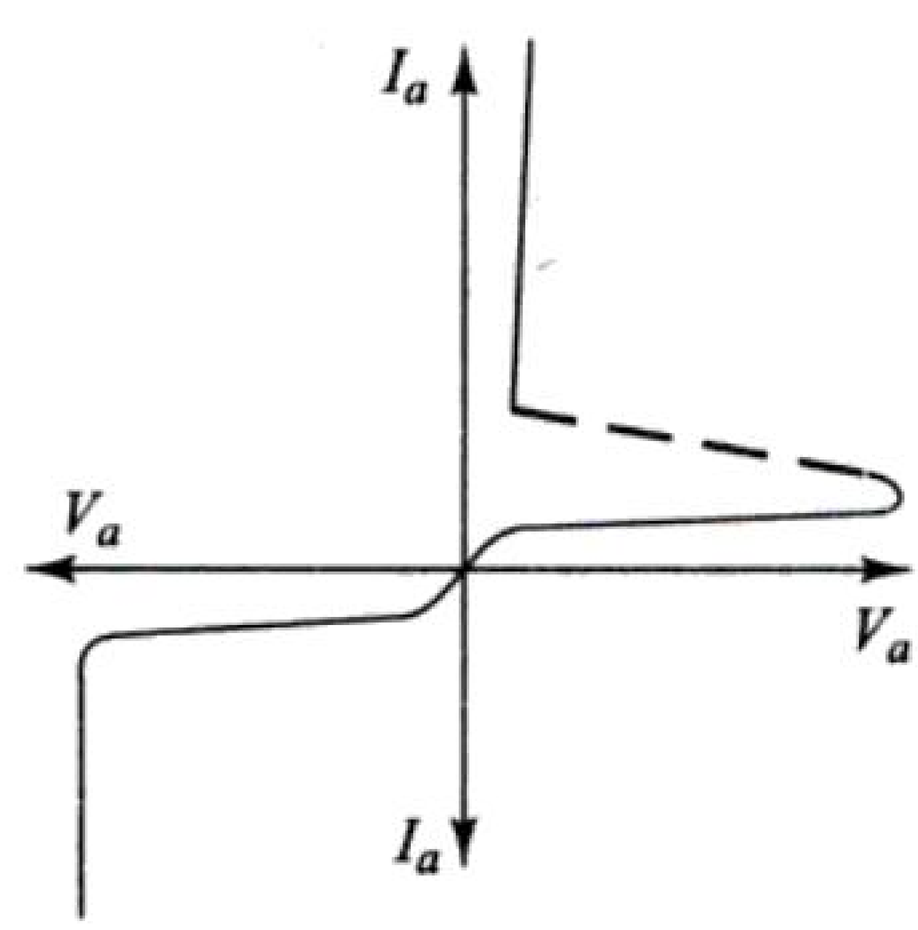
(3) TRIAC (Bidirectional triode thyristor)





(4) SUS (Silicon unilateral switch)





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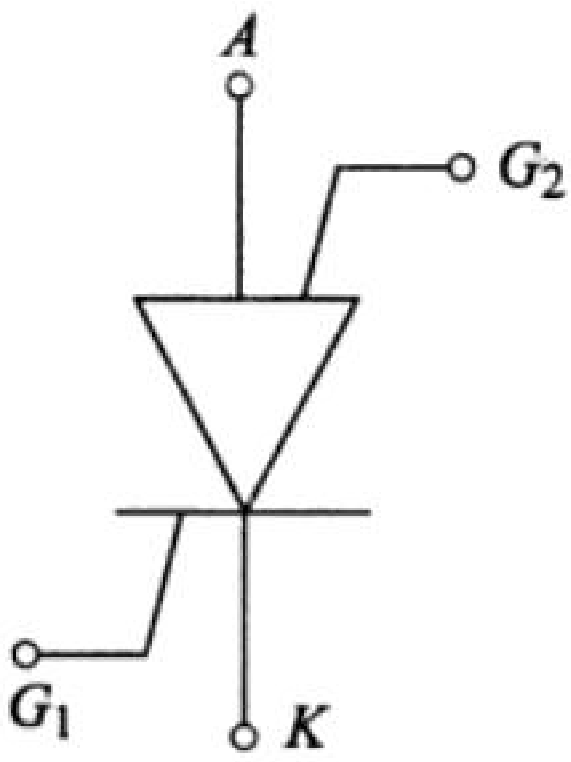
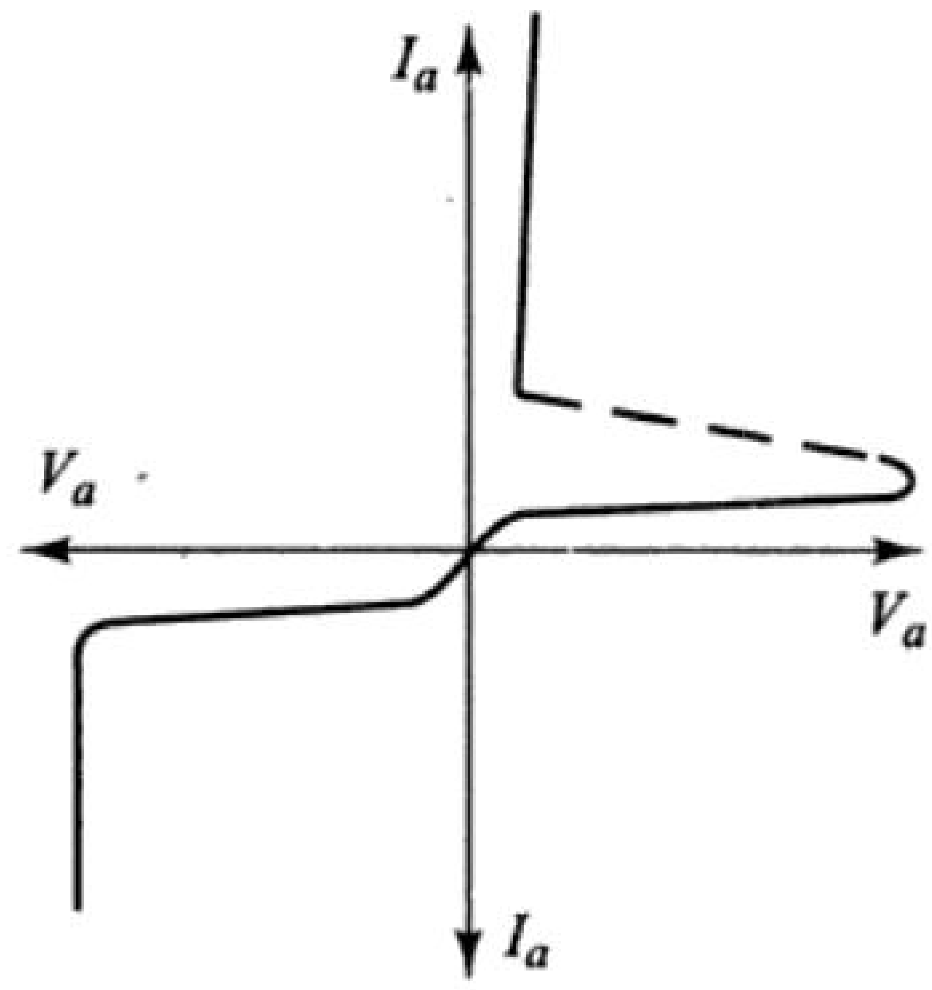
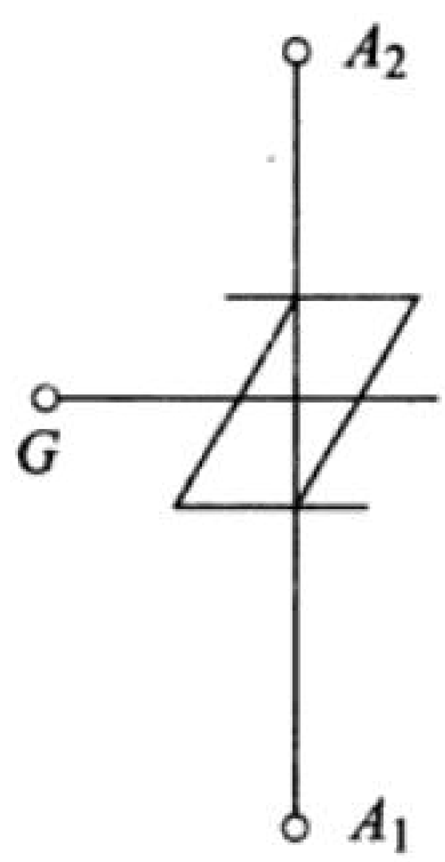
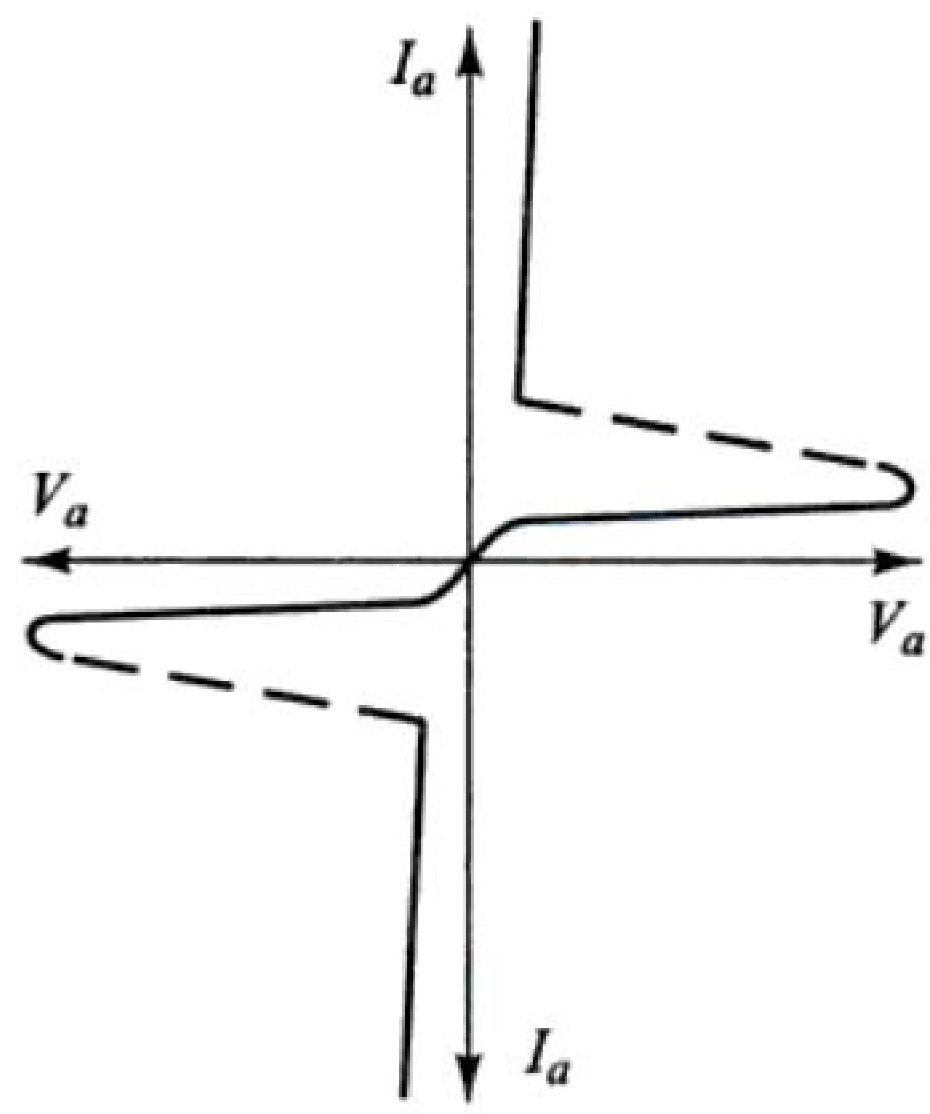
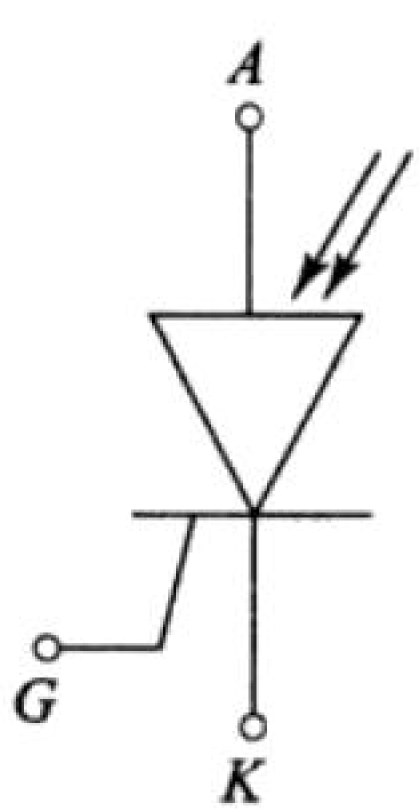
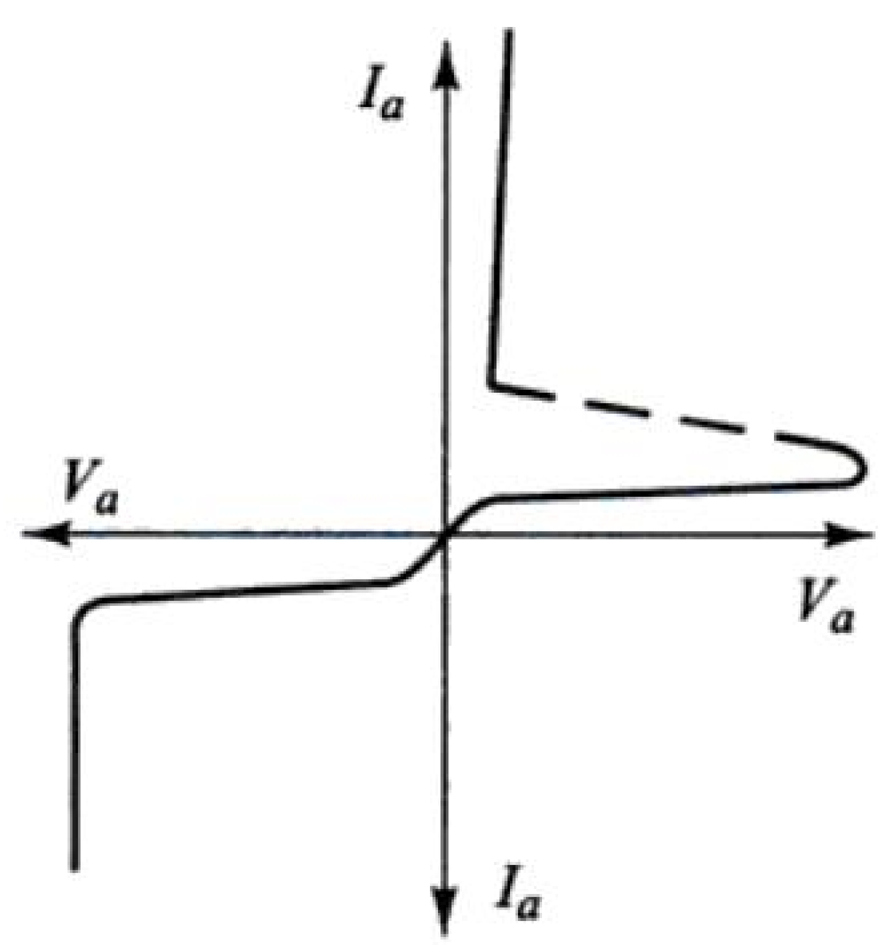
Power devices	*Symbols*	*V-I characteristics*
(5) SCS (Silicon controlled switch)		
(6) SBS (Silicon bilateral switch)		
(7) LASCR (Light activated SCR)		

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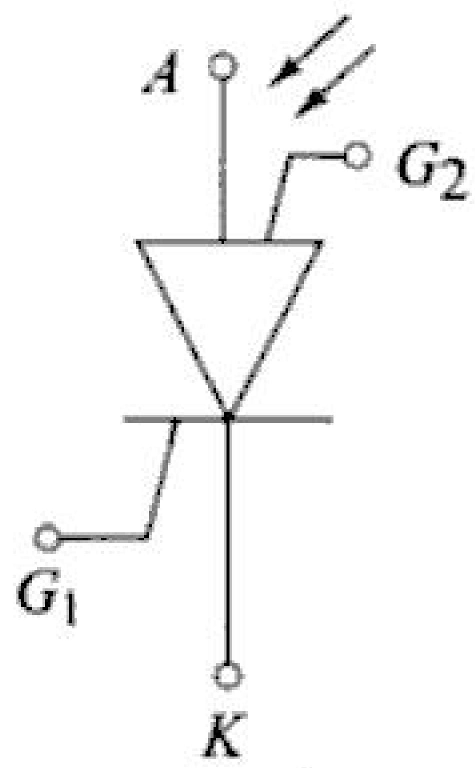
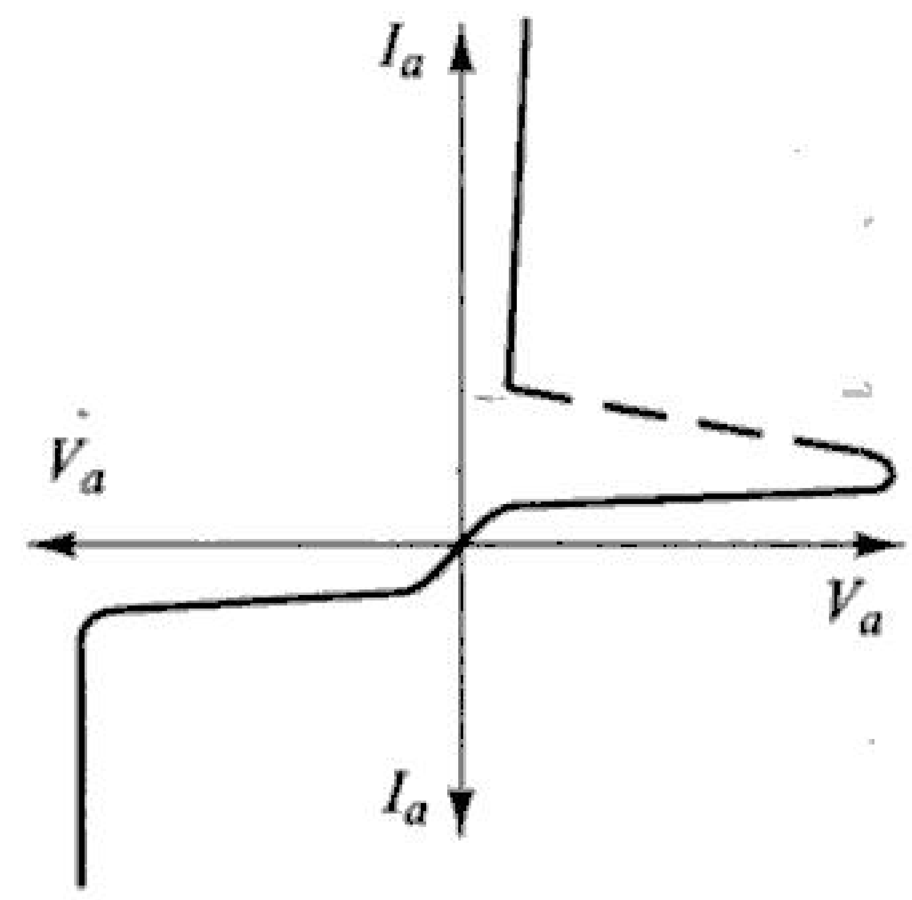
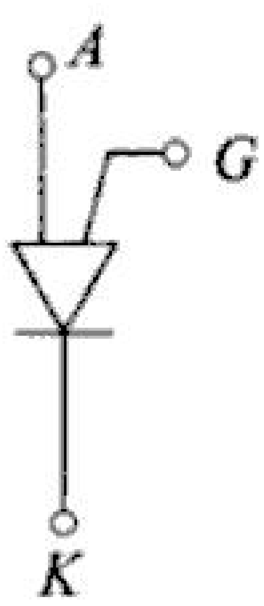
Power devices	Symbols	V-I characteristics--

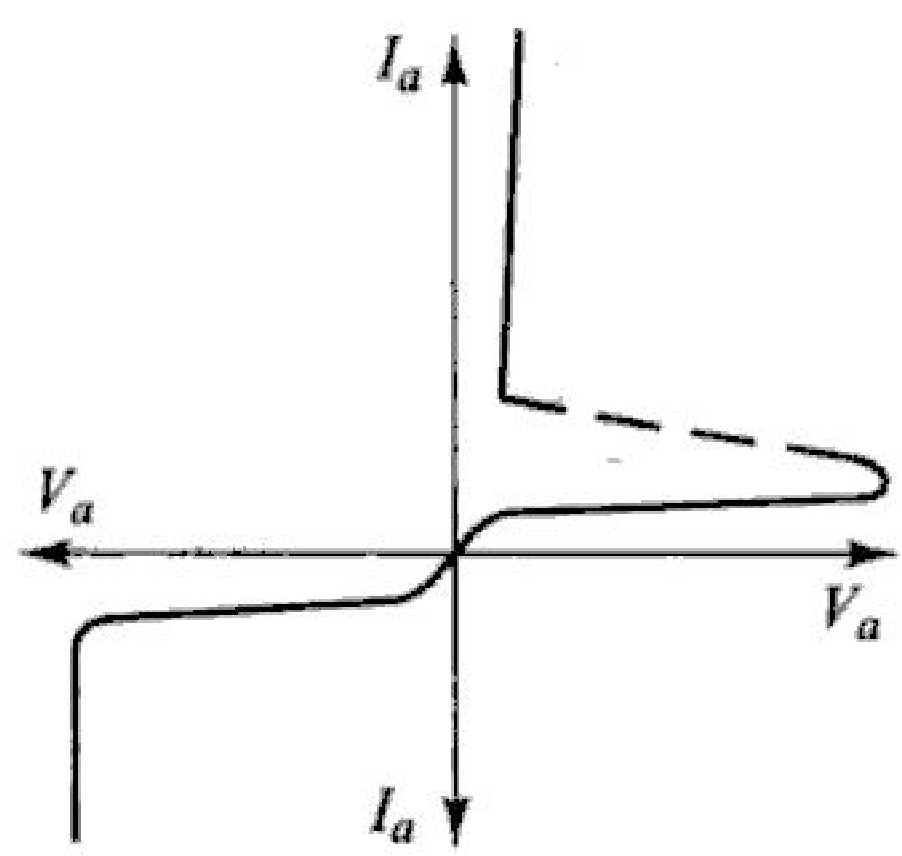
(8) LASCS (Light activated SCS)



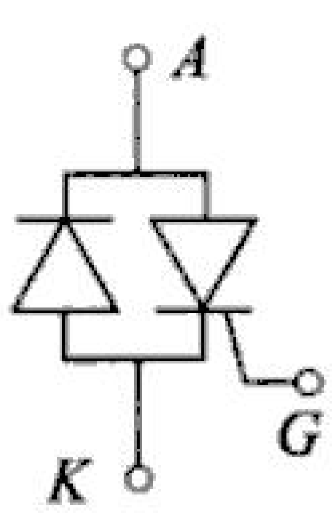


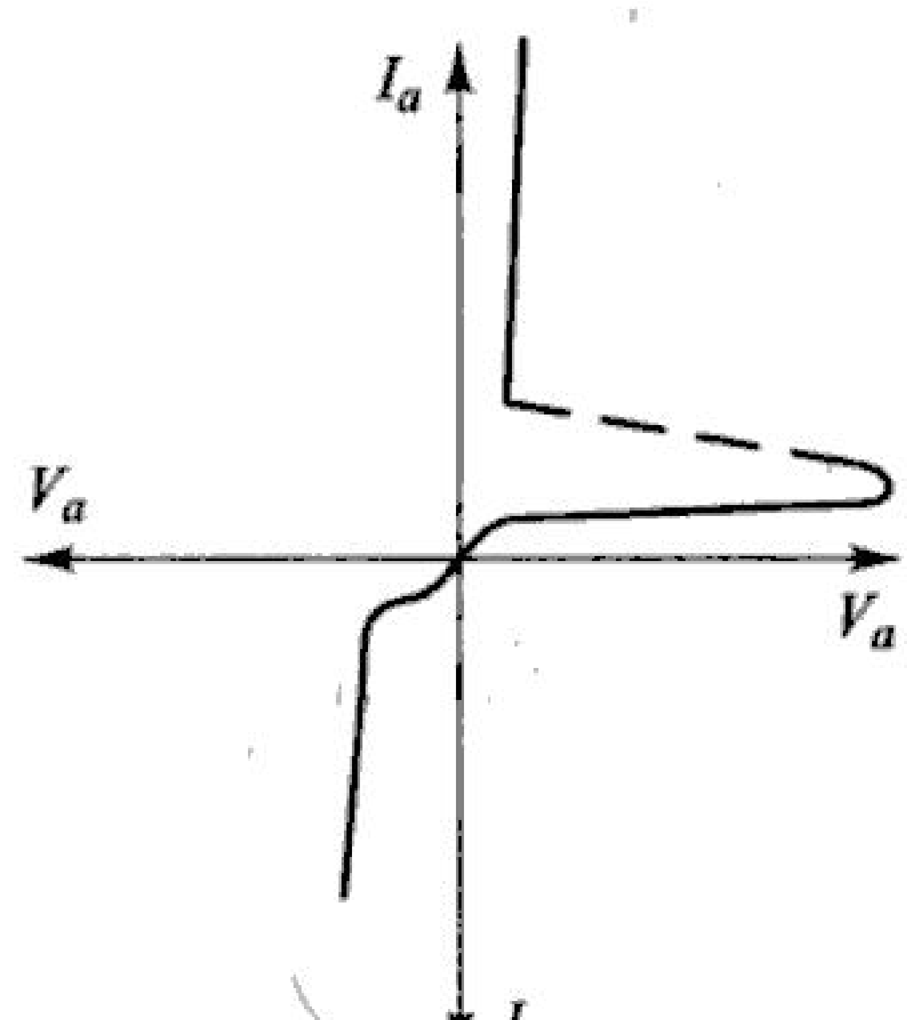
(9) PUT (Programmable unijunction transistor)





(10) RCT (Reverse conducting thyristor)

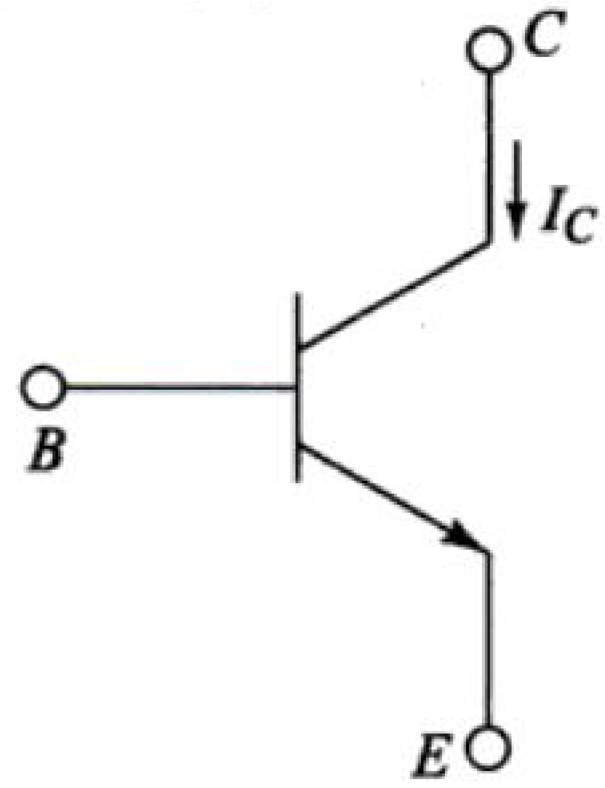


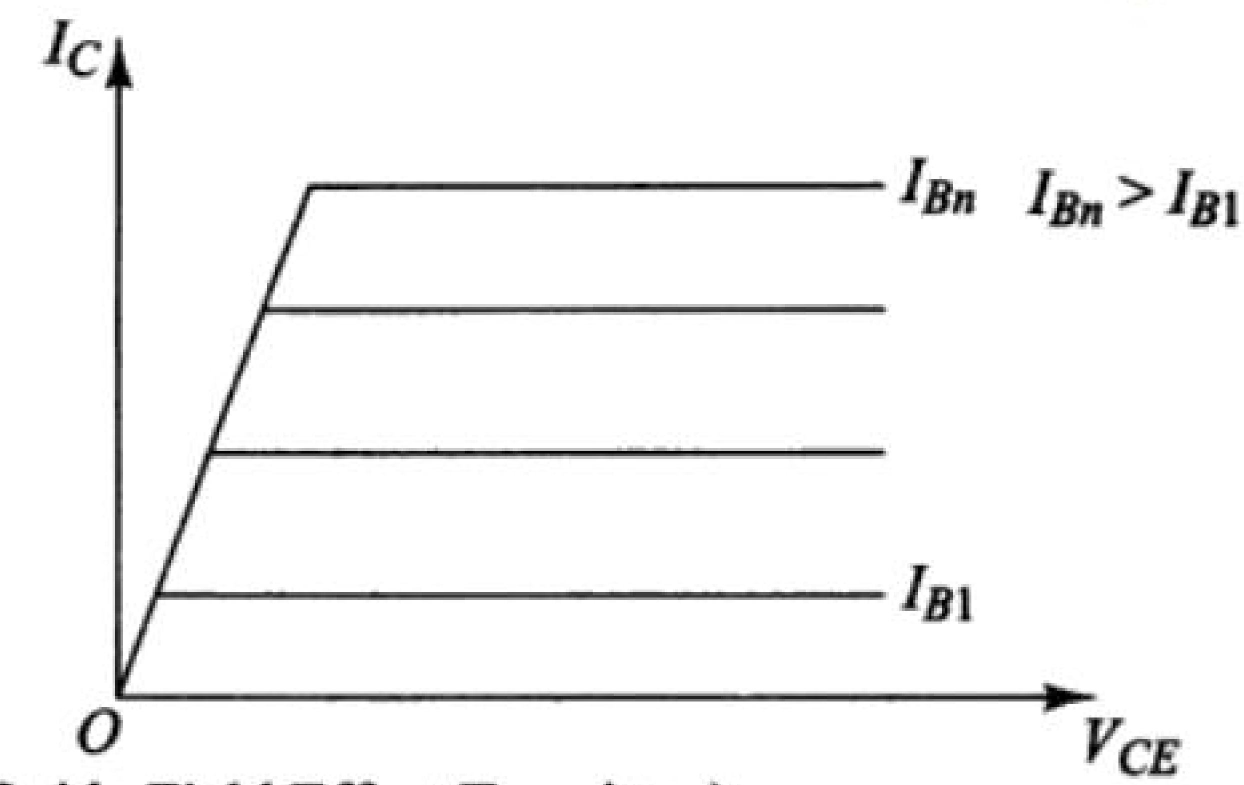


(Contd.)

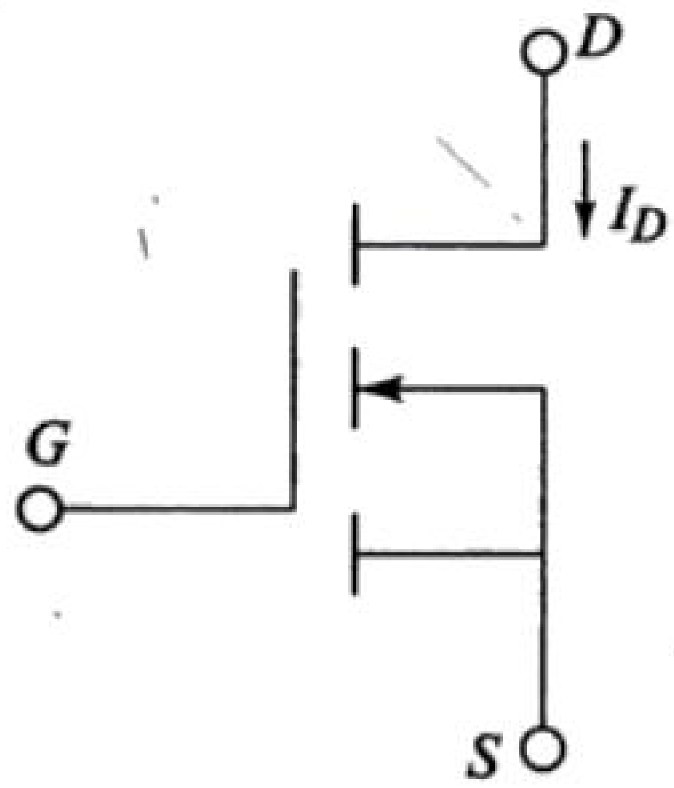
Power devices	Symbols	V-I characteristics

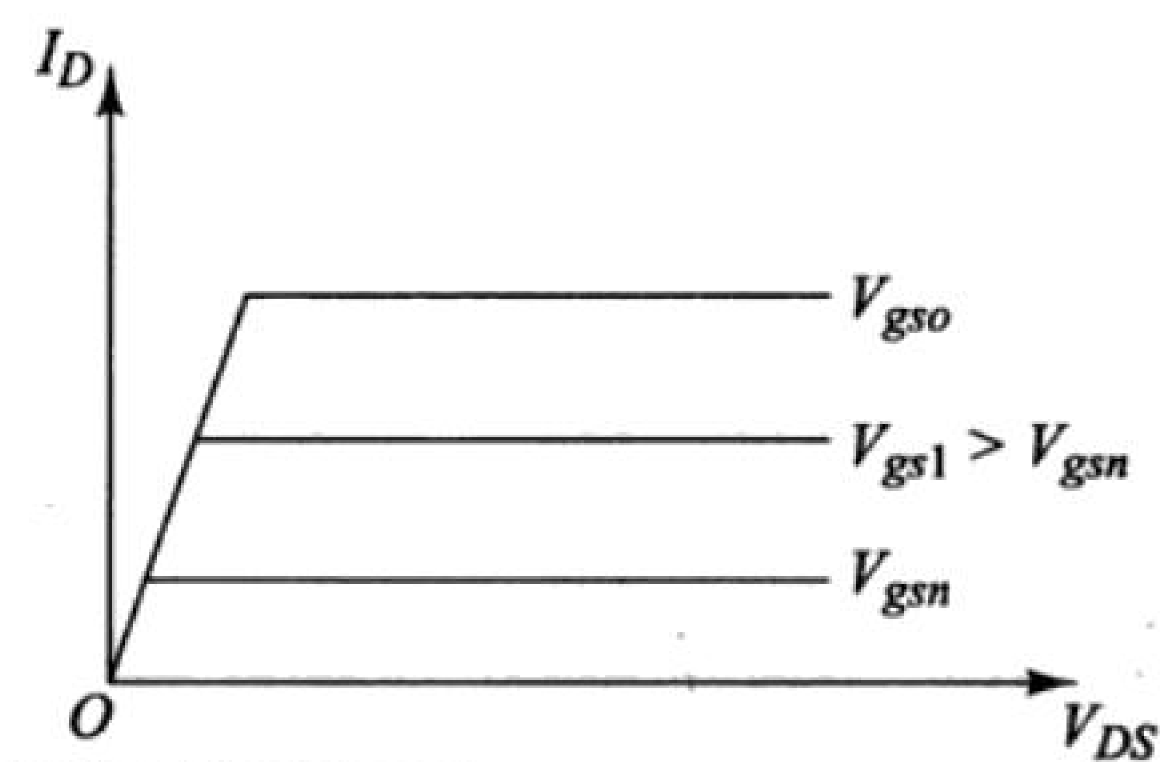
(11) BJT (Bipolar Junction Transistor)



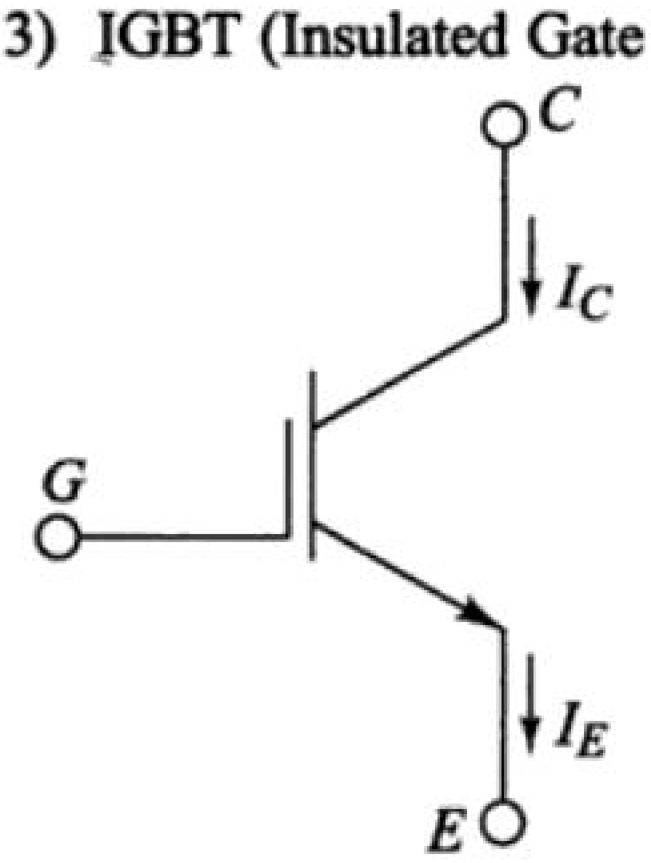


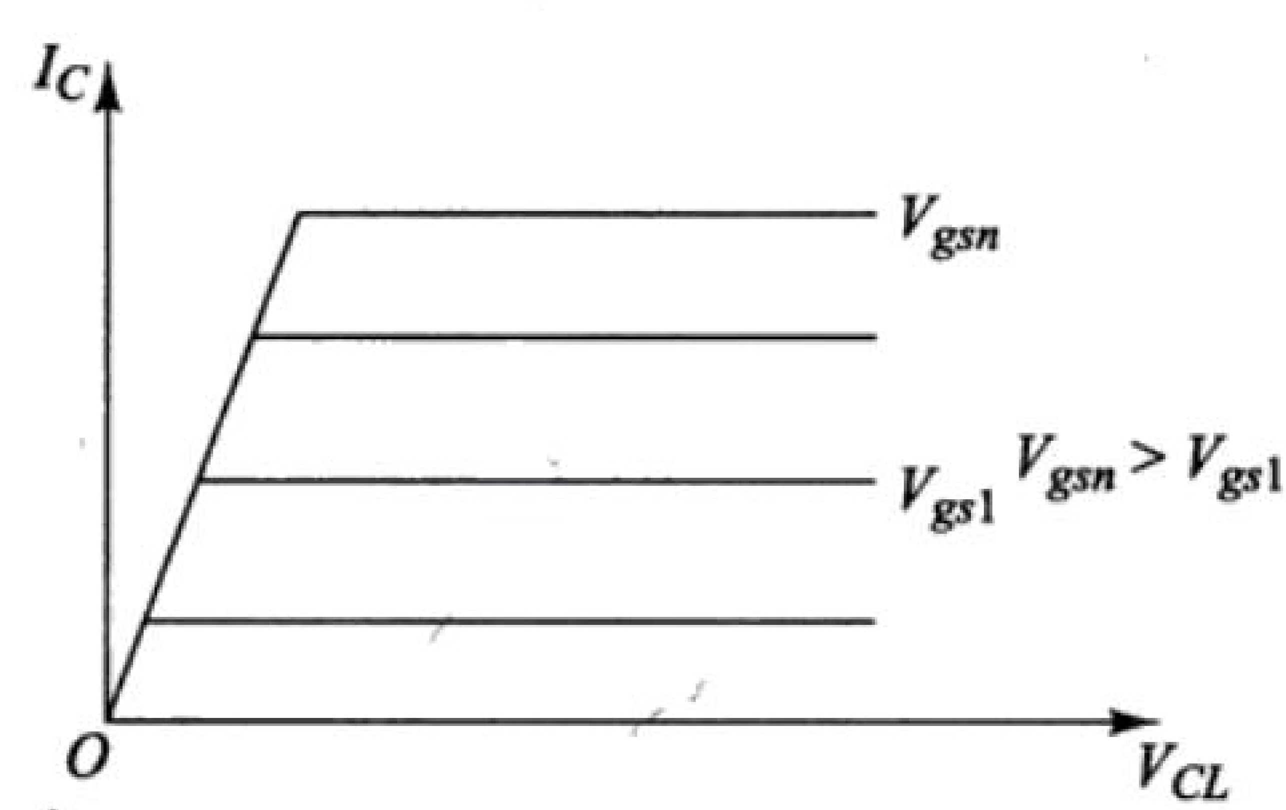
(12) N-channel MOSFET (Metal Oxide Field Effect Transistor)



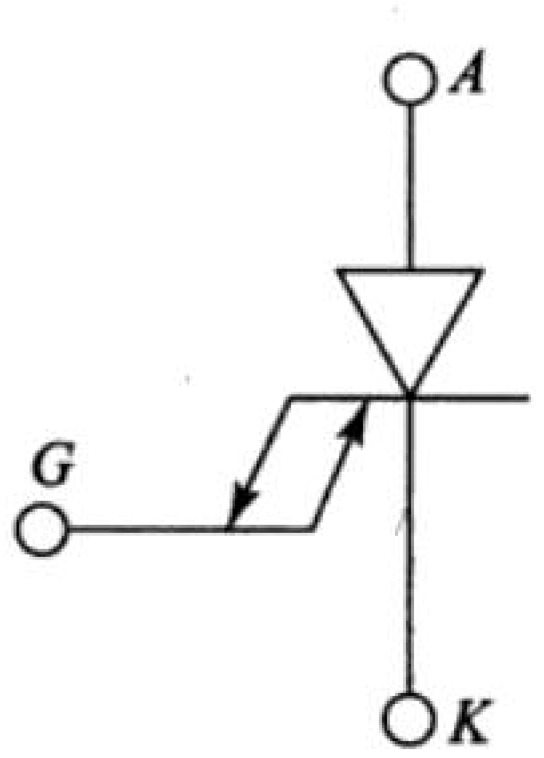


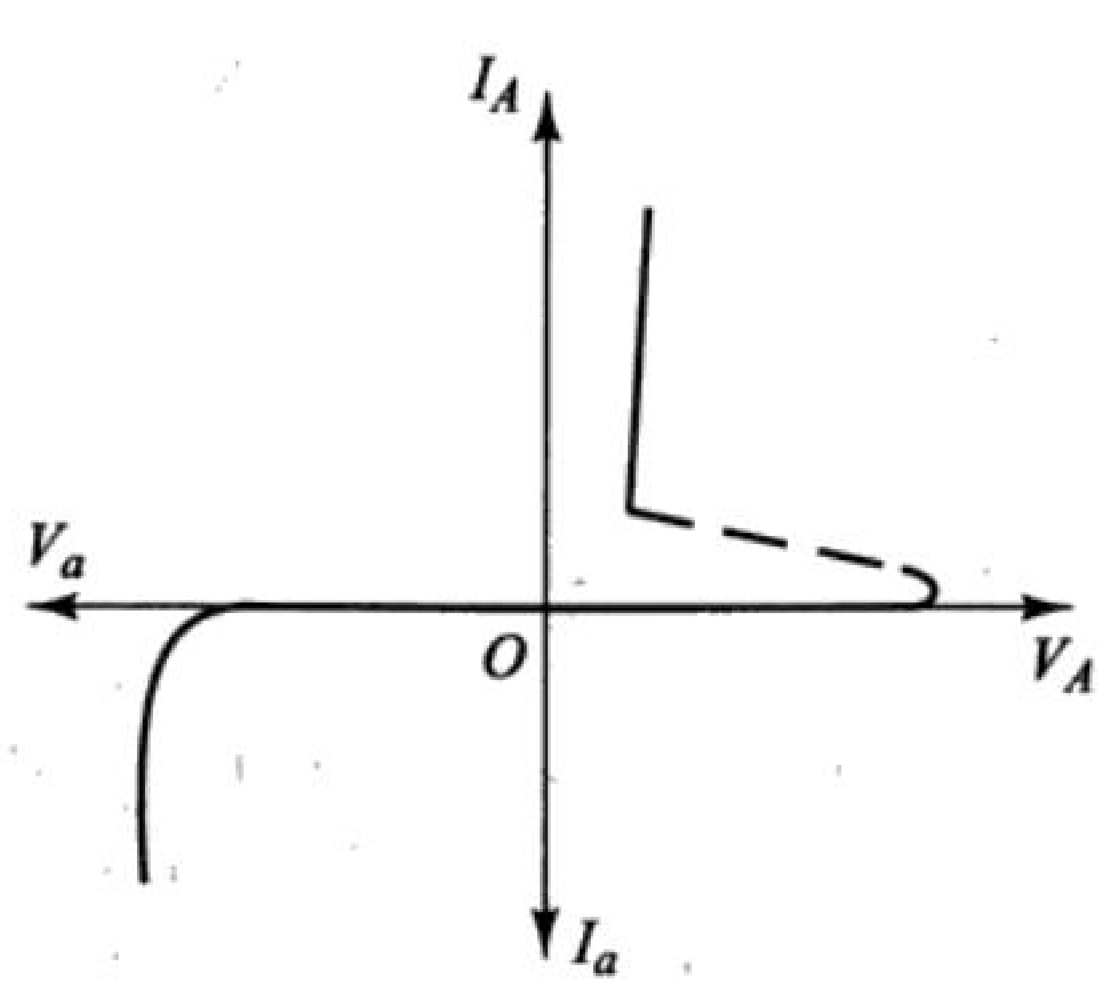
(13) IGBT (Insulated Gate Bipolar Junction Transistor)





(14) GTO (Gate-turn-off thyristors)





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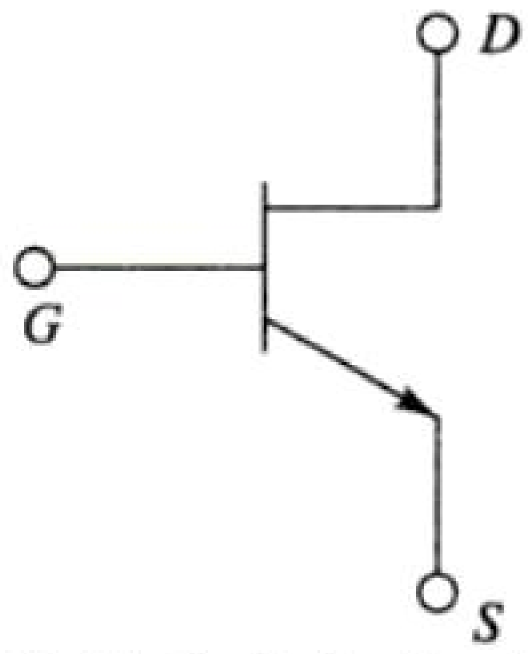
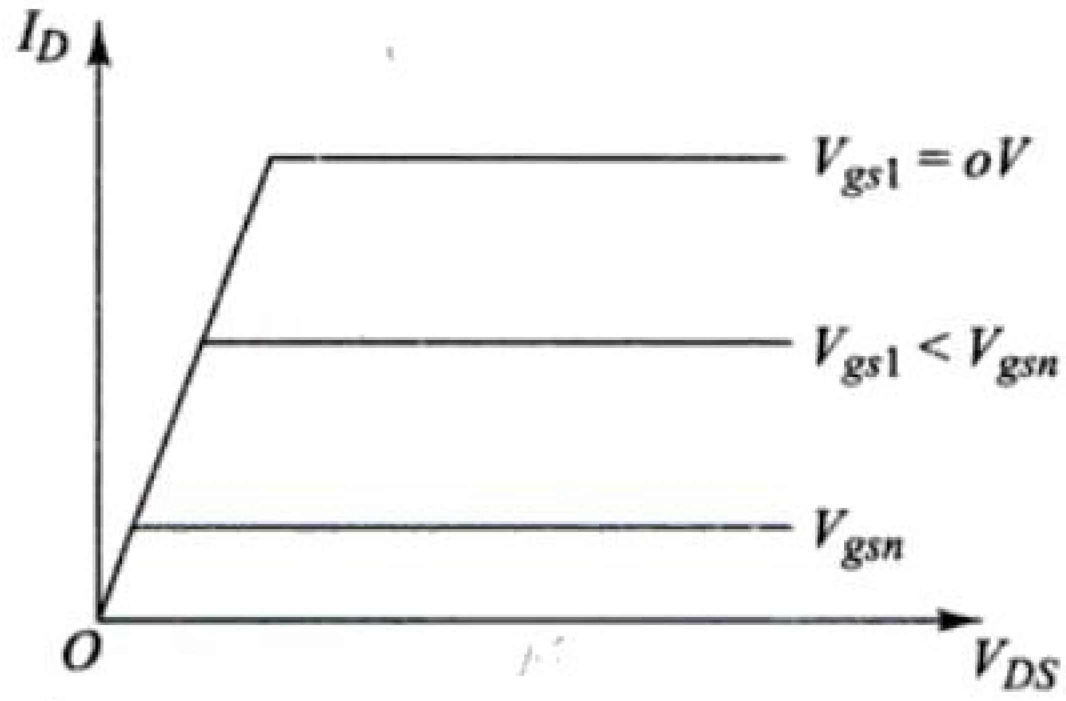
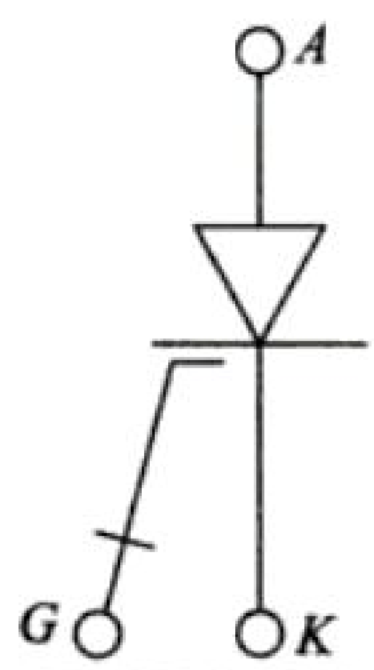
Power devices	Symbols	V-I characteristics

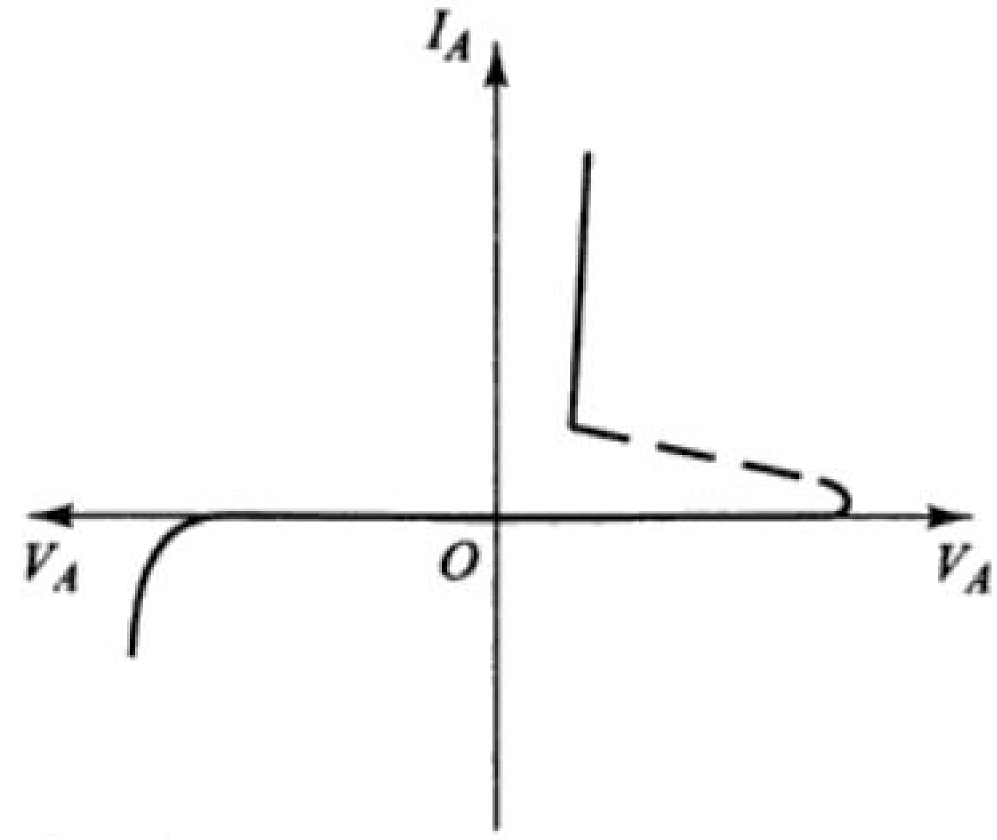
(15) SIT (Static Induction Transistor)



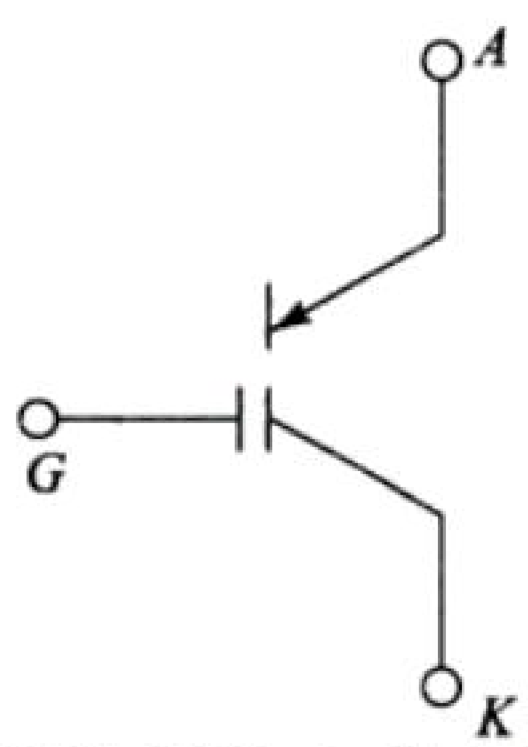


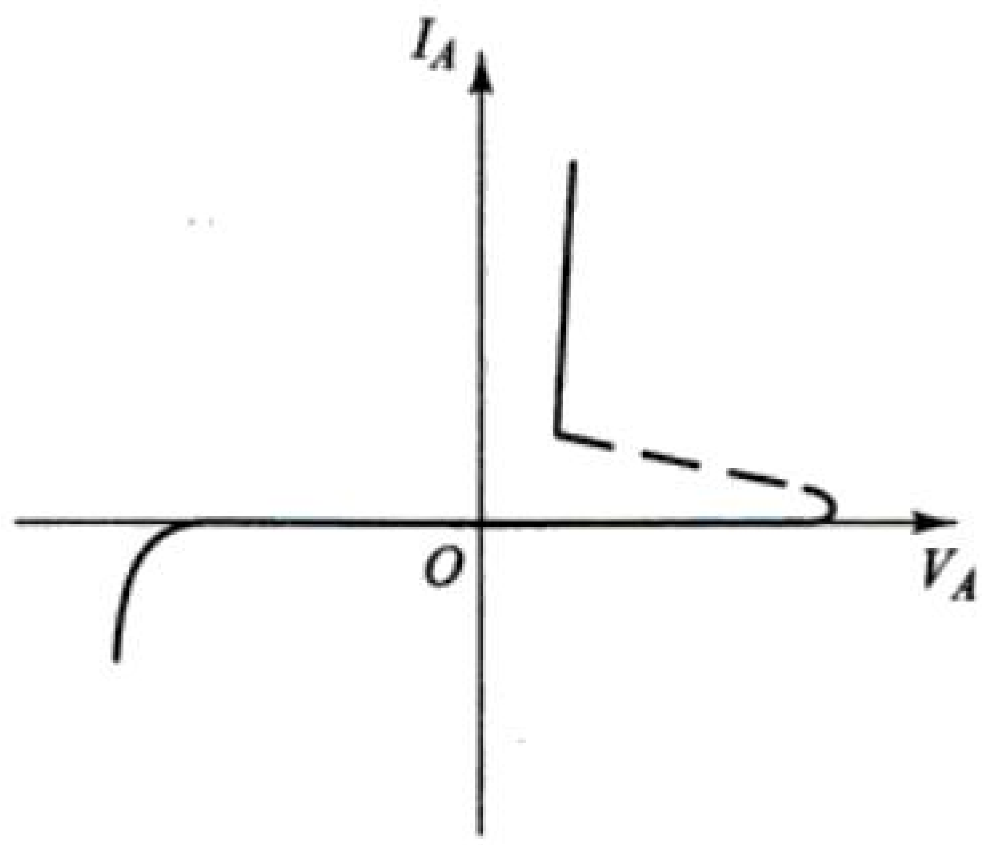
(16) SITH (Static Induction Transistor)



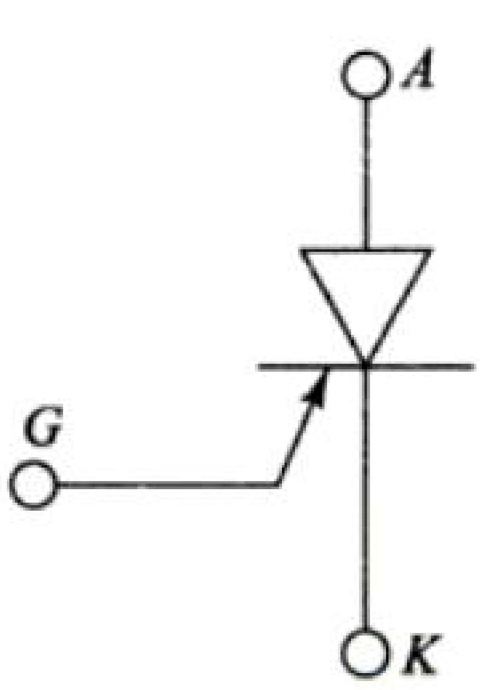


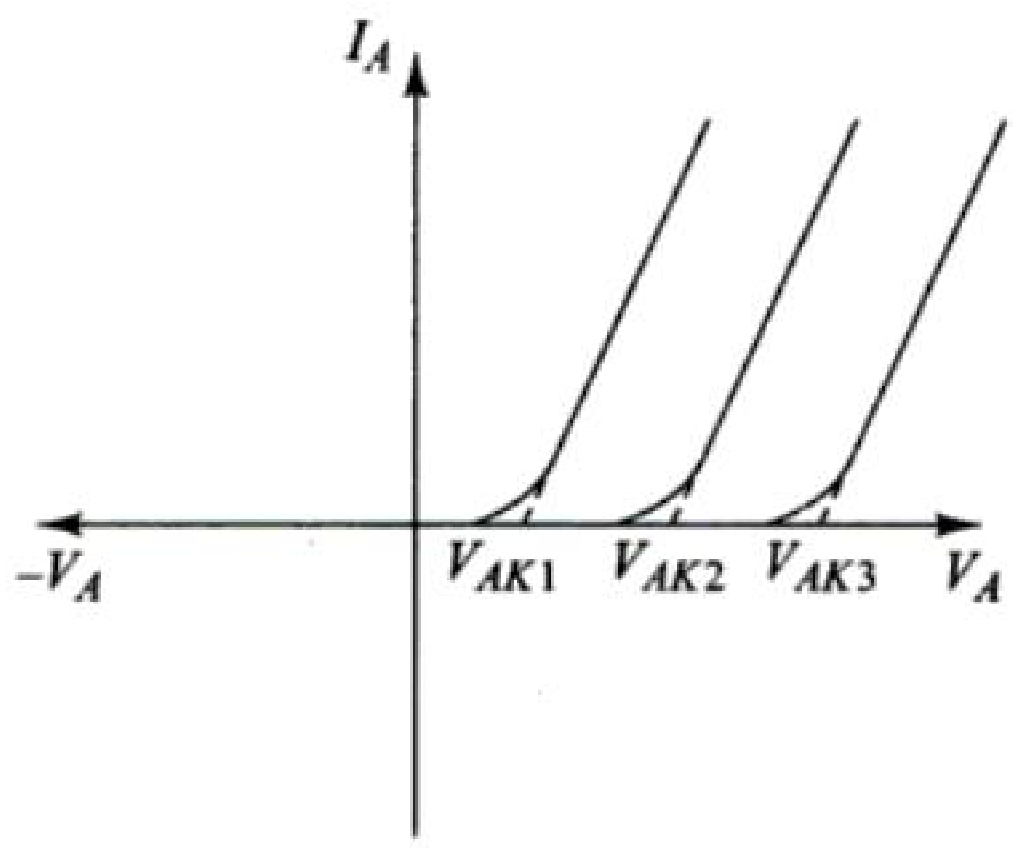
(17) N-MCT (N-MOS-Controlled Thyristor)





(18) FCT (Field Controlled Thyristor)





1.5 POWER ELECTRONIC CONVERTERS

The great strides taken in the industrial applications of power electronics during recent years have demonstrated that this versatile tool can be of great importance in increasing production, efficiency and control. Power Electronic Circuits are also called as power converters. A converter uses a matrix of power semiconductor switches to convert electrical power at high efficiency. The converter system is comprised of switches, reactive components L, C, and transformers. Switches include two terminal devices such as diodes and three terminal devices such as transistors or thyristors. These converters/controllers are generally classified into the following five broad categories:

1. Phase Controlled Rectifiers (AC to DC Converters) These controllers convert fixed ac voltage to a variable dc output voltage. These converters takes power from one or more ac voltage/current sources of single or multiple phases and delivers to a load. The output variable is a low-ripple dc voltage or dc current. These controller circuits use line voltage for their commutation. Hence they are also called as line commutated or naturally commutated ac to dc converters. These circuits include diode rectifiers and single/three phase controlled circuits. These controllers are discussed in detail in Chapter 6.

Applications: High voltage dc transmission systems
DC motor drives
Regulated dc power supplies
Static VAR compensator
Wind generator converters
Battery charger circuits

2. Choppers (DC to DC Converter) A chopper converts fixed dc input voltage to a variable dc output voltage. The dc output voltage may be different in amplitude than the input source voltage. Choppers are designed using semiconductor devices such as power transistors, IGBTs, GTOs, Power MOSFETs and thyristors. Output voltage can be varied steplessly by controlling the duty ratio of the device by low power signals from a control unit. Chopper has either a battery, a solar powered dc voltage source or a line frequency (50–60 Hz) derived dc voltage source. Choppers are discussed in Chapter 8.

Applications: DC drives
Subway cars
Battery driven vehicles
Electric traction
Switch mode power supplies

3. Inverters (DC to AC Converter) An inverter converts a fixed dc voltage to an ac voltage of variable frequency and of fixed or variable magnitude. A practical inverter has either a battery, a solar powered dc voltage source or a line frequency (50 Hz) derived dc voltage source (often unregulated). Inverters are widely used from very low-power portable electronic systems such as the flashlight discharge system in a photography camera to very high power industrial systems.

Inverters are designed using semiconductor devices such as power transistors, MOSFETs, IGBTs, GTOs and thyristors. Chapter 9 deals with the study of inverters in detail.

Applications: Uninterruptible power supply (UPS)
Aircraft and space power supplies
Induction and synchronous motor drives
High voltage dc transmission system
Induction heating supplies

4. Cycloconverters (AC to AC Converters) These circuits convert input power at one frequency to output power at a different frequency through one stage conversion. These are designed using thyristors and are controlled by triggering signals derived from a control unit.

The output frequency is lower than the source frequency. Output frequency in cycloconverter is a simple fraction such as $\frac{1}{3}, \frac{1}{5}$ and so on of the source frequency. These are mainly used for slow speed, very high power industrial drives. Cycloconverters are discussed in Chapter 10.

Applications: AC drives like rotary kilns multi-MW ac motor drives.

5. AC Voltage Controllers (AC Regulators) These converters convert fixed ac voltage directly to a variable ac voltage at the same frequency using line commutation. These converters employs a thyristorised voltage controller. Stepless control of the output voltage can be obtained by controlling firing angle of converter thyristors by low power signals from a control unit. This type of converters are briefly discussed in Chapter 11.

Applications: Lighting control
Speed control of large fans and pumps
Electronic tap changers

1.6 POWER ELECTRONIC APPLICATIONS

The importance of power electronics in industrial automation, energy systems, energy generation and conservation, and indirectly for environmental pollution control is tremendous. As the technology is maturing and cost is decreasing, power electronics is expanding in applications, such as switch mode power supplies (SMPS), UPS systems, electrochemical processes, heating and lighting, static VAR compensation, active filtering, high voltage dc system, photo-voltaic system, and variable frequency motor drives. The motor drives possibly constitute the most fascinating and complex applications of power electronics where the applications include computer peripherals, servos and robotics, pumps and fans, paper and textile mills, rolling mills, wind generation system, variable sneed heat pump and air-conditioning, transportation system, ship propulsion etc.

The importance of power electronics is being increasingly visible now-a-days in the energy saving of electrical apparatus by more efficient use of electricity. The energy consumption in the world is increasing by leaps and bounds to improve the human living standard, particularly in industrialized countries. The major amount of this energy comes by burning fossil fuels, such as coal, natural gas and oil which create global warming effect besides urban pollution problem. The energy efficiency improvement of electrical apparatus with the help of power electronics not only reduce electricity consumption but the corresponding reduced power generation indirectly helps reduction of environmental pollution problem. It has been estimated that roughly 15% of electricity consumption can be saved by extensive application of power electronics. Table 1.2 list various applications of power-electronics. However, this list is not exhaustive.

Table 1.2 Applications of power-electronics in various sectors

Sectors	*Applications*
1. Home Appliances	Refrigerators, sewing machines, photography, airconditioning, food warming trays, washing machines, lighting, dryers, vaccum cleaners, electric blankets, grinders and mixers, cooking appliances
2. Games and entertainment	Games and toys, televisions, movie projectors
3. Commercial	Advertising, battery chargers, blenders, computers, electric fans, electronic ballasts, hand power tools, photocopiers, vending machines, light dimmers
4. Aerospace	Aircraft power systems, space vehicle power systems, satellite power systems
5. Automotive	Alarms and security systems, electric vehicles, audio and Rf amplifiers, regulators
6. Industrial	Blowers, boilers, chemical processing equipment, contactor and circuit breakers, conveyors, cranes and hoists, dryers, electric furnaces and ovens, electric, vehicles, electromagnets, electronic ignitions, elevators, flashers, gas-turbine starters, generator exciters, induction heating, linear induction motion control, machine tools, mining power equipments, motor drives and starters, nuclear reactor control, oil-well drilling equipment, paper mill machinery, power-supplies, printing press machinery, pumps and compressors, servo systems, steel mill instrumentation, temperature controls ultrasonic generators, uninterruptible power supplies (UPS), welding equipment
7. Medical	Fitness machines, laser power supplies, medical instrumentation
8. Security systems	Alarms and security systems, radar/sonar
9. Telecommunications	Uninterruptible power supplies (UPS), solar power supplies, VLF transmitters, wireless communication power supplies
10. Transportation	Magnetic levitation, trains and locomotives, motor drives, trolly buses, subways
11. Utility systems	VAR compensators, power factor correction, static circuit breakers, supplementary energy systems (solar, wind)

1.7 COMPUTER SIMULATION OF POWER ELECTRONIC CIRCUITS

Computer simulation plays a vital role in the analysis and design of power electronic circuits and systems. When a new converter circuit is to be developed, or a control strategy of a converter or drive system is formulated, it is often convenient to study the system performance by simulation before building the breadboard or prototype. The simulation not only validates the system's operation but also permits optimization of the system's performance by iteration of its parameters. Besides control and circuit parameters, the plant parameter variation effect can be studied. Thus, valuable time is saved in the design and development of a product, and the failure of components of poorly designed systems can be avoided.

The simulation techniques reduces the time to market the product. Simulation softwares are used to calculate the circuit waveforms, the steady state and dynamic performance of the systems, and the ratings of the various components used in the circuit. The tools used for simulation are generally classified either as circuit-oriented simulators or equation-solvers.

In circuit oriented simulator packages, the user needs to supply the circuit topology and the component values. The simulator internally generates the circuit equations that are completely transparent to the user. The user has the flexibility of selecting the details of the component models. With circuit oriented simulators, the initial set up time is small and it is easy to make changes in the circuit topology and control. Many built-in models for the components and the controllers are usually available. The focus is mainly on the circuit rather than the mathematical modelling. Circuit oriented simulators have a small control over the simulation process which results in maximum simulation time and may suffer from oscillation problems.

In equation solver packages, the user needs to supply the differential and algebraic equations which describes the circuits and the systems. These packages has the complete control over the simulation process which results in less simulation time.

Circuit-oriented simulators such as SPICE, EMTP, SABER, KREAN, etc. are available. The abbreviation SPICE stands for Simulation Program with Integrated Circuit Emphasis. It can handle nonlinearities and provides an automatic control on the time-step of integration. Many commercial versions of SPICE that operate on personal computers under several popular operating systems are available. Commercial versions can be divided into two types, i.e. mainframe versions and PC-based versions.

The mainframe versions are:

(i) PSpice (Microsim)
(ii) HSPICE (meta-software), which is designed for integrated circuit design with special device models.
(iii) RAD-SPICE (Metal Software), which simulates circuits subjected to ionizing radiation.
(iv) Precise (Electronic Engineering Software)

(v) Cadence-SPICE (Cadence Design)
(vi) Accusim (Mentor Graphics)
(vii) SPICE-Plus (Valid logic)

The PC-Versions are:

PSpice (Microsim)
AllSpice (Acotech)
IS-SPICE (Intusoft)
Z-SPICE (Z-Tech)
SPICE-plus (Analog Design Tools)
DSPICE (Daisy Systems)

In PSpice, many features are available which makes it a multilevel simulator. The controllers can be represented by their input-output behaviour-model. The input data can also be entered by drawing the circuit schematic. Free-evaluation (class-room) version of PSPICE is available. This evaluation version is very powerful for power electronic circuit simulations. PSPICE examples are provided on the on-line centre (OLC) of the book.

If we use an equation-solver, then we have to write differential and algebraic equations which describes various circuit states and the logical expressions within the controller. Then simultaneously solve these equations as a function of time. MATLAB is a very convenient equation solver. It is a software package for high-performance numerical computation and visualization. It provides an interactive environment with hundreds of built-in functions for technical computation, graphics and animation. The name MATLAB stands for MATrix LABoratory. SIMULINK is a powerful graphical user-interface to MATLAB which allows dynamic systems to be described in an easy block diagram form. A library of function blocks, such as sources, sinks, discrete, linear, nonlinear and connections can be used in the simulation. The power semiconductor device is normally simulated by the element switch, which is an element in nonlinear function block.

REVIEW QUESTIONS

1.1 Explain briefly the concept of power electronics.
1.2 State essential parts of power electronic systems.
1.3 With the help of neat block diagram, explain the functional elements of power electronic system.
1.4 What are the functions of power modulator?
1.5 Briefly explain the sources employed in power electronic systems.
1.6 State and explain the functions of various converters.
1.7 List all the motors employed in power-electronic system.
1.8 Discuss the basis of classifying power semiconductor devices into various categories.
1.9 List alteast two applications of power electronic converters.
1.10 Mention atleast two applications of power electronics in various energy activity sectors.

1.11 List the semiconductor devices which can withstand both unipolar as well as bipolar voltages.

1.12 What is the basic difference between cycloconverter and ac voltage controller?

1.13 List the devices which can withstand bidirectional current.

1.14 Write the basic difference between the equation solver packages and circuit oriented simulator packages?

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Chapter **2**

Thyristor: Principles and Characteristics

LEARNING OBJECTIVES:

- To become familiar with the SCR.
- To define a thrysitor and its family.
- To study the *V-I* and dc gate-current control characteristics of an SCR.
- To explain the two-transistor analogy of silicon controlled rectifier.
- To explain the term commutation and also the different methods of commutation.
- To consider the turn-on and turn-off mechanisms of SCR.
- To establish the thyristor ratings.

2.1 INTRODUCTION

Thyristor is a general name given to a family of power semiconductor switching devices, all of which are characterised by a bistable switching action depending upon the PNPN regenerative feedback. The thyristor has four or more layers and three or more junctions. The SCR is the most widely used and important member of the thyristor family. This device has revolutionised the art of solid state power control. The SCR is almost universally referred to as the *thyristor*.

From the construction point of view, the thyristor (PNPN structure) can be best visualized as consisting of two transistors (a PNP and an NPN interconnected-to-form a regenerative feedback pair, as shown in Section 2.4). The name thyristor is derived by a combination of the capital letters from thyratron and transistor. Thus, a thyristor is a solid state device like a transistor and has characteristics similar to that of a thyratron tube.

In this chapter, we will study the operation, characteristics, ratings and commutation methods of thyristors.

2.2 PRINCIPLE OF OPERATION OF SCR

The structure and symbol of the thyristor (SCR) are shown in Fig. 2.1. It is a four layered *PNPN* switching device, having three junctions J_1, J_2 and J_3. It has three external terminals, namely, the anode (A), cathode (K) and gate (G). The anode and cathode are connected to the main power circuit. The gate terminal carries a low level gate current in the direction gate to cathode. Normally, the gate terminal is provided at the P layer near the cathode. This is known as cathode gate.

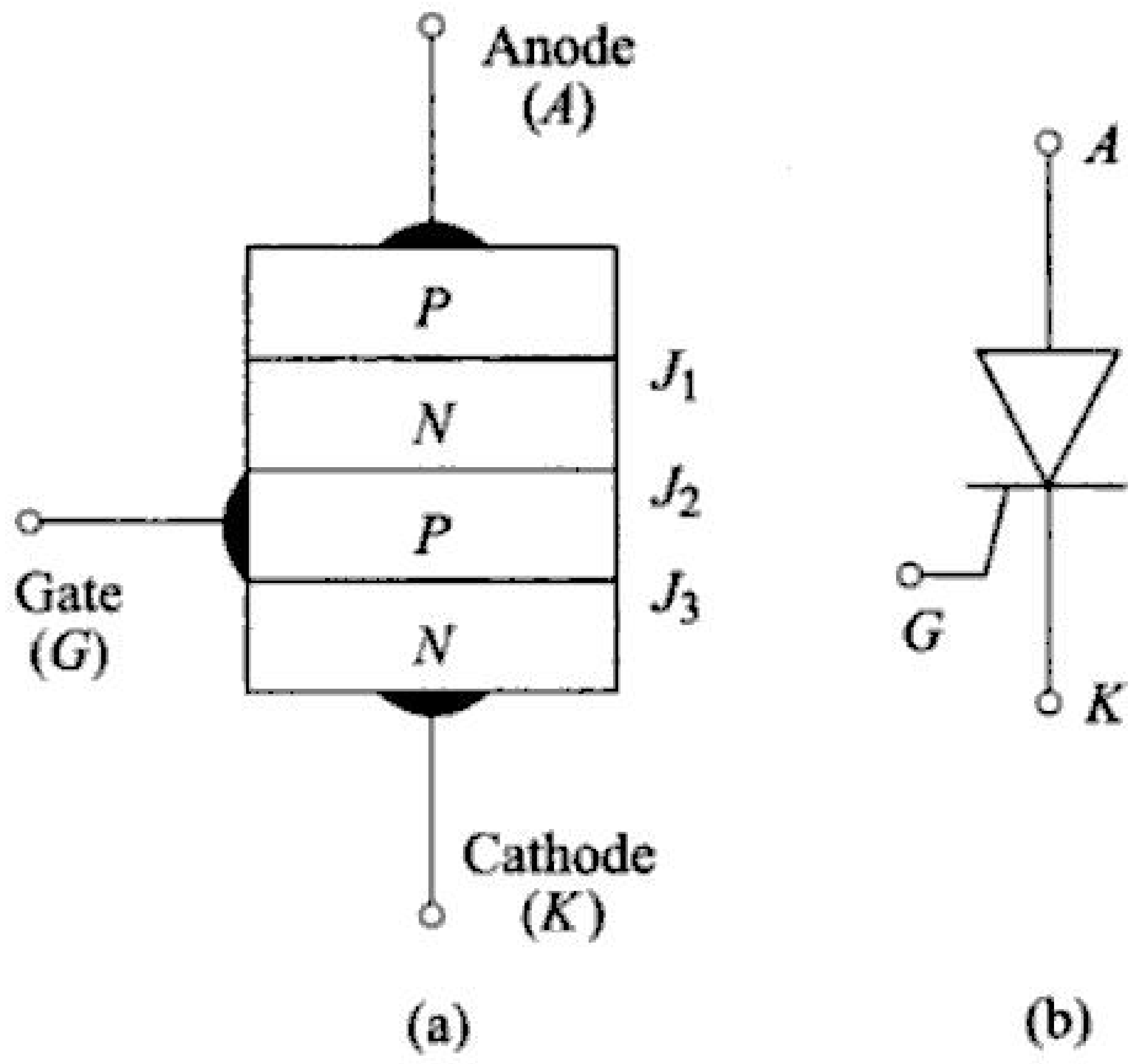


Fig. 2.1 ***(a)*** *Structure* ***(b)*** *symbol*

When the end P layer is made positive with respect to the end N layer , the two outer junctions, J_1 and J_3 are forward biased but the middle junction J_2 becomes reverse biased. Thus the junction J_2 because of the presence of depletion layer, does not allow any current to flow through the device. Only leakage current, negligibly small in magnitude, flows through the device due to the drift of the mobile charges. This current is insufficient to make the device conduct. The depletion layer, mostly of immobile charges do not constitute any flow of current. In other words, the SCR under the forward biased condition does not conduct. This is called as the *forward blocking state* or off-state of the device.

When the end n layer is made positive with respect to end p layer, the middle junction J_2 becomes forward biased, whereas the two outer junctions, J_1 and J_3 become reverse biased. The junctions J_1 and J_3 do not allow any current to flow through the device. Only a very small amount of leakage current may flow because of the drift of the charges. The leakage current is again insufficient to make the device conduct. This is known as the *reverse blocking state* or off-state of the device.

The width of the depletion layer at the junction J_2 decreases with the increase in anode to cathode voltage (since the width is inversely proportional to voltage). If the voltage between the anode and cathode is kept on increasing, a stage comes (corresponding to forward break-over voltage) when the depletion layer at J_2 vanishes. The reverse biased junction J_2 will breakdown due to the large voltage gradient across its depletion layer. This phenomenon is known as the *Avalanche breakdown*. Since the other junctions, J_1 and J_3 are already forward biased, there will be a free carrier movement across all the three junctions resulting in a large amount of current flowing through the device from anode to cathode. Due to the flow of this forward current, the device starts conducting and it is then said to be in the *conducting state* or on state.

2.3 STATIC ANODE-CATHODE CHARACTERISTICS OF SCR

An elementary circuit diagram for obtaining static *V–I* characteristics of a thyristor is shown in Fig. 2.2. Here, the anode and cathode are connected to the main source through a load. The gate and cathode are fed from another source E_g.

The static *V–I* characteristic of an SCR is shown in Fig. 2.3. Here, V_a is the anode–cathode voltage and I_a is the anode current. The thyristor *V-I* characteristics is divided into three regions of operation. These three regions of operation are described below.

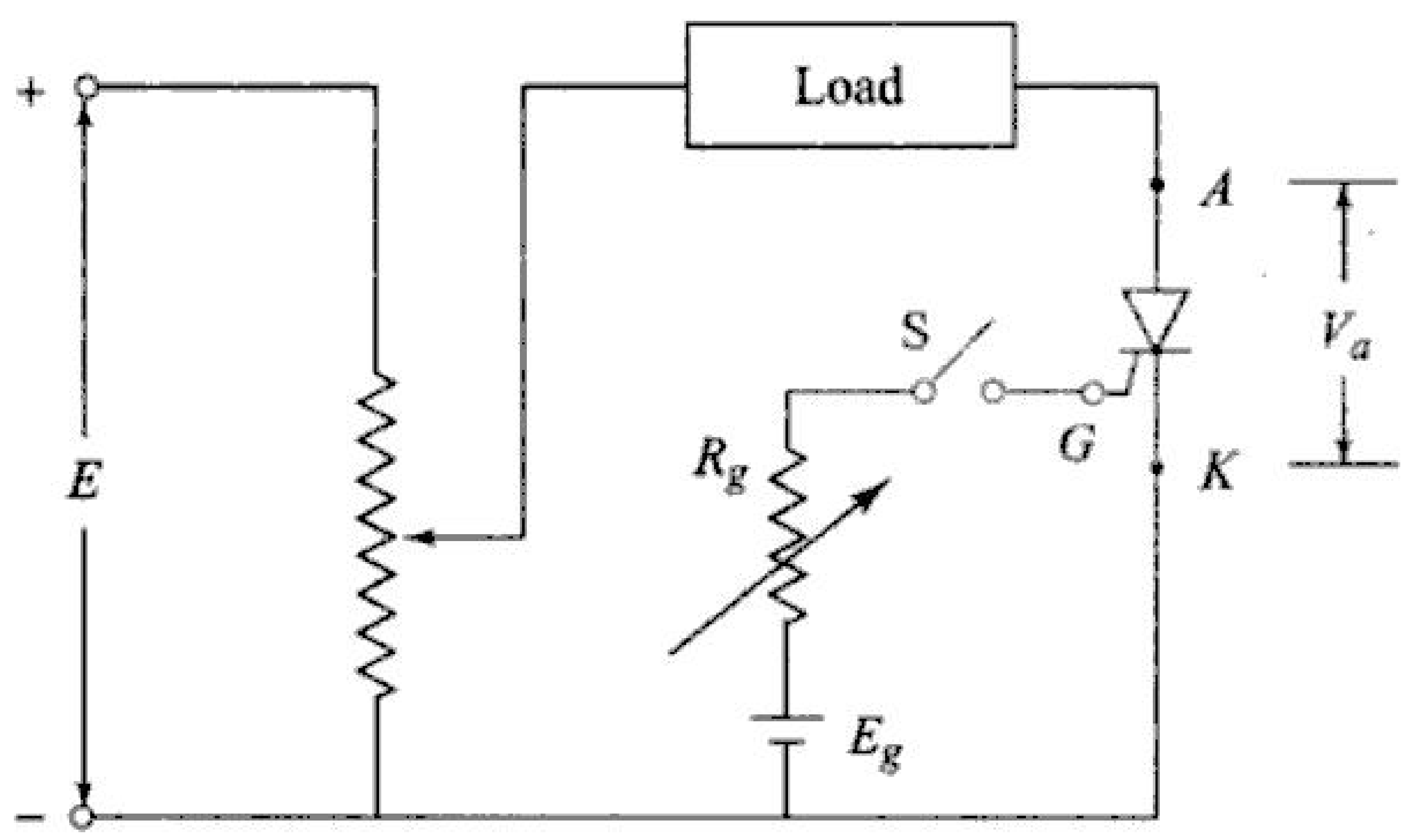
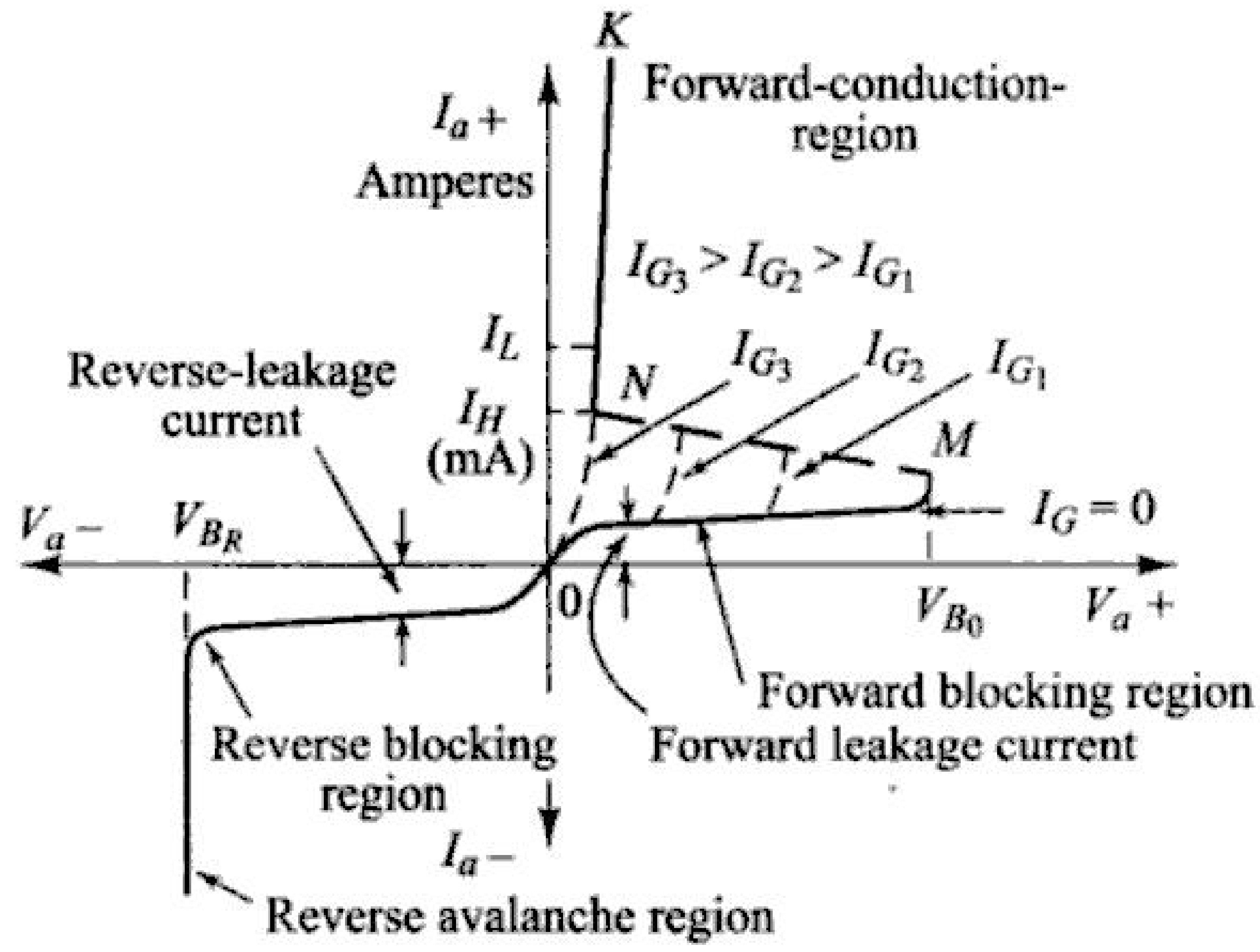


Fig. 2.2 *Elementary circuit*

1. Reverse Blocking Region When the cathode is made positive with respect to anode with the switch *s* open (Fig. 2.2), the thyristor becomes reverse biased. In Fig. 2.3, *OP* is the reverse blocking region. In this region, the thyristor exhibits a blocking characteristic similar to that of a diode. In this reverse biased condition, the outer junction J_1 and J_3 are reverse biased and the middle junction J_2 is forward biased. Therefore, only a small leakage current (in mA) flows. If the reverse voltage is increased, then at a critical breakdown level called reverse breakdown voltage V_{BR}, an avalanche will occur at J_1 and J_3 increasing the current sharply. If this current is not limited to a safe value, power dissipation will increase to a dangerous level that may destroy the device. Region *PQ* is the reverse-avalanche region. If the reverse voltage applied across the device is below this critical value, the device will behave as a high-impedance device (i.e., essentially open) in the reverse direction.



V_{B_0} = Forward breakover voltage; V_{B_R} = Reverse breakover voltage; I_G = Gate current; I_L = Latching current; and I_H = Holding current

Fig. 2.3 *V-I characteristics*

The inner two regions of the SCR are lightly doped compared to the outer layers. Hence, the thickness of the J_2 depletion layer during the forward biased conditions will be greater than the total thickness of the two depletion layers at J_1 and J_3 when the device is reverse biased. Therefore, the forward break–over voltage V_{BO} is generally higher than the reverse break–over voltage V_{BR}.

2. Forward Blocking Region In this region, the anode is made positive with respect to the cathode and therefore, junctions J_1 and J_3 are forward biased while the junction J_2 remains reverse biased. Hence, the anode current is a small forward leakage current. The region *OM* of the *V–I* characteristic is known as the forward blocking region when the device does not conduct.

3. Forward Conduction Region When the anode to cathode forward voltage is increased with the gate circuit kept open, avalanche breakdown occurs at the junction J_2 at a critical forward break-over voltage (V_{BO}), and the SCR switches into a low impedance condition (high conduction mode). In Fig. 2.3, the forward breakover voltage is corresponding to the point *M*, when the device latches on to the conducting state. The region *MN* of the characteristic shows that as soon as the device latches on to its *ON* state, the voltage across the device drops from say, several hundred Volts to 1–2 Volt, depending on the rating of the SCR, and suddenly a very large amount of current starts flowing through the device. The part *NK* of the characteristic is called as the forward conduction state. In this high conduction mode, the anode current is determined essentially by the external load impedance. Therefore when the thyristor conducts forward current, it can be regarded as a closed switch.

through the windows in the mask. The finished *PNPN* wafers are then diced into individual pellets. Triacs and other more complex structures are fabricated using similar techniques. In the manufacture of some higher current SCR's, where only a limited number of pellets, sometimes only one, can be obtained from each wafer, the original *PNP* wafers are pelletised before adding the final *N*-region. Where this is the case, precision alloying techniques are used after pelletising to fuse a gold-antimony preform into each *PNP* pellet, thus forming the required *PNPN* structures.

2.5.1 Planar-Diffused (All Diffused)

The cross-sectional view of a typical all diffused SCR structure is shown in Fig. 2.5. As shown, the SCR consists of a four-layer pellet of *P* and *N*-type semiconductor materials. Silicon is used as the intrinsic semiconductor doped with proper impurities. The junctions are diffused type. A planar structure therefore describes a type of pellet where all the *PN* junctions come out to a single surface on the silicon pellet.

The principle advantage of planar construction is that junction information always takes place underneath a thin layer of silicon dioxide grown over the silicon wafer, before diffusion commences, which prevents contamination of silicon surfaces. As a result, planar, pellets are to a large degree protected from the outside environment. Disadvantages of planar construction are that more silicon is required per ampere of current carrying capability, and that more wafer processing steps are needed. Planar structures are best-suited, therefore, to low current devices where many pellets can be obtained from a single wafer, and to complex structures where photoresist techniques are required for geometry control.

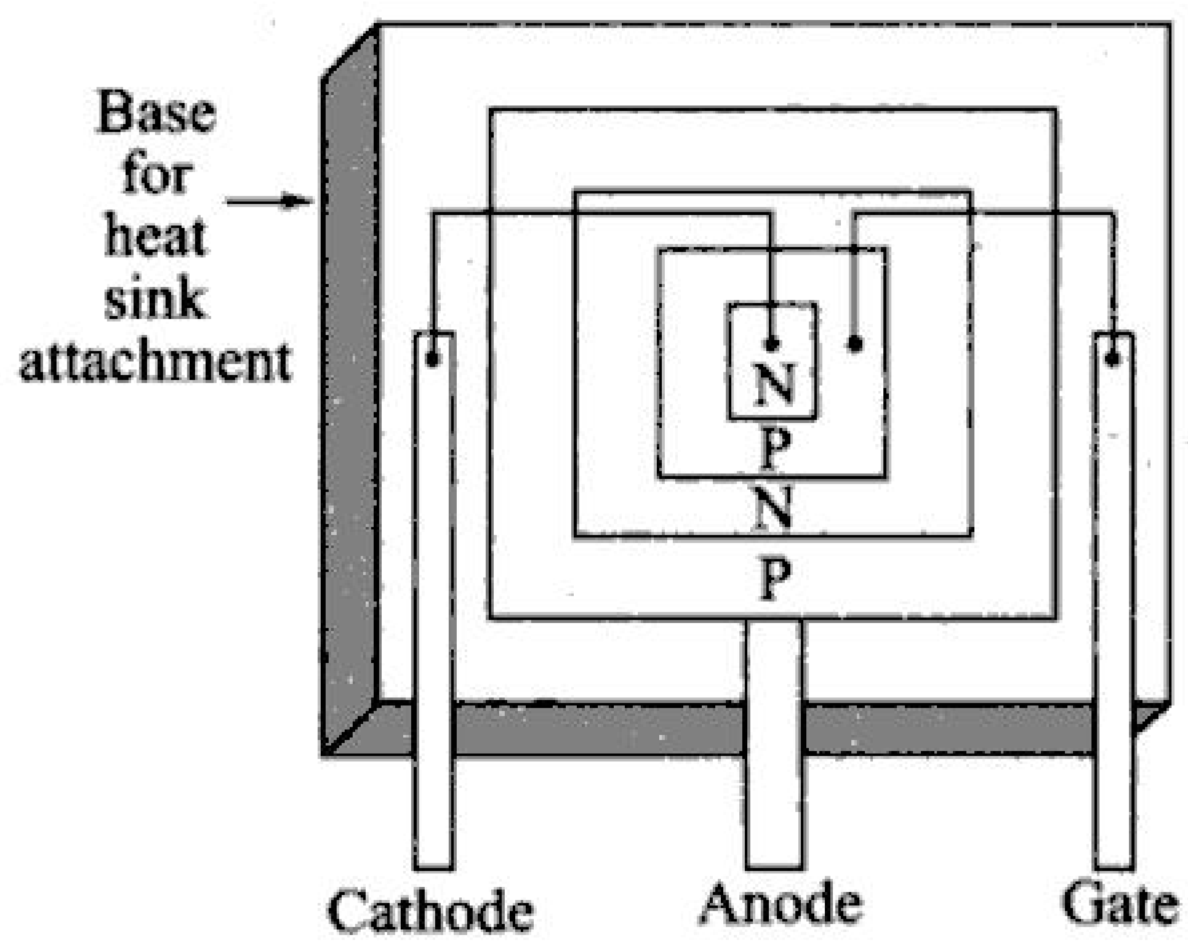


Fig. 2.5 *Cross-sectional view of planar-type SCR*

2.5.2 Alloy-Diffused [Mesa Type]

The cross-sectional view of a typical Mesa type construction is shown in Fig. 2.6. Here, the inner junction J_2 is obtained by diffusion, and then the outer two layers are alloyed to it. Since the *PNPN* pellet is required to handle large-currents, it is properly braced with tungsten or molybdenum plates to provide greater mechanical strength. One of these plates is hard soldered to a copper or an aluminum stud, that is threaded for attachment to a heat-sink. This provides an efficient thermal path for conducting the internal losses to the surrounding medium. The use of hard solder between the pellet and backup plates minimises thermal fatigue when the SCRs are subjected to temperature induced stresses. The gate or control electrode consists of a small aluminium wire that is connected to the silicon pellet. This is ohmic contact and not a rectifying junction. Control of the device is accomplished by applying a signal to the top *PN* junction; that is, between the gate and cathode leads.

When a larger cooling arrangement is required for high-power SCRs, the *press pack* or *hockey puck* construction is used, which provides for double-sided air or water cooling.

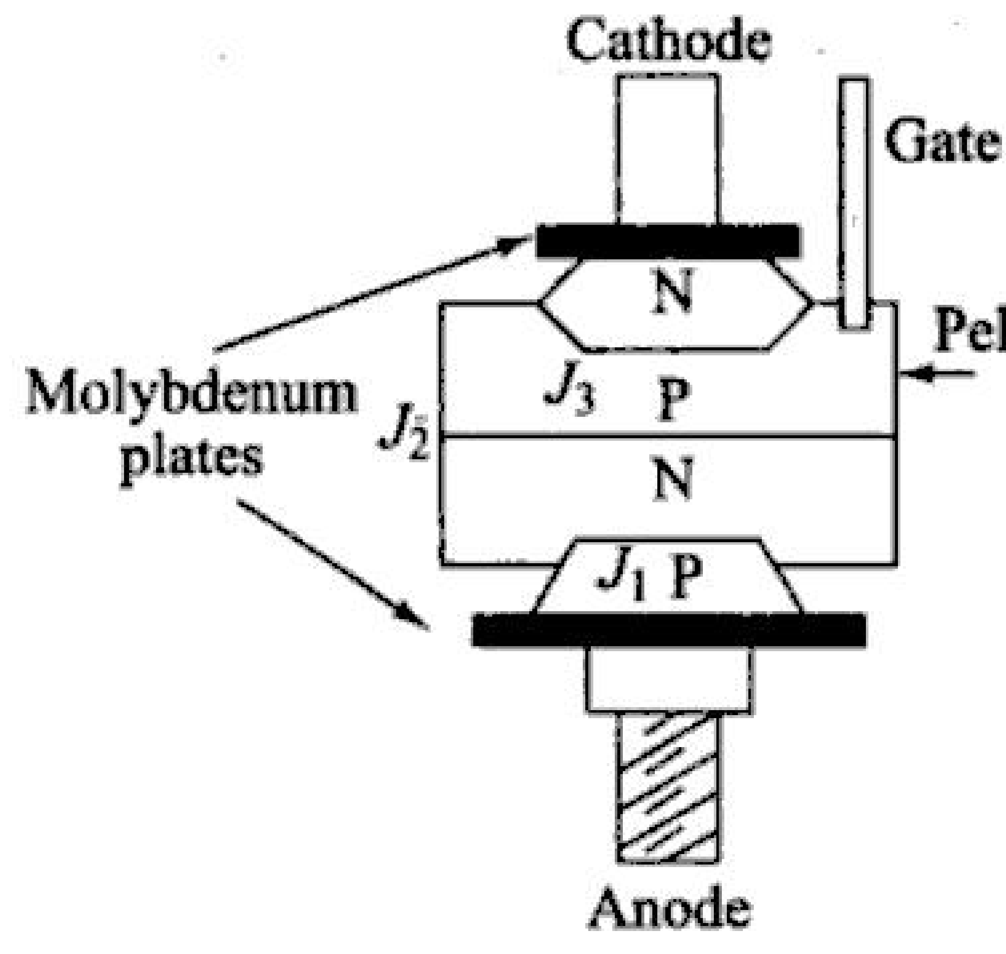


Fig. 2.6 *Cross-sectional view of alloy-diffused SCR (Mesa type)*

2.6 GATE CHARACTERISTICS OF SCR

In a thyristor, the gate is connected to the cathode through a *PN* junction and resembles a diode. Therefore, the *V-I* characteristic of a gate is similar to a diode but varies considerably in units. The circuit which supplies firing signals to the gate must be designed:

(1) to accommodate these variations,
(2) not to exceed the maximum voltage, and power capabilities of the gate,
(3) to prevent triggering from false signals or noise, and
(4) to assure desired triggering.

The design specification pertaining to gate characteristics are usually provided by the manufacturers. Figure 2.7 shows the gate characteristics of a typical SCR. Here, positive gate to cathode voltage V_g and positive gate to cathode current I_g represent d.c. values.

Applying gate drive increases the minority carrier density in the inner *P* layer and thereby facilitate the reverse breakdown of the junction J_2. There are maximum and minimum limits for gate voltage and gate current to prevent the permanent destruction of junction J_3 and to provide reliable triggering. Similarly, there is also a limit on the maximum instantaneous gate power dissipation ($P_{gmax} = V_g I_g$). The permissible maximum value of P_{gmax} depends on the type of gate drive. The gate signal can be d.c. or a.c. or a sequence of high frequency pulses. With pulse firing, a larger amount of instantaneous gate power-dissipation can be tolerated if the average-value of P_g is within the permissible limits. Hence, the gate can be driven harder (greater V_g and I_g) when pulse firing is used. This provides for reliable and faster turn-on of the device.

All possible safe operating points for the gate are bounded by the low and high current limits for the *V-I* characteristics, maximum gate voltage, and the hyperbola representing maximum gate power. Within these boundaries there are three regions of importance.

(1) The first region *OA* lies near the origin (shown hatched) and is defined by the maximum gate voltage that will not trigger any device. This value is obtained at the maximum rated junction temperature (usually 125°C). The gate must be operated in this region whenever forward bias is applied across the thyristor and triggering is not necessary. In other words, this region sets a limit on the maximum false signals that can be tolerated in the gate-firing circuit.

(2) The second region is further defined by the minimum value of gate-voltage and current required to trigger all devices at the minimum rated junction temperature. This region contains the actual minimum firing points of all devices. In a sense, it is a forbidden region for the firing circuit because a signal in this region may not always fire all devices or never fire any at all. In Fig. 2.7, *OL* and *OV* are the minimum gate-voltage and gate current limits respectively.

(3) The third region is the largest and shows the limits on the gate-signal for reliable firing. Ordinarily, a signal in the lower left part of this region is adequate for firing. For applications, where fast turn-on is required, a 'hard' firing signal in the upper right part of the region may be needed.

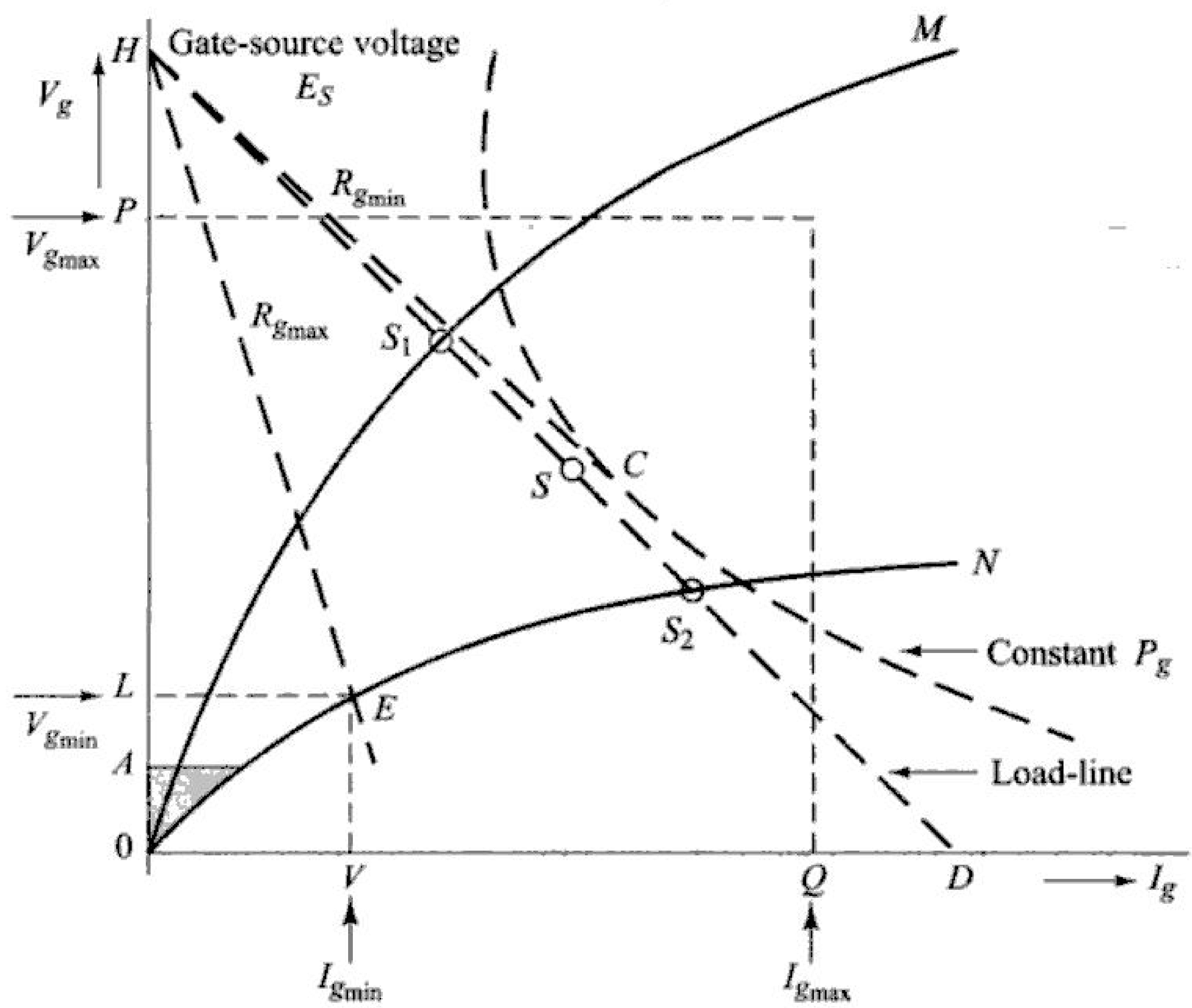


Fig. 2.7 *Gate characteristics*

In Fig. 2.7 curves *ON* and *OM* corresponds to the possible spread of the characteristic for SCRs of the same rating. For best results, the operating point *S*, which may change from S_1 to S_2, must be as close as possible to the permissible

P_g curve and must be contained within the maximum and minimum limits of gate voltage and gate current. This provides the necessary hard drive for the device. For selecting the operating point, usually a load line of the gate source voltage $E_s = OH$ is drawn as HD. The gradient of the load line HD (= OH/OD) will give the required gate source resistance R_g. The maximum value of this series resistance is given by the line HE, where E is the point of intersection of lines indicating the minimum gate voltage and gate current. The minimum value of gate source series resistance is obtained by drawing a line HC tangential to P_g curve.

A thyristor may be considered to be a charged controlled device. Thus, higher the magnitude of gate current pulse, lesser is the time needed to inject the required charge for turning on the thyristor. Therefore the SCR turn-on time can be reduced by using gate current of higher magnitude. It should be ensured that pulse width is sufficient to allow the anode current to exceed the latching current. In practice, the gate pulse width is usually taken as equal to or greater than SCR turn-on time, t_{on}. If T is the pulse width as shown in Fig. 2.8, then

$$T \geq t_{on}$$

With pulse firing, if the frequency of firing f is known, the peak instantaneous gate power dissipation $P_{g\max}$ can be obtained as

$$P_{g\max} = V_g I_g = \frac{P_{g_{av}}}{fT} \qquad (2.10)$$

where $\quad f = \dfrac{1}{T_1}$ = frequency of firing or pulse repetition rate in Hz

and $\quad T$ = pulse width in second

A duty cycle is defined as the ratio of pulse-on period to the periodic time of pulse. In the Fig. 2.8 pulse-on period is T and the periodic time is T_1. Therefore, duty-cycle is given by

$$\delta = \frac{T}{T_1} = fT \qquad (2.11)$$

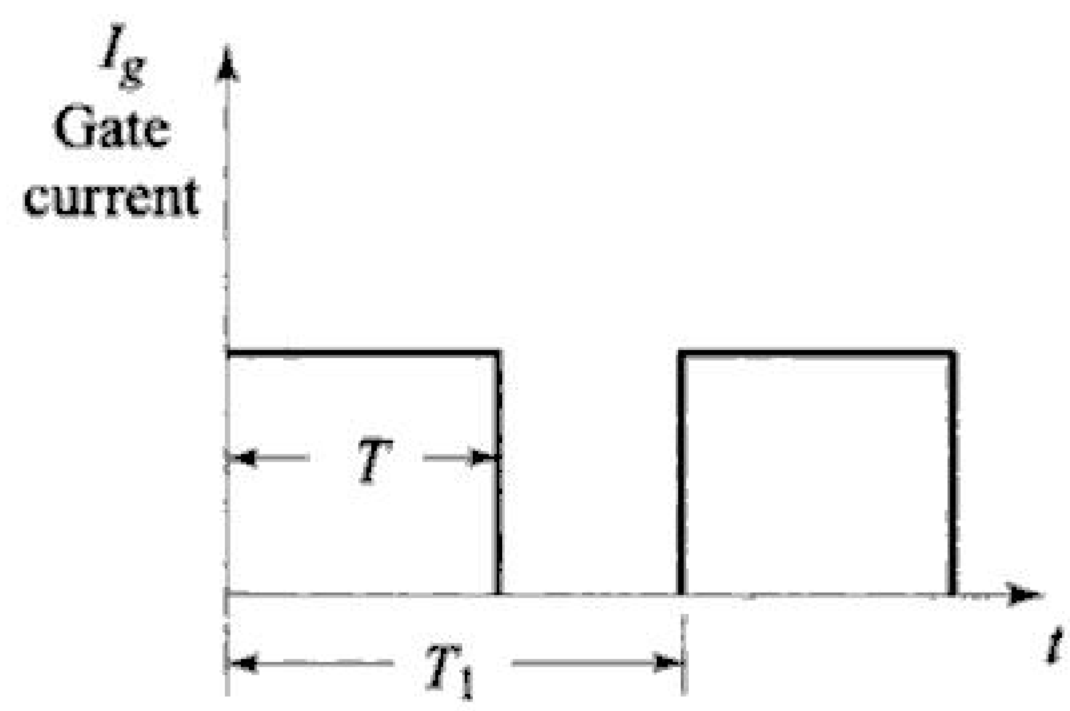


Fig. 2.8 *Pulse gating*

From Eq. (2.10)

$$\frac{P_{g_{av}}}{\delta} \leq P_{g\max} \qquad (2.12)$$

2.6.1 Gate Circuit Parameters

The gate cathode circuit with different circuit parameters is shown in Fig. 2.9. A series resistance R_g should be placed in series with the gate-source voltage E_g, to limit the magnitude of gate voltage and gate-current.

The shunt resistor R_{gc} is introduced to bypass the thermally generated leakage current across junction J_2 when the device is in the blocking state, in order to improve the thermal-stability of the device. This shunt resistance in turn will increase the required gate current and also the device holding and latching current levels.

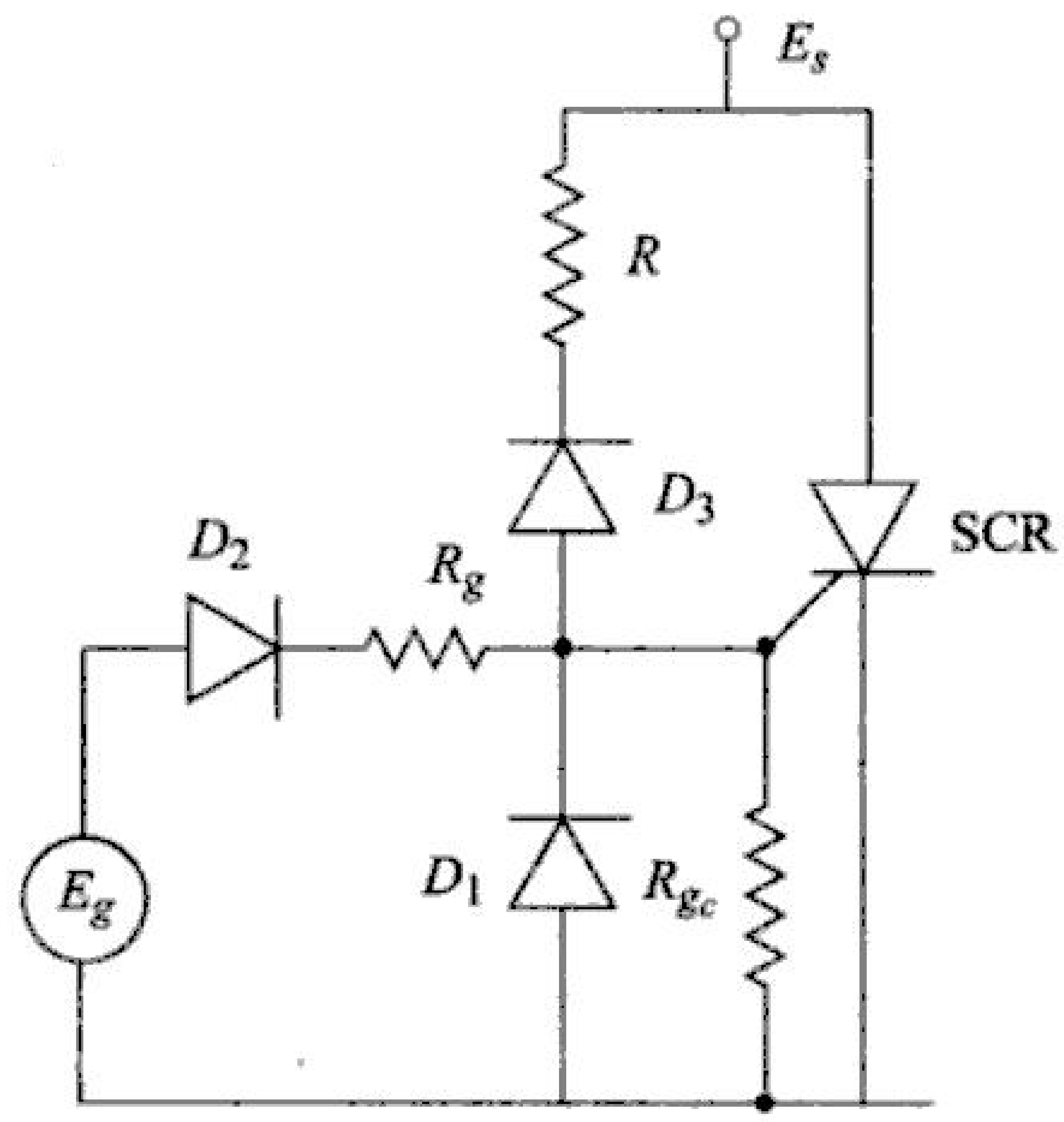


Fig. 2.9 *Gate circuit*

Diode D_1 applies a negative voltage between the gate and the cathode when a reverse voltage is applied across the device. This negative gate-voltage reduces the reverse blocking current and improves the turn-off mechanism. This diode D_1 also serves to limit the reverse voltage applied between the cathode and the gate, if the gate, source voltage E_g is alternating. The negative gate current flows through the device while the SCR is ON because the diode D_1 will then be reverse biased. This will increase the dissipation of gate power. A series diode D_2 in the circuit will prevent the negative source current. Another diode D_3 is connected as shown in the figure to block the positive gate current coming from the supply when the device is forward biased.

A shunt capacitor C_s may be connected across gate to cathode to improve the *dv/dt* capability. However, pulse firing results in a larger portion of the gate drive being bypassed by the capacitor which will increase the delay time and consequently the *di/dt* rating of the device is also lowered. This shunt capacitor also poses one more problem. When the device is turned ON, the gate acts as a voltage source and charges the capacitor. This charge can provide enough gate current after the anode current has stopped thereby increasing the turn-off time of the SCR and commutation may fail.

If an inductance is connected across gate to cathode, the negative gate current is maintained by the inductance even after the anode-current has stopped, and this will facilitate faster turn-off. However, when pulse firing is used for gating the device, the negative gate current that continues to flow out of the gate can possibly turn-off the thyristor.

Thus, depending upon the specific requirements, gate circuit parameters are chosen. The use of a negative voltage bias between the gate and cathode is generally recommended. This will increase the forward breakover voltage and d*v*/d*t* withstanding capability. Similarly, the reverse leakage current will also be reduced by the negative gate bias. The only drawback is that a greater gate source voltage E_g is required to overcome this bias and turn-on the SCR.

SOLVED EXAMPLES

Example 2.4 An SCR has a V_g–I_g characteristics given as $V_g = 1.5 + 8\ I_g$. In a certain application, the gate voltage consists of rectangular pulses of 12 V and of duration 50 μs with duty cycle 0.2.

(a) Find the value of R_g series resistor in gate circuit to limit the peak power dissipation in the gate to 5 watts.

(b) Calculate average power dissipation in the gate.

Solution: During conduction,

$$V_{gs} = R_g I_g + V_g = R_g I_g + 1.5 + 8\ I_g$$

$$12 = (R_g + 8)\ I_g + 1.5 \qquad \text{(i)}$$

Peak power loss $= V_g I_g = 5 \quad \therefore \quad 5 = (1.5 + 8I_g)\ I_g$

$\therefore \quad 8\ I_g^2 + 1.5\ I_g - 5 = 0 \qquad \therefore \quad I_g = \dfrac{-1.5 \pm \sqrt{(1.5)^2 - 160}}{16} = 0.7$ A

Substitute I_g in Eq. (i), $\quad \therefore \quad I_2 = (R_g + 8)\ 0.7 + 1.5,\ R_g = 7\ \Omega$

Now, Average, power loss = peak power loss × duty cycle = 5 × 0.2 = 1W

Example 2.5 If the $V_g - I_g$ characteristics of an SCR is assumed to be a straight line passing through the origin with a gradient of 3×10^3, calculate the required gate source resistance. Given E_{gs} = 10V and allowable $P_g = 0.012\Omega$.

Solution: The allowable P_g = 0.012 watt, $\quad \therefore \quad V_g I_g = 0.012 \qquad$ (i)

Also, gradient $= \dfrac{V_g}{I_g} = 3 \times 10^3, \qquad \therefore \quad V_g = 3 \times 10^3\ I_g$

Substituting V_g in Eq (i),

$(3 \times 10^3 \times I_g \times I_g) = 0.012,\ I_g = 2$ mA. $\qquad \therefore \quad V_g = 3 \times 10^3 \times 2 \times 10^{-3} = 6$ V.

Example 2.6 A thyristor has a forward characteristic which may be approximated over its normal working range to the straight line shown in Fig. E2.6. Calculate the mean power-loss for—

(a) a continues on state current of 23 A.
(b) a half-sine wave of mean value 18 A.
(c) a level current of 39.6 A for one-half cycle.
(d) a level current of 48.5 A for one third cycle.

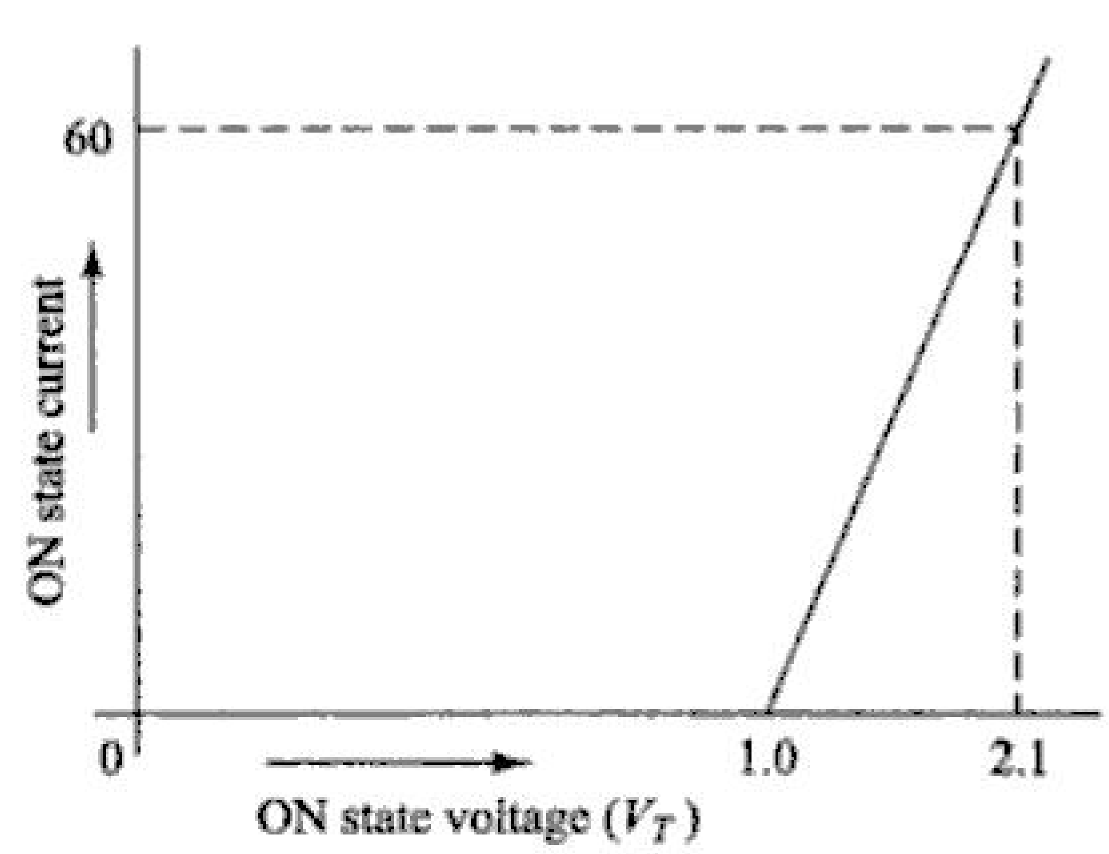


Fig. E2.6

Solution: (a) At a ON state current of 23A, the ON state voltage from Fig. E2.6 is

$$V_T = 1 + \frac{23 \times 1.1}{60} = 1.42 \text{ V}$$

$\therefore$ Power loss $= V_T I_T = 1.42 \times 23 = 32.7$ W

(b) The maximum value of the sine wave = 18 πA

From the figure, at any current I, Voltage $V = 1 + \frac{1.1}{60} I$.

Over one cycle, the total base length is 2π from 0 to π, $I = 18\pi \sin x$, and from π to 2π, $I = 0$.

$$\therefore \quad \text{Mean power} = \frac{1}{2\pi}\int_0^{\pi} V\, I\, dx = \frac{1}{2\pi}\int_0^{\pi} V\left(I + \frac{1.1}{60} 18\pi \sin x\right) 18\pi \sin x\, dx = 32.6 \text{ W}$$

(c) The mean power loss will be half the instantaneous power loss over the half cycle when the current is flowing.

$$\therefore \quad \text{Mean power} = \left[39.6\left(1 + \frac{1.1}{60} 39.6\right)\right]\Big/2 = 34.2 \text{ W}$$

(d) Now, the mean power loss for a level current of 48.5 A for one-third cycle is given by

$$\text{Mean power} = \left[48.5\left(1 + \frac{1.1}{60} 48.5\right)\right]\Big/3 = 30.5 \text{ W.}$$

Example 2.7 Compute the peak inverse voltage of thyristor connected in the three phase, six pulse bridge circuit having input voltage of 415 V. Voltage safely factor is 2.1.

Solution: We have the relation,

$$PIV = \sqrt{2} \times V_{in} \times V_f = \sqrt{2} \times 415 \times 2.1 = 1232.49 \text{ V.}$$

Example 2.8 For an SCR, the gate cathode characteristic is given by a straight line with a gradient of 16 volts per amp passing through the origin, the maximum turn-on time is 4 μs and the minimum gate current required to obtain this quick turn-on is 500 mA. If the gate source voltage is 15 V,

(a) Calculate the resistance to be connected in series with the SCR gate.
(b) Compute the gate power dissipation, given that the pulse width is equal to the turn-on time and that the average gate power dissipation is 0.3 W. Also, compute the maximum triggering frequency that will be possible when pulse firing is used.

Solution: (a) Given : $I_{g_{min}} = 500\text{ mA} = 0.5\text{ A}$, $\frac{V_g}{I_g} = 16\text{V/A}$ $\therefore$ $V_g = 16 \times 0.5 = 8\text{ V}$

From Fig. E1.7,

$$R_S = \frac{E_{gs} - V_g}{I_g} = \frac{(15-8)}{0.5} = R_S = 14\ \Omega$$

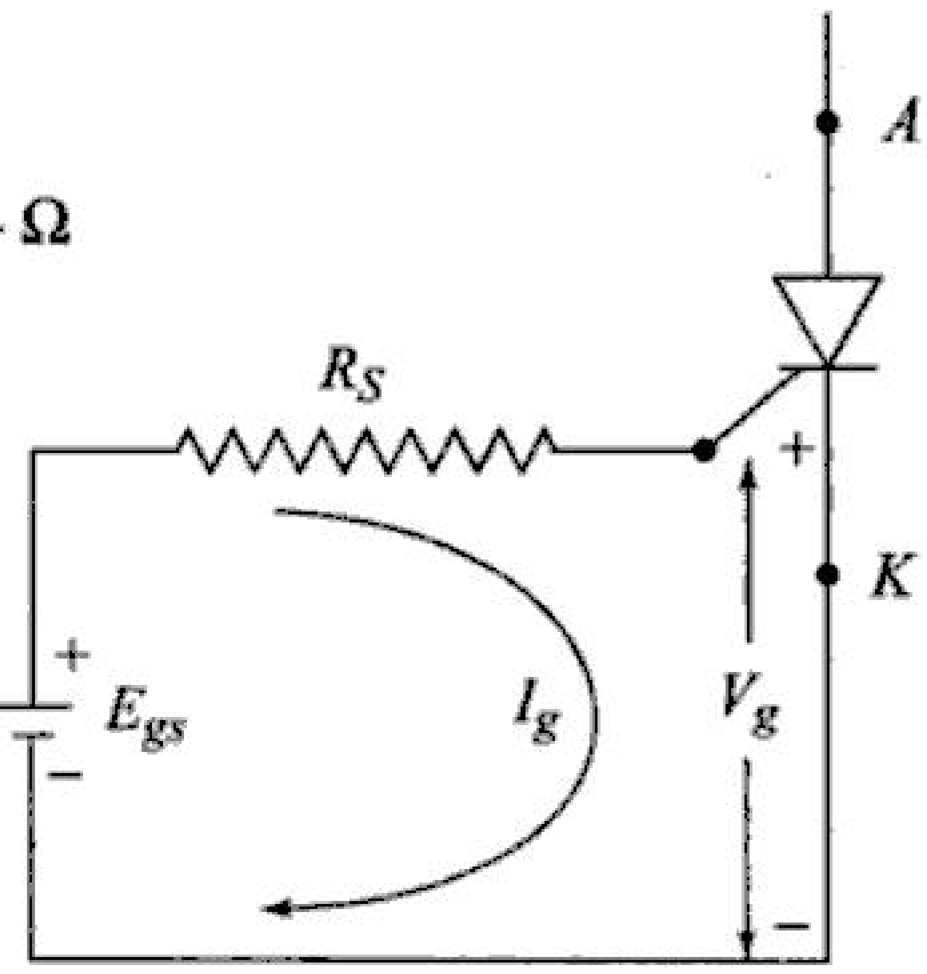


Fig. E2.8

(b)

Power dissipation,

$$P_g = V_g I_g$$

$$= 8 \times 0.5 = 4\text{ W}$$

Now, $$P_{g_{max}} = \frac{P_{g_{av}}}{f \cdot T_{on}} \quad \therefore \quad 4 = \frac{0.3 \times 10^6}{f \times 4}$$

$$f = 18.75\text{ kHz} \quad \therefore \quad F \approx 19\text{ kHz.}$$

2.7 TURN-ON METHODS OF A THYRISTOR

A thyristor can be switched from a nonconducting state to a conducting state in several ways described as follows.

2.7.1 Forward Voltage Triggering

When anode-to-cathode forward voltage is increased with gate circuit open, the reverse biased junction J_2 will have an avalanche breakdown at a voltage called forward breakover voltage V_{BO}. At this voltage, a thyristor changes from OFF state (high voltage with low leakage current) to ON-state characterised by a low voltage across it with large forward current. The forward voltage-drop across the SCR during the ON state is of the order of 1 to 1.5 V and increases slightly with load current.

2.7.2 Thermal Triggering (Temperature Triggering)

Like any other semiconductor, the width of the depletion layer of a thyristor decreases on increasing the junction temperature. Thus, in a thyristor when the voltage applied between the anode and cathode is very near to its breakdown voltage, the device can be triggered by increasing its junction temperature. By increasing the temperature to a certain value (within the specified-limits), a situation comes when the reverse biased junction collapses making the device conduct. This method of triggering the device by heating is known as the thermal triggering process.

2.7.3 Radiation Triggering (Light Triggering)

In this method, as the name suggests, the energy is imparted by radiation. Thyristor is bombarded by energy particles such as neutrons or photons. With the help of

(ii) ***Rise Time (t_r):*** This is the time required for the anode current to rise from 10 to 90% of its final value. It can also be defined as the time required for the forward blocking off-state voltage to fall from 0.9 to 0.1 of its initial value-OP.

This time is inversely proportional to the magnitude of gate current and its build up rate. Thus, t_r can be minimized if high and steep current pulses are applied to the gate. For series *RL* circuit, the rate of rise of anode current is slow, therefore, t_r is more and for the *RC* series circuit, di/dt is high thus t_r is less. During rise-time, turn-on losses are the highest due to high anode voltage *Va* and large anode current I_T occuring together in the thyristor.

(iii) ***Spread-time (t_s):*** The spread time is the time required for the forward blocking voltage to fall from 0.1 to its value to the on-state voltage drop (1 to 1.5 V). After the spread time, anode current attains steady-state values and the voltage drop across SCR is equal to the on-state voltage drop of the order of 1 to 1.5 V.

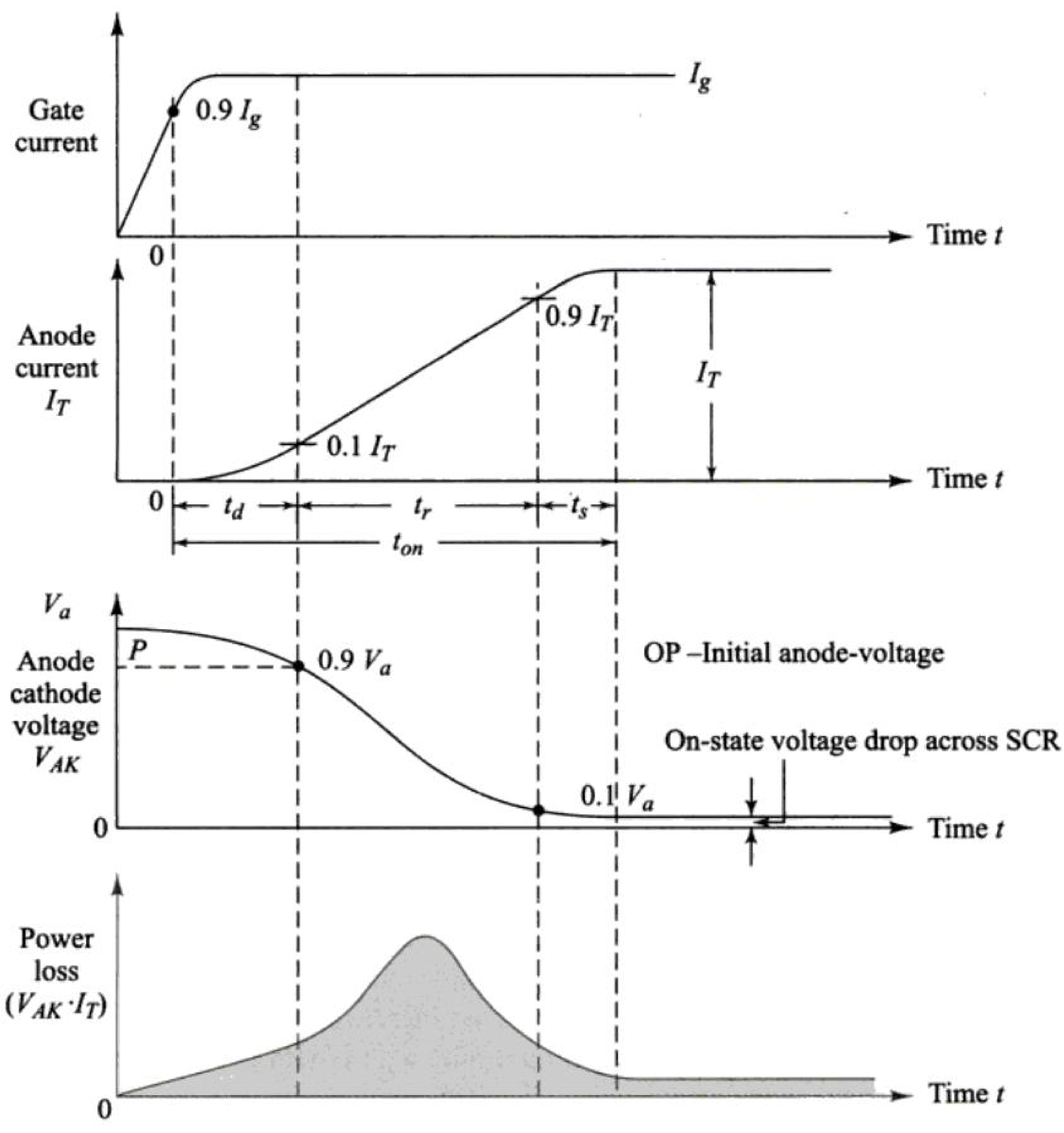


Fig. 2.10 *Waveforms during SCR turn-on*

(iv) ***Turn-on Time*** (t_{on})**:** This is the sum of the delay time, rise-time and spread time. This is typically of the order of 1 to 4 μs, depends upon the anode circuit parameters and the gate signal waveshapes.

The width of the firing pulse should, therefore, be more than 10 μs, preferably in the range of 20 to 100 μs. The amplitude of the gate-pulse should be 3 to 5 times the minimum gate current required to trigger the SCR.

From Fig. 2.10, it is noted that during rise-time, the SCR carries a large forward current and supports an appreciable forward voltage. This may result in high-instantaneous power dissipation creating local internal hot-spots which could destroy the device. It is, therefore, necessary to limit the rate of rise of current. Normally, a small inductor, called *di/dt* inductor is inserted in the anode circuit to limit the *di/dt* of the anode current.

The shadow area under the power-curve in Fig. 2.10 represents the switching loss of the device. This loss may be significant in high-frequency applications.

2.9 TURN-OFF MECHANISM (TURN-OFF CHARACTERISTIC)

Once the SCR starts conducting an appreciable forward current, the gate has no control on it and the device can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current. Process of turn-off is also called as commutation. Various methods used for turning off thyristors will be discussed in Section 2.10. However, if a forward voltage is applied immediately after reducing the anode current to zero, it will not block the forward voltage and will start conducting again, although it is not triggered by a gate pulse. It is, therefore, necessary to keep the device reverse biased for a finite period before a forward anode voltage can be reapplied.

The turn-off time of the thyristor is defined as the minimum time interval between the instant at which the anode current becomes zero, and the instant at which the device is capable of blocking the forward voltage. The turn-off time is illustrated by the waveforms shown in Fig. 2.11. The total turn-off time t_{off} is divided into two time intervals the reverse, recovery time t_{rr} and the gate recovery time t_{gr}.

At the instant t_1, the anode forward current becomes zero. During the reverse recovery time, t_1 to t_3, the anode current flows in the reverse direction. At the instant t_2, a reverse anode voltage is developed and the reverse recovery current continues to decrease. At t_3, junction J_1 and J_3 are able to block a reverse voltage. However, the thyristor is not yet able to block a forward voltage because carriers, called *trapped charges*, are still present at the junction J_2. During the interval t_3 to t_4, these carriers recombine. At t_4, the recombination is complete and therefore, a forward voltage can be reapplied at this instant. The SCR turn-off time is the interval between t_4 and t_1. In an SCR, this time varies in the range 10 to 100 μs. Thus, the total turn-off time (t_q) required for the device is the sum of the duration for which the reverse recovery current flows after the application of reverse voltage, and the time required for the recombination of all excess carriers in the

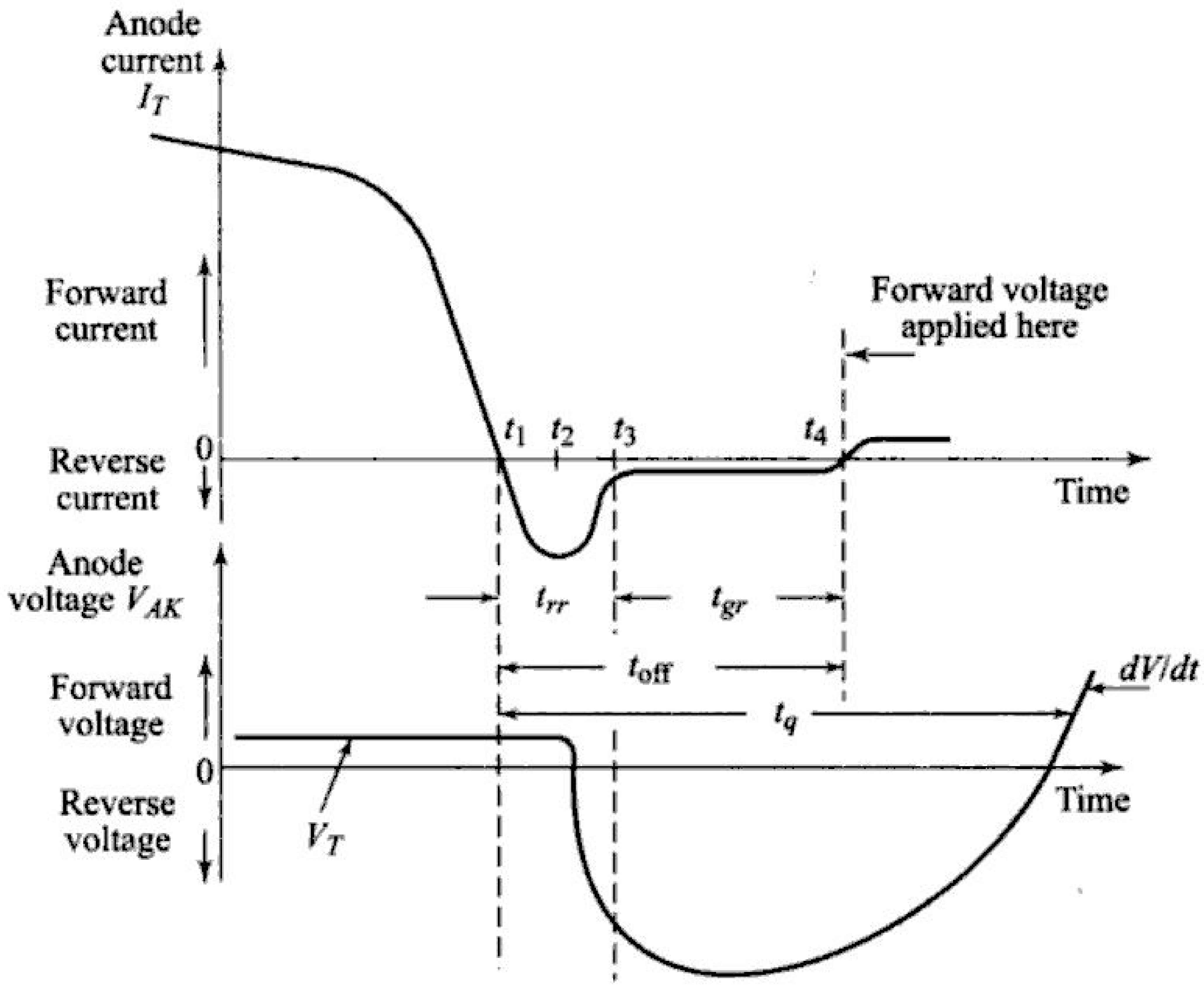


Fig. 2.11 *Waveforms during SCR turn-off*

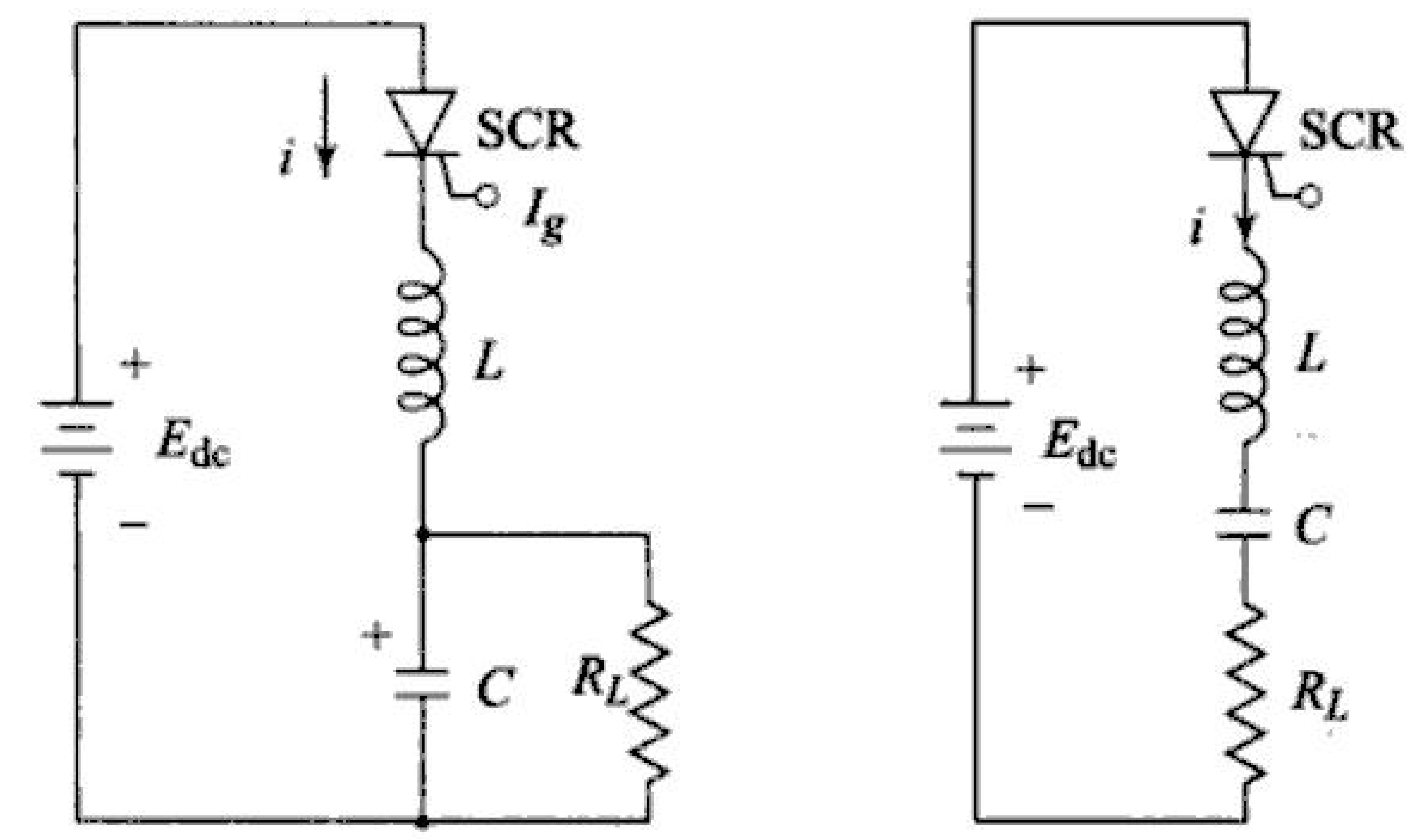
inner two layers of the device. This may be noted that in case of highly inductive load circuit, the current cannot change abruptly at t_1. Also, the fast change in current at t_2 may give rise to high voltage surges in the inductance, which will then appears across the terminals of the thyristor.

In practical applications, the turn-off time required to the SCR by the circuit, called the circuit turn-off time t_q, must be greater than the device turn-off time t_{off} by a suitably safe margin, otherwise the device will turn-on at an undesired instant a process known as *commutation failure*. Thyristor having large turn-off time (50–100 μs) are called as slow switching or phase control type thyristors (or converter grade thyristors), and those having low turn-off time (10–50 μs) are called fast switching or inverter type thyristors. In high frequency applications, the required circuit turn-off time consumes an appreciable portion of the total cycle time and therefore, inverter grade thyristors must be used.

2.10 TURN-OFF METHODS

The term *commutation* basically means the transfer of current from one path to another. In thyristor circuits, this term is used to describe process of transferring current from one thyristor to another. As explained earlier, it is not possible for a thyristor to turn itself OFF; the circuit in which it is connected must reduce the thyristor current to zero to enable it to turn-off. 'Commutation' is the term to describe the methods of achieving this.

L–C circuit. In this process of commutation, the forward current passing through the device is reduced to less than the level of holding current of the device. Hence, this method is also known as the current commutation method. The waveforms of the thyristor voltage, current and capacitor voltages are shown in Fig. 2.13.



(a) Load in parallel with capacitor (b) Load in series with capacitor

Fig. 2.12 *Class A commutation circuit*

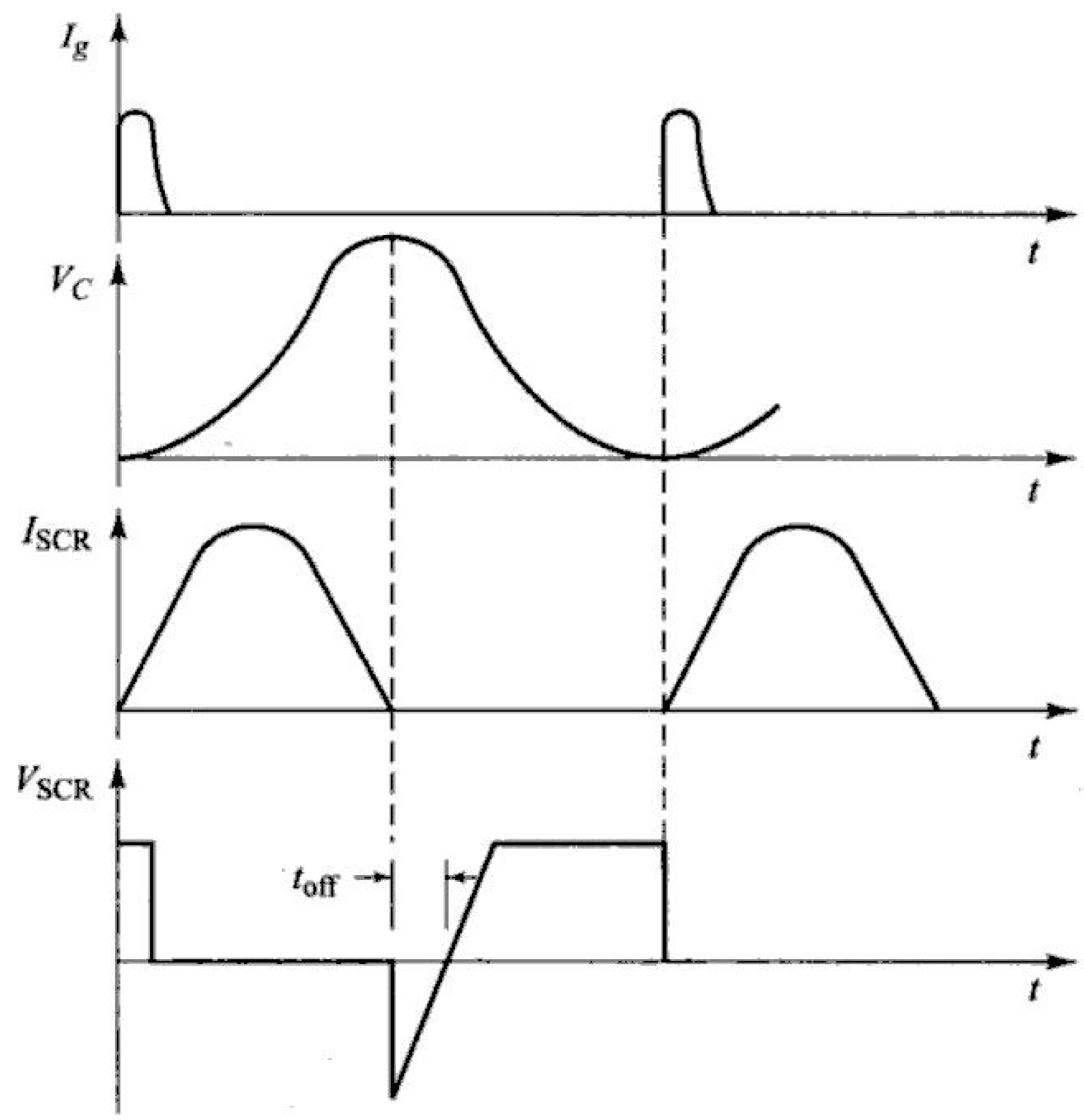
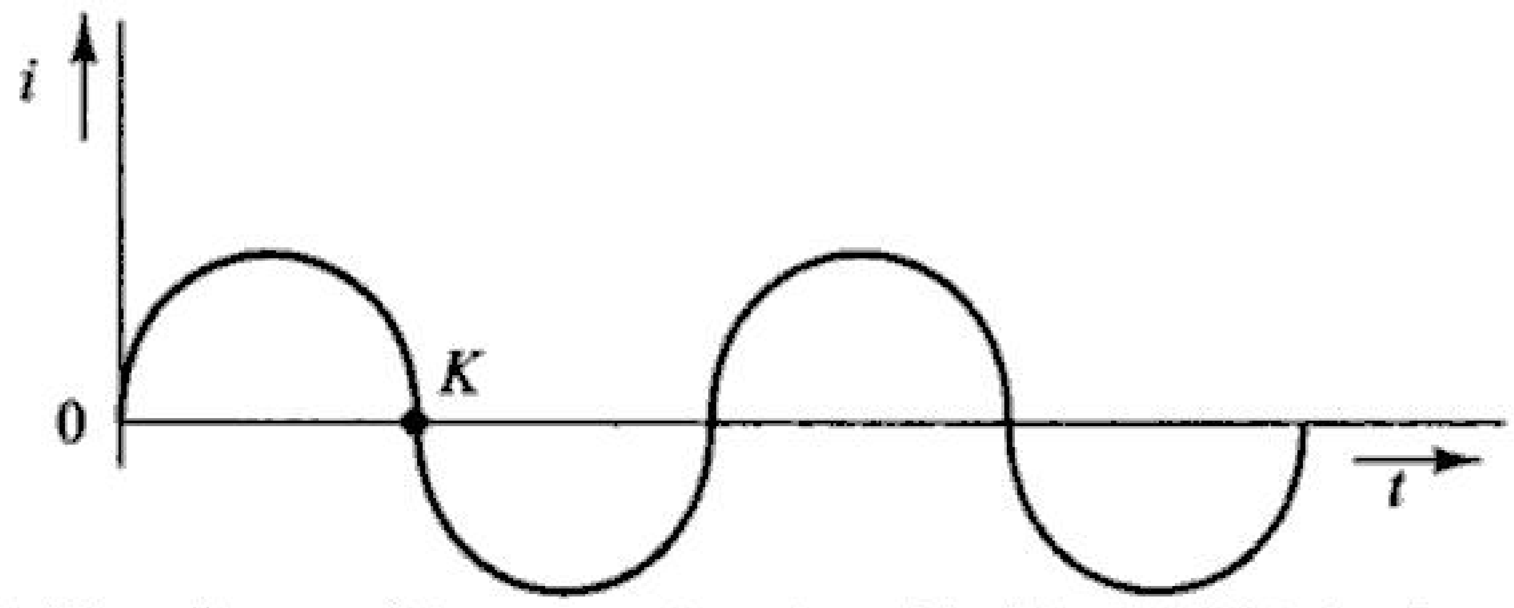
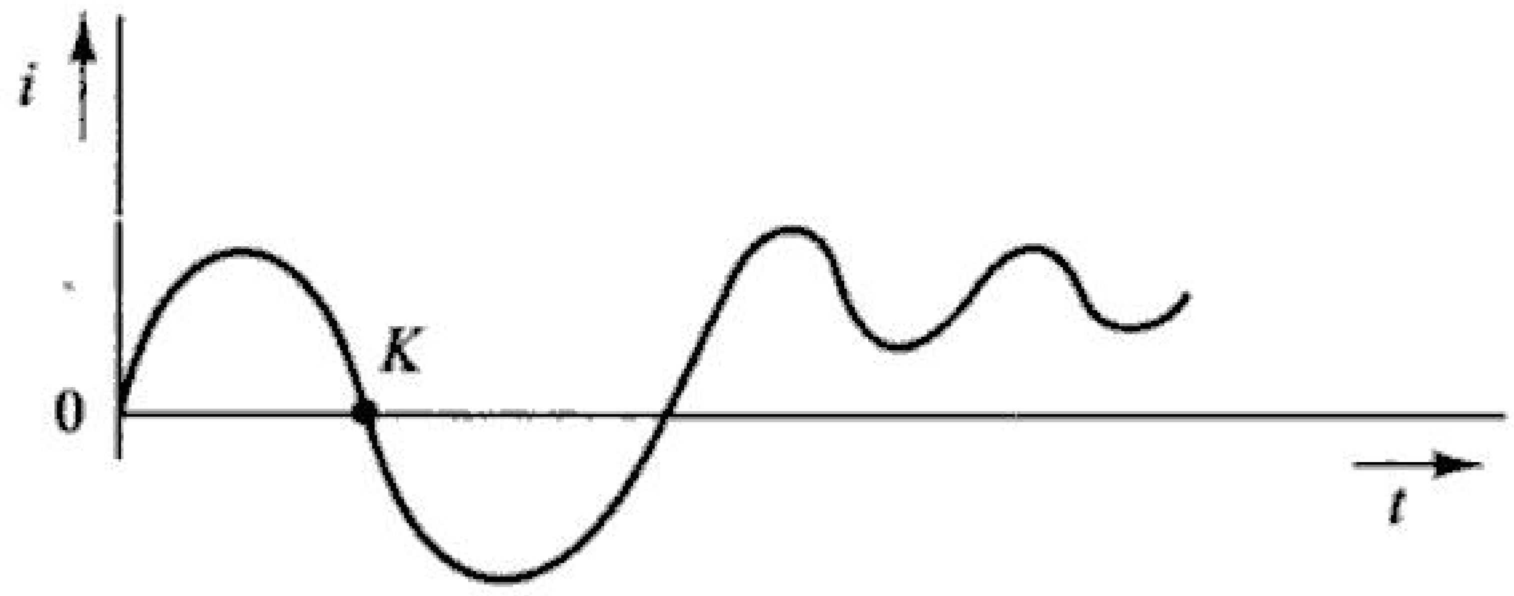


Fig. 2.13 *Voltages and currents in Class A (load is parallel with capacitor)*



(a) Waveforms of the current produced in Fig. 2.12(b) (series capacitor)



(b) Waveforms of the current produced in Fig. 2.12(a) (parallel capacitor)

Fig. 2.14

The load resistance R_L and the commutating components are so selected that their combination forms an underdamped resonant circuit. When such a circuit is excited by a d.c. source, a current of the nature shown in Fig. 2.14 will be obtained across the device. This current, as evident from its shape, has zero value at the point K where the device is automatically turned OFF. Beyond point K, the current is reversed in nature which assures definite commutation of the device. The thyristor when ON carries only the charging current of capacitor C which will soon decay to a valueless than the holding current of the device, when capacitor C is charged up to the supply voltage E_{dc}. This simultaneously switches off the thyristor. The time for switching off the device is determined by the resonant frequency which in turn depends on the values of the commutating components L and C, and the total load resistance.

This type of commutation circuits are most suitable for high frequency operation, i.e., above 1000 Hz, because of the need for an L–C resonant circuit which carries the full load current. This commutation circuit is used in series inverter.

Design Considerations

(a) Load in parallel with capacitor C Let us consider the resonant circuit of Fig. 2.12 (a). Let E_{dc} be the applied d.c. voltage, V be the load voltage, and i be the load current.

The circuit equation is

$$E_{dc} = L\,\frac{di}{dt} + V$$

and $$i = C\frac{dV}{dt} + \frac{V}{R}$$

By using Laplace transform, we can write

$$E_{dc}(s) - V(s) = S \cdot L\, I(s) \tag{2.15}$$

and $$I(s) = \frac{V(s)}{R} + S \cdot C \cdot V(s) \tag{2.16}$$

From Eq. (2.15), we can write

$$V(s) = E_{dc}(s) - SL\, I(s) \tag{2.17}$$

But $$E_{dc}(s) = \frac{E_{dc}}{S} \tag{2.18}$$

Substitute Eqs (2.17) and (2.18) in Eq. (2.16)

$$\therefore \quad I(s) = \frac{E_{dc}}{R \cdot S} - \frac{SLI(s)}{R} + SC\left[\frac{E_{dc}}{s} - SLI(s)\right]$$

$$I(s) + SL\,\frac{I(s)}{R} + S^2\, CLI(s) = \frac{E_{dc}}{R \cdot S} + \frac{E_{dc}SC}{S}$$

$$\therefore \quad I(s)\left[1 + \frac{SL}{R} + S^2CL\right] = \frac{E_{dc}}{S}\left[\frac{1}{R} + SC\right]$$

$$I(s)\left[\frac{R + LS + RCLS^2}{R}\right] = \frac{E_{dc}}{s}\left[\frac{1 + RCS}{R}\right]$$

$$I(s) = \frac{E_{dc}}{s}\left[\frac{1 + RCS}{R + LS + RCLS^2}\right]$$

$$I(s) = \frac{E_{dc}}{RLCS}\left[\frac{1 + RCS}{S^2 + \frac{1}{RC}S + \frac{1}{LC}}\right] \tag{2.19}$$

Taking inverse Laplace transform of Eq. (2.19), we get

$$i(t) = \frac{E_{dc}}{R}\left[1 + \frac{1}{\sqrt{1-\varepsilon^2}}\,\frac{W_n^2}{\varepsilon}\, e^{-t/RC}\sin(\omega t + \phi)\right]$$

where $\varepsilon = \frac{1}{2R}\sqrt{\frac{L}{C}}$ = damping ratio

$W_n = \frac{1}{\sqrt{LC}}$ = undamped natural angular frequency.

The solution of this well known second order equation for under damped case is

$$i = e^{-\varepsilon t}\,[A_1 \cos \omega t + A_2 \sin \omega t] \qquad (2.26)$$

where $$\varepsilon = \frac{R}{2l} \qquad (2.27)$$

and $$\omega_o = \frac{1}{\sqrt{LC}} \qquad (2.28)$$

$$\omega = \omega_o \sqrt{1-\varepsilon^2} = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \qquad (2.29)$$

When $i(0+) = i(0-) = 0$

$$A_1 = 0, \qquad A_2 = \frac{E_{dc}}{L}$$

This gives $$i(t) = e^{-\frac{R}{2L}t}\left[\frac{E_{dc}}{\omega L}\sin \omega t\right] \qquad (2.30)$$

This equation shows that the thyristor-current i goes to zero at

$$\omega t = \pi$$

or $$t = \frac{\pi}{\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}} \qquad (2.31)$$

Now, $$\frac{di}{dt} = -\,e^{-\frac{\pi R}{2\omega L}}\left(\frac{E_{dc}}{l}\right)$$

Therefore, the capacitor voltage at the end of conduction, $V_c = E_{dc} - V_L$

where $V_L = L\,di/dt$

$$\therefore \quad V_c = E_{dc}\left[1 + e^{-\pi R/2\omega L}\right] \qquad (2.32)$$

Now, if V_0 is the initial-state voltage of the capacitor then Eq. (2.30) becomes

$$i(t) = e^{-(R/2L)t}\left[\frac{E_{dc} - V_0}{\omega L}\cdot\sin \omega t\right] \qquad (2.33)$$

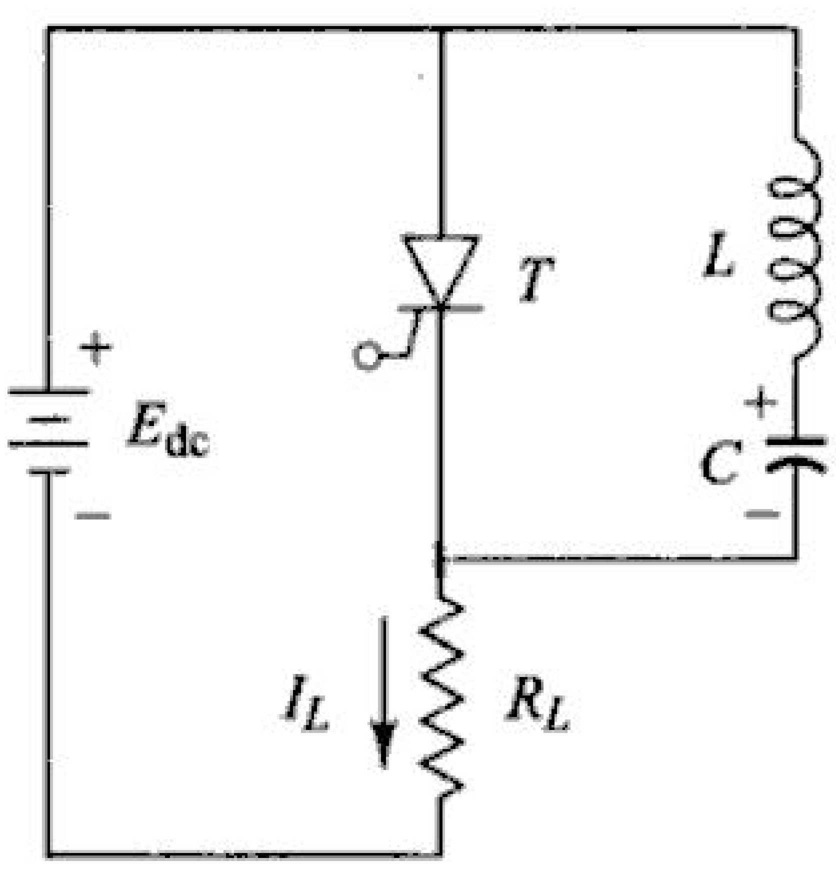
and $$V_c = E_{dc} + e^{-\pi R/2\omega t}\,(E_{dc} - V_0) \qquad (2.34)$$

For $\omega > 0$, we now calculate the condition for underdamped.

$$\therefore \quad \frac{1}{LC} - \frac{R^2}{4L^2} > 0 \qquad \text{i.e.,}\ \frac{1}{LC} > \frac{R^2}{4L^2}$$

or $$R < \sqrt{\frac{4L}{C}} \qquad (2.35)$$

2. *Class B—Self Commutation by an LC Circuit* In this method, the *LC* resonating circuit is across the SCR and not in series with the load. The commutating circuit is shown in Fig. 2.15 and the associated waveforms are shown in Fig. 2.16.



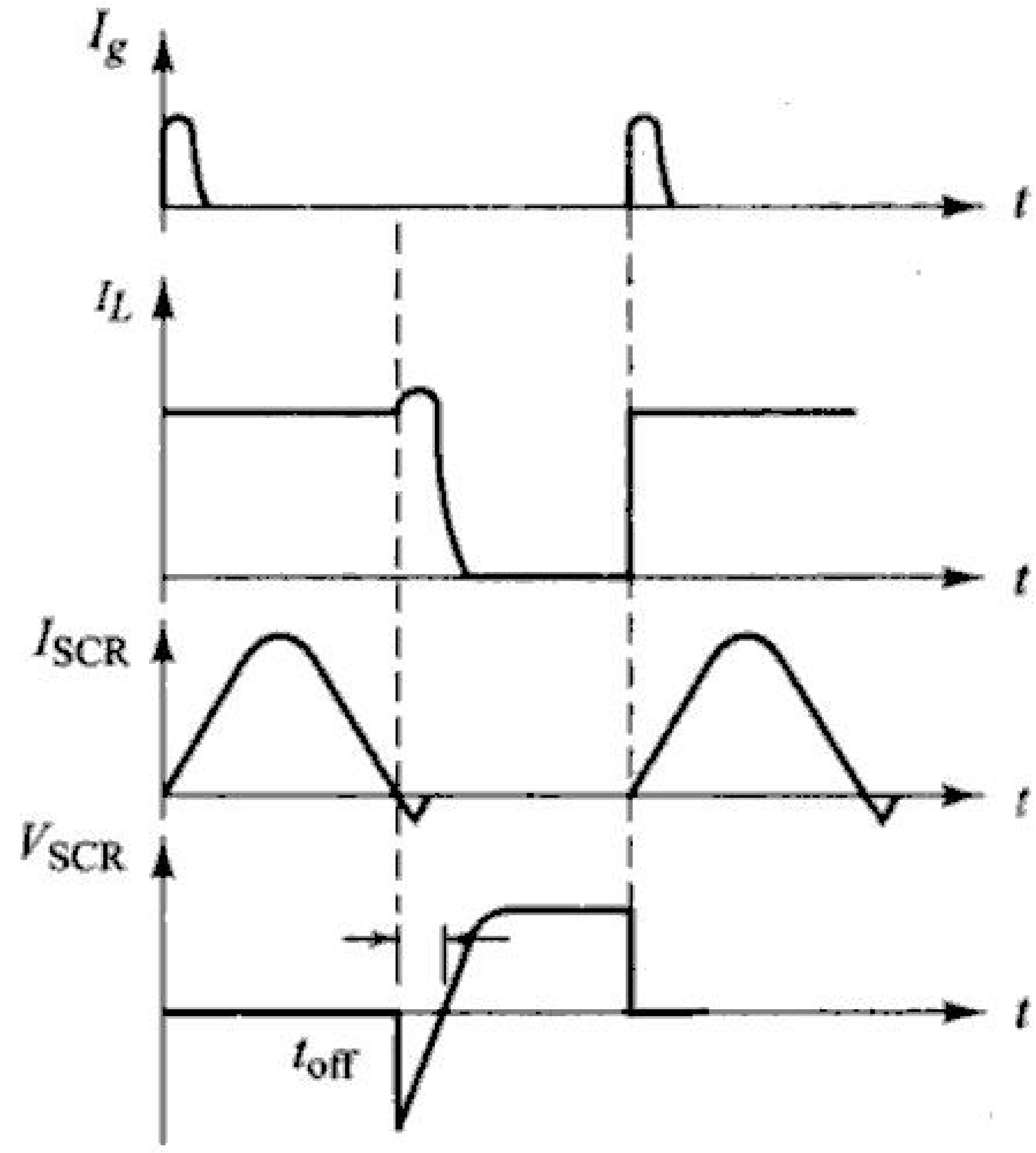


Fig. 2.15 *Class B commutation circuit* **Fig. 2.16** *Associated waveforms*

Initially, as soon as the supply voltage E_{dc} is applied, the capacitor *C* starts getting charged with its upper plate positive and the lower plate negative, and it charges up to the voltage E_{dc}.

When thyristor *T* is triggered, the circuit current flows in two directions: (1) The load current I_L flows through the path $E_{dc+} - T - RL - E_{dc-}$, and (2) Commutating current I_c.

The moment thyristor *T* is turned ON, capacitor C starts discharging through the path $C_+ - L - T - C-$. When the capacitor *C* becomes completely discharged, it starts getting charged with reverse polarity. Due to the reverse voltage, a commutating current I_C starts flowing which opposes the load current I_L. When the commutating current I_C is greater than the load current I_L, thyristor *T* becomes turned OFF. When the thyristor *T* is turned OFF, capacitor C again starts getting charged to its original polarity through *L* and the load. Thus, when it is fully charged, the thyristor will be ON again.

Hence, from the above discussion it becomes clear that the thyristor after getting ON for sometime automatically gets OFF and after remaining in OFF state for sometime, it again gets turned ON. This process of switching ON and OFF is a continuous process. The desired frequency of ON and OFF states can be obtained by designing the commutating components as per the requirement. The main application of this process is in d.c. chopper circuits, where the thyristor is required to be in conduction state for a specified duration and then to remain in the OFF state also for a specified duration. Morgan chopper circuit using a saturable reactor in place of the ordinary inductor L is a modified arrangement for this process. The circuit has the advantage of longer oscillation period and therefore of more assurance of commutation. In this Class B commutation method, the commutating component does not carry the load current. Both Class A and Class B turn-off circuits are self-commutating types, that is in both of these circuits the SCR turns-off automatically after it has been turned on.

Design Considerations

The circuit equations for the LC circuit are:

$$L\,\frac{di}{dt} + \frac{1}{C}\int i\,dt = 0 \tag{2.36}$$

$$\therefore \quad L\,\frac{d^2 i}{dt^2} + \frac{1}{C}\,i(t) = 0$$

Taking laplace transform of the above equation, $\left(S^2 L + \frac{1}{C}\right) I(s) = 0$

$$\therefore \quad i(t) = E_{dc}\sqrt{\frac{C}{L}}\,\sin\omega_0 t \tag{2.37}$$

where

$$\omega_0 = \sqrt{\frac{1}{LC}} \tag{2.38}$$

Therefore, the peak commutation current is

$$I_{C_{(peak)}} = E_{dc}\cdot\sqrt{C/L} \tag{2.39}$$

For this Class B commutation method, the peak discharge current of the capacitor is assumed to be twice the load-current I_L, and the time for which the SCR is reverse biased is approximately equal to one-quarter period of the resonant circuit.

Therefore,

$$I_{C_{(peak)}} = 2\,I_L = E_{dc}\sqrt{C/L} \tag{2.40}$$

And

$$t_{off} = \frac{\pi}{2}\sqrt{LC} \tag{2.41}$$

3. Class C—Complementary Commutation (Switching a Charged Capacitor by a Load Carrying SCR) The class C commutation circuit is shown in Fig. 2.17. In this method, the main thyristor (SCR T_1) that is to be commutated is connected in series with the load. An additional thyristor (SCR T_2), called the complementary thyristor is connected in parallel with the main thyristor.

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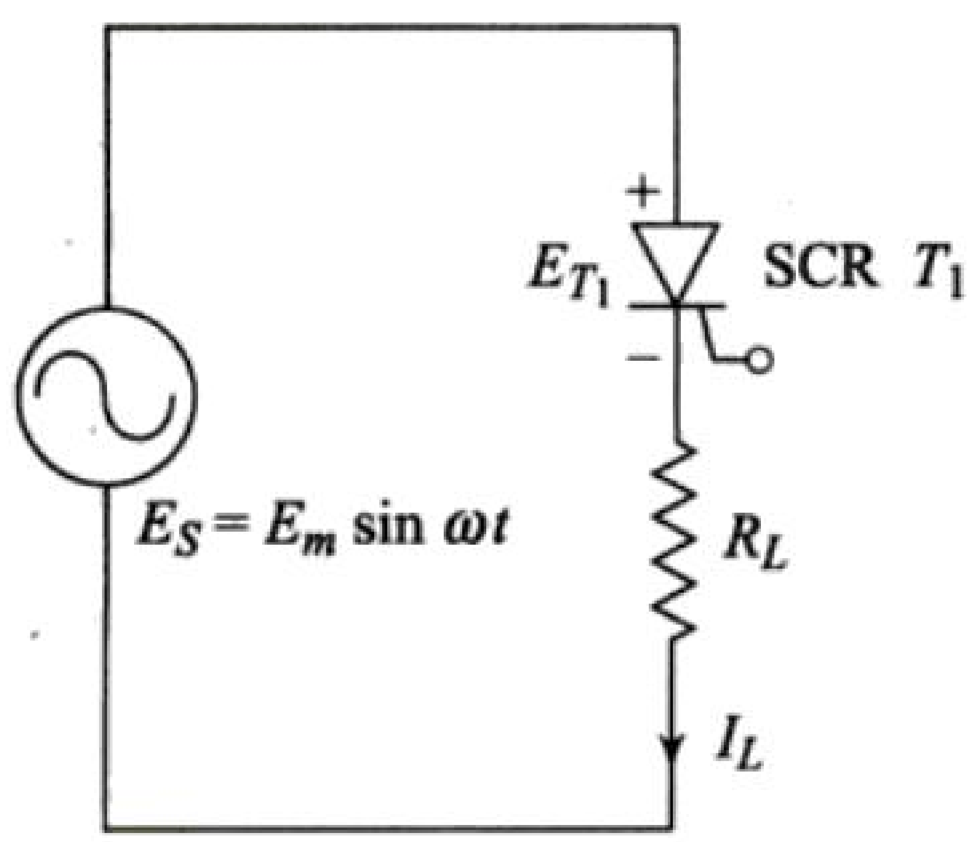

Fig. 2.23 *Class F commutation circuit*

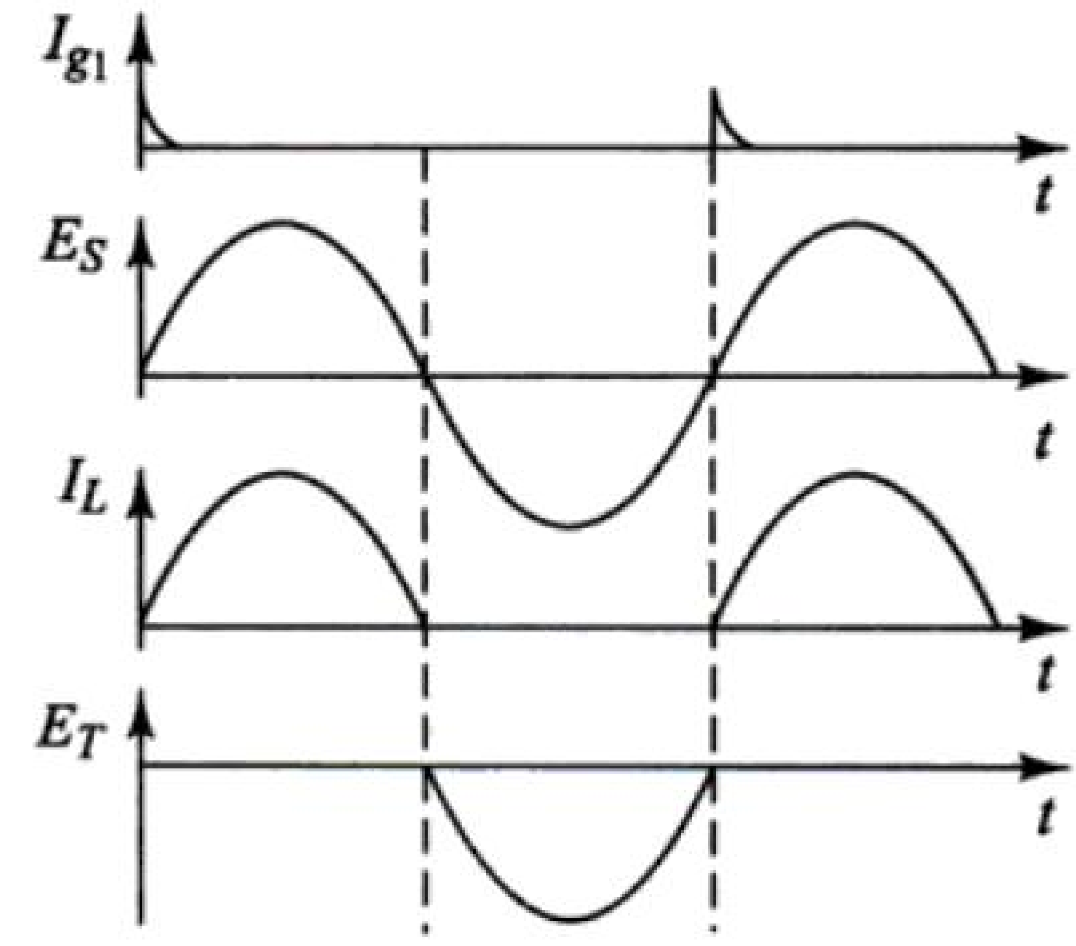

Fig. 2.24 *Associated waveforms*

SOLVED EXAMPLES

Example 2.9 For the Class C commutation circuit of Fig. 2.17, the d.c. source voltage $E_{dc} = 120$ V and current through R_1 and $R_2 = 20$ A. The turn-off time of both the SCRs is 60 μs. Calculate the value of commutating capacitance C for successful commutation.

Solution: The resistances $R_1 = R_2 = \dfrac{E_{dc}}{I} = \dfrac{120}{20} = 6$ W

Now, we have the relation for C for successful commutation as

$$C = 1.44 \,.\, \frac{t_{off}}{R_1} = 1.44 \times \frac{60 \times 10^{-6}}{6} = 14.4\ \mu\text{F}.$$

Example 2.10 For the Class D commutation circuit of Fig. 2.19, compute the value of the commutations capacitor C and commutating inductor L for the following data:

$$E_{dc} = 50V, I_{L(max)} = 50\text{ A}, t_{off} \quad \text{of} \quad \text{SCR}_1 = 30\ \mu\text{s}$$

Chopping frequency $f = 500$ Hz and the load voltage variation required is 10 to 100%.

Solution: For reliable operation, let us assume 50% tolerance on turn-off time of SCR_1.

$$\therefore \qquad t_{off} = \left(30 + \frac{50}{100} \times 30\right) = 45\mu\text{s}$$

Now, we have the relation for the commutating capacitor, C as

$$C = \frac{I_L\, t_{off}}{E_{dc}} = \frac{50 \times 45 \times 10^{-6}}{50} = C = 45\ \mu\text{F}.$$

The resetting time for capacitor voltage could be reduced by decreasing the value of L, but the peak capacitor current would increase as seen from Eq. (2.51). A large resetting time would limit the minimum voltage available at the load, which means the range of voltage available at the load is reduced.

Therefore, the minimum load voltage available is given by

$$V_{0(\min)} = \frac{t_1 - t_2}{T} E_{dc}$$

where t is chopping time period, or

$$V_{0(\min)} = \frac{\pi\sqrt{LC}}{T} E_{dc}$$

$$\therefore \qquad L \le \left(\frac{V_{0(\min)}}{E_{dc}}\right)^2 \frac{T^2}{\pi^2 C} \qquad \text{(i)}$$

Given $\qquad V_{0(\min)} = 10\%(50) = 5\text{ V}$

$$T = \frac{1}{f} = 2 \times 10^{-3}\text{ s}$$

$$\therefore \qquad L \le \frac{(2\times10^{-3})^2}{\pi^2 \times 45\times10^{-6}} \times \left(\frac{5}{50}\right)^2 \quad \text{or} \quad L \le 90\ \mu\text{H}$$

Also, we have the relation

$$L \ge C\left(\frac{E_{dc}}{I_{L(\max)}}\right)^2 \quad \text{or} \quad L \ge 45 \times 10^{-6}\left(\frac{50}{50}\right)^2$$

or $\qquad L \ge 45\ \mu\text{H}$

Hence, the range of commutating inductor is 45 μH < L < 90 μH

The choice of lower value of L would allow a larger voltage variation at the load.

2.11 THYRISTOR RATINGS

All semiconductor devices have definite limits to their capability and exceeding these even for short times will result in failure, loss of control, or irreversible deterioration. All thyristors, therefore, have to be used within their limits and this must include extreme conditions as may exist during circuit faults and it must take into account load, supply system, temperature and environmental variations. If extreme conditions are not precisely known and cannot be calculated, then appropriate safety margins have to be chosen to allow for the unknown factors. Correct safety margins can only be decided from practical operating experience. Therefore, the reliable operation of the device can be ensured only if its ratings are not exceeded under all operating conditions. The objective of this section is to discuss the various SCR ratings.

2.11.1 Voltage Ratings

It is essential that the voltage capability of a thyristor is not exceeded during operation even for a very short period of time. Therefore, the voltage rating of the device should be high enough to withstand anticipated voltage transients as well as the repetitive OFF state and reverse—blocking voltages. The various ratings related to the voltage are discussed in this section.

1. Working peak-off state forward voltage (V_{Dwm}) This is the maximum instantaneous value of the forward OFF state voltage that occurs across the thyristor excluding all repetitive and non-repetitive transient voltages.

2. Repetitive peak-off state forward voltage (V_{Drm}) It refers to the peak transient voltage that a thyristor in the OFF state can block repeatedly in the forward direction. This rating is specified at a maximum allowable junction temperature with gate circuit open or with a specified biasing resistance between the gate and cathode terminals.

3. Non-repetitive peak-off-state forward voltage (V_{DSM}) This is the maximum instantaneous value of any non-repetitive transient OFF state voltage that occurs across a thyristor.

4. Working peak reverse voltage (V_{RWM}) This is the maximum instantaneous value of the reverse voltage that occurs across the device excluding all repetitive and non-repetitive transient voltages.

5. Repetitive peak reverse voltage (V_{RRM}) This is the peak reverse transient voltage that may occur repeatedly in the reverse direction at the allowable maximum junction temperature. If this rating is exceeded, the SCR may be damaged due to excessive junction temperature.

6. Non-repetitive peak reverse voltage (V_{RSM}) This is the maximum transient reverse-voltage which can be safety blocked by the thyristor. The transient reverse voltage rating can be increased by inserting a diode of equal current rating in series with the thyristor.

7. On state voltage (V_T) This is the voltage drop between anode and cathode with specified forward ON state current and junction temperature. Its value is of the order of 1 to 1.5 V.

8. Gate trigger voltage (V_{GT}) This is the minimum gate voltage required to produce the gate trigger current.

9. Voltage safety factor (V_f) To avoid damage to a thyristor due to uncertain conditions, normal operating voltage is kept well below the V_{RSM} value of the device. The operating voltage and V_{RSM} (or peak inverse voltage V_{PIV}) value are related by the voltage safety factor V_f that is defined as

$$V_f = \frac{V_{RSM}\text{ (Peak Reverse Voltage)}}{\sqrt{2} \times \text{RMS Value of input voltage}} \tag{2.54}$$

The normal value of this factor lies between 2 and 2.5.

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lower than the capability to withstand static $\frac{dV}{dt}$. In Fig. 2.29, the rate of application of the forward voltage is varied by changing the charging rate of capacitor C_1. The initial value of dv/dt, when switch S_1 is closed and S_2 is open, is given by

$$\frac{dV}{dt} = \frac{E_s\, R_s}{C_1} \tag{2.57}$$

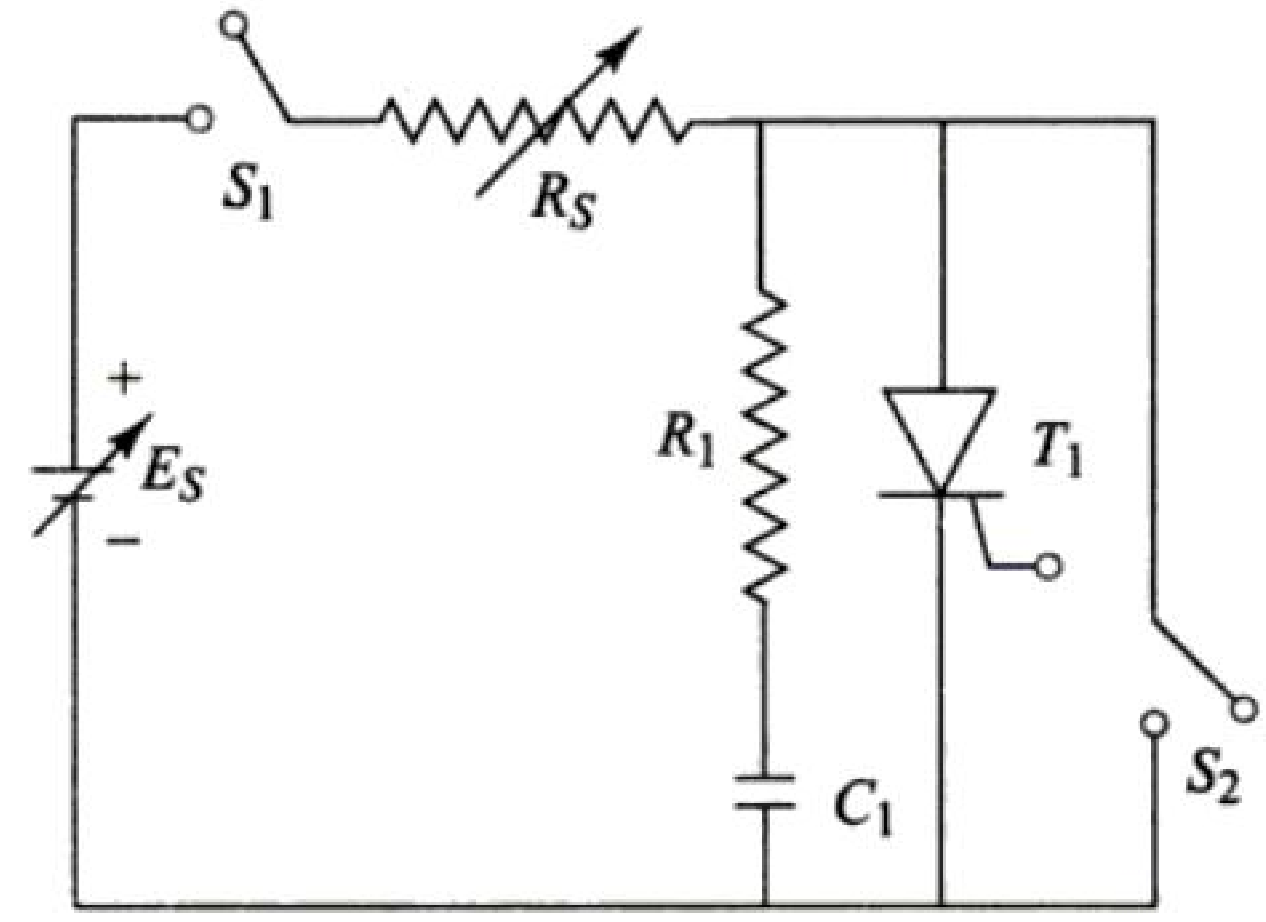

Fig. 2.29 *Circuit for the measurement of $\frac{dV}{dt}$ and $\frac{di}{dt}$*

If this value is more than the $\frac{dV}{dt}$ rating of the SCR, it will conduct without any external gate signal. It is assumed that resistance R_1 is very small and the initial jump in voltage appearing across the SCR $\frac{E_s\, R_s}{(R_s + R_1)}$ is small enough to maintain the SCR in the OFF state.

For conducting the $\frac{di}{dt}$ test on the SCR, connect a small inductor in series with the anode circuit. The rate of change of anode current after the device is triggered, is controlled by varying the initial voltage on the capacitor.

2.13 COMPARISON BETWEEN TRANSISTORS AND THYRISTORS

Both transistors and thyristors are semiconductor devices, but they differ in many ways as under:

Transistors	*Thyristors*
(1) Transistor is a three-layer, two junction device.	(1) Thyristor is a four layer, three junction device.
(2) To keep a transistor in the conducting state, a continuous base current is required.	(2) Thyristors require a pulse to make it conducting and thereafter it remain conducting.
(3) When transistors (power transistor) conduct appreciable current, the forward voltage drop is of the order of 0.3 to 0.8 V.	(3) The forward voltage drop across the device is of the order of 1.2 to 2 V.
(4) The voltage and current ratings of transistors available at present are not as high as those of thyristors.	(4) Due to the difference in fabrication and operation, thyristors with very high voltage and current ratings are available.

(Contd.)

Transistors	Thyristors
(5) Power transistors have no surge current capacity and can withstand only a low rate of change of current.	(5) Thyristors have surge-current rating and therefore can withstand high rate of change of current compared to transistors.
(6) Commutation circuitry, which is costly and bulky, is not required.	(6) Commutation circuit is required.
(7) Power transistors switch on faster than SCRs, and turn-off problems are practically non existent. If the base current is removed, the transistor turns off. Therefore, power-transistors can be used in very high-frequency applications.	(7) Thyristors are used in comparatively low frequency applications.
(8) Circuits using power transistors will be smaller in size and less costly compared to circuits using thyristors.	(8) Comparatively larger in size and is costlier.
(9) There has been little operating experience in high power applications of transistors. Power transistors or Darlington pairs are more susceptible to failure.	(9) Thyristor circuits, on the other hand, have a proven record of many years of reliable operation.

Review Questions

2.1 Describe the different modes of operation of a thyristor with the help of its static *V–I* characteristic.

2.2 Describe the holding current and latching current as applicable to an SCR with the help of its static *V–I* characteristic.

2.3 With the help of a neat diagram, explain the two transistor analogy of an SCR. Also discuss the triggering conditions of SCR.

2.4 Give the constructional details of an SCR. Sketch its schematic diagram and the circuit symbol.

2.5 Explain why

(i) The inner two layers of an SCR are lightly doped and are wide.

(ii) The inner *n* layer of an SCR is doped with gold.

(iii) I_H is less than I_L.

2.6 Explain in detail the turn-off mechanism of an SCR.

2.7 Explain the various types of triggering methods of SCR briefly. Which is the universal method and why?

2.8 What are the different signals which can be used for turning on an SCR by gate control? Compare them.

2.9 Draw the gate characteristic of an SCR and explain it.

2.10 Draw the turn-off characteristic of an SCR and explain the mechanism of turn-off.

2.11 What are the different methods for turning off an SCR? Explain all methods in detail.

2.12 Define the following terms in connection with SCR:
(i) Peak inverse voltage. (ii) Critical rate of rise of voltage
(iii) Voltage safety factor (iv) Latching current.
(v) Holding current

2.13 What do you mean by commutation of SCR? What are the different classes of forced commutation method? Explain the class C and class D methods.

2.14 Explain the following ratings of SCRs and their significance.
(i) Peak working reverse voltage (V_{Rwm})
(ii) Working peak OFF state forward voltage (V_{Dwm})
(iii) Repetitive peak OFF state forward voltage (V_{DRM})
(iv) Non-repetitive peak OFF state forward voltage (V_{RSM}).
(v) Repetitive peak reverse voltage (V_{RRM})
(vi) Non-repetitive peak reverse voltage (V_{RSM})
(vii) On state voltage

2.15 Explain in detail the following current ratings of SCR in detail
(i) Average ON state current (ii) Surge current rating
(iii) RMS ON state current (iv) $I^2\,t$ rating
(v) $\frac{di}{dt}$ rating

2.16 Explain in detail the power rating of SCR.

2.17 What are $\frac{dV}{dt}$ and $\frac{di}{dt}$ ratings of SCRs? What happens if these ratings are exceeded? Explain.

2.18 Explain the following thermal ratings of SCRs.
(i) Junction temperature. (ii) Transient thermal resistance.

2.19 Explain the methods of measurement of following SCR parameters
(i) Holding and latching current (ii) Turn-off time
(iii) $\frac{dV}{dt}$ and $\frac{di}{dt}$

2.20 Give the comparison between transistors and thyristors.

PROBLEMS

2.1 A typical thyristor circuit is shown in Fig. P2.1. If T_1 is switched ON at $t = 0$ determine the conduction time of thyristor T_1 and the capacitor voltage after T_1 is turned OFF. The inductor carries an initial current of $I_n = 250$A.
[*Ans*: $T_c = 38.45$ μs; $V_c = 297.97$ V]

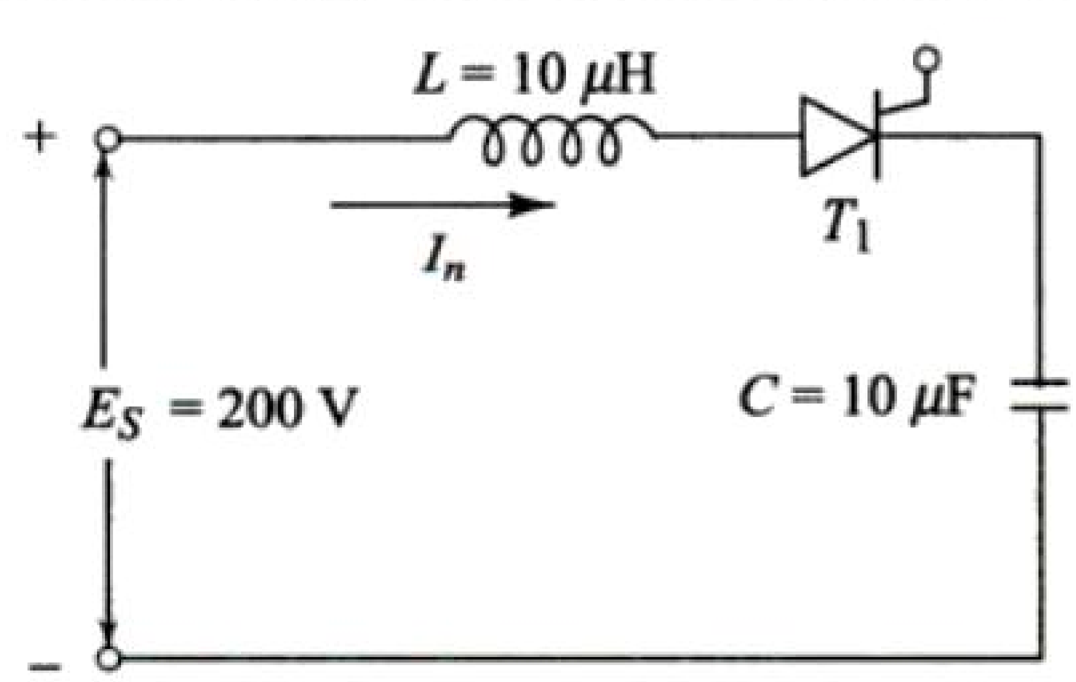

Fig. P2.1

2.2 The reverse biased junction capacitance of an SCR is 25 picofarads. The device can be turned ON if the charging current flowing through the junction capacitor is 5 mA. Calculate the $\frac{dV}{dt}$ capability of the device.
[*Ans*: 200 V/μs]

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Figure 3.4 shows different ways of using a transformer to drive an inverse parallel pair of SCRs. Full isolation is provided by the three-winding transformer in Fig. 3.4(a). Where such isolation is not required, a two-winding transformer may be used either in a series mode, Fig. 3.4(b) or a parallel mode Fig. 3.4(c). In any case, the pulse generator must supply sufficient energy to trigger both SCRs, and the pulse transformer (plus any additional balancing resistors) must supply sufficient gate current to both SCRs under worst conditions of unbalanced gate impedances.

A trigger pulse transformer is primarily used to enhance the efficiency. The simplest test is to use the designed trigger pulse generator to drive a 20 Ω resistor alone and then drive the same resistor through the pulse transformer. If the pulse waveforms across the resistor are the same under both conditions, the transformer is perfect. Some loss is to be expected, however, and must be compensated by increased drive from the generator.

3.4 OPTICAL ISOLATORS (OPTOISOLATORS)

A common situation where a low-voltage, low-current logic circuit controlling a high voltage, high current load is shown in Fig. 3.5. The logic circuit is usually an IC and is very often part of a process-control computer. The logic output E_0 will be either at 0 V (ground) or +5 V with respect to ground. When it is at 0 V, the SCR is "off" and the load receives no power from the ac source. When E_0 is + 5 V, the SCR is "on", and the 230 V ac is switched to the load.

Generally it is not desirable to have a direct electrical connection between low-power control circuitry and the high-power load it controls, as done in this circuit. One reason is the possibility of noise being coupled from the high current circuit into the logic circuitry, especially over the common ground-line. Another reason is the possibility of high voltage from the load circuitry feeding back into the logic circuit as a result of component failure. For example, if the SCR became shorted out between the gate and cathode, 230 V would be coupled to the logic circuit output and could easily destroy many ICs, and perhaps the whole computer.

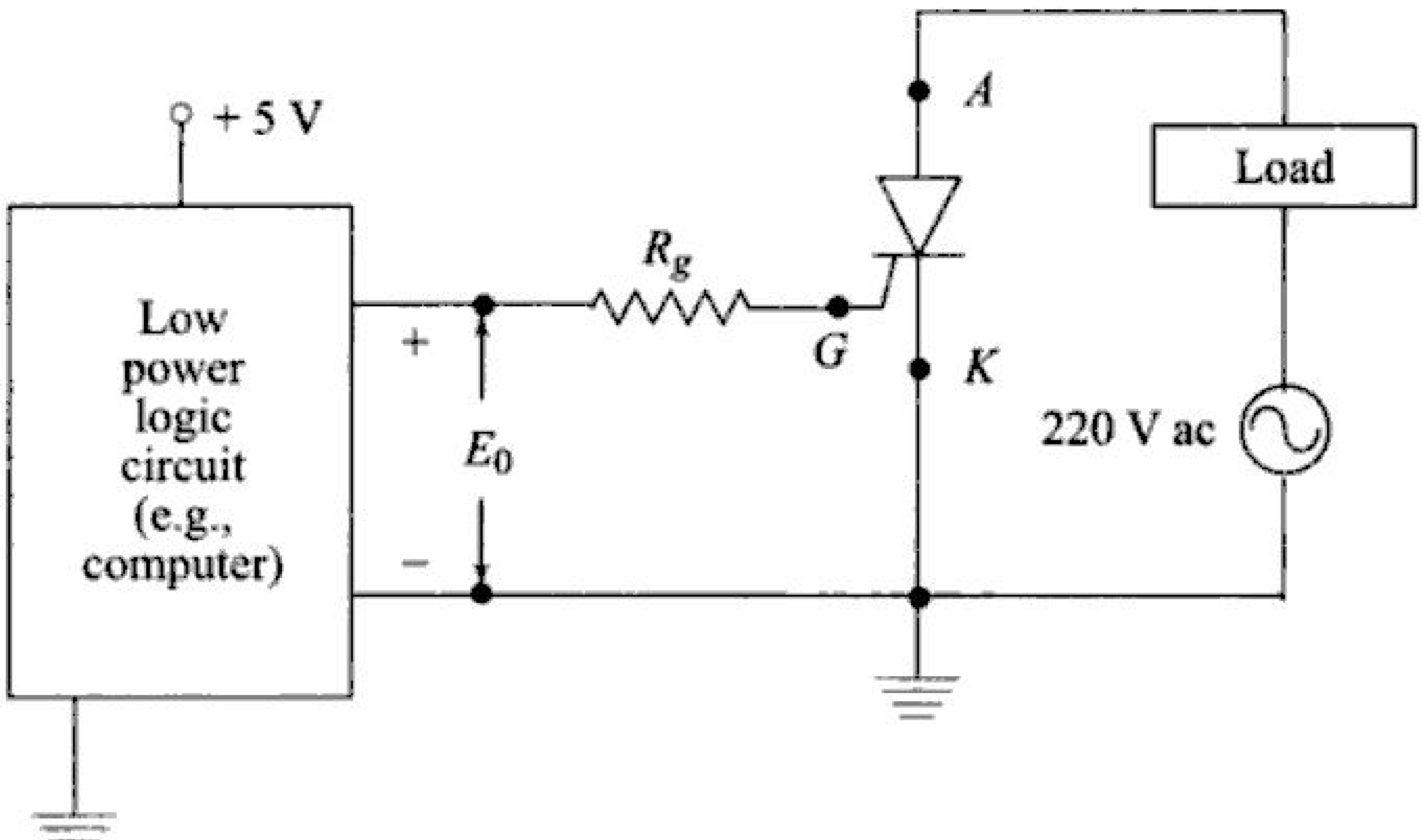


Fig. 3.5 *A low power logic circuit controlling a high-power load*

Thus, it is often necessary to electrically isolate the low-power control-circuitry and high power load circuitry. One means for doing this is to use an electro-mechanical relay (Fig. 3.6). The logic circuit drives the low current relay coil and the relay magnetically controls the switch contacts that connect power to the load.

While relays are widely used in industrial control applications, they do have certain shortcomings including—

(a) They are fairly expensive.
(b) Relays are bulkier than solid-state devices.
(c) They create magnetic fields and inductive "kick", which can be trouble-some sources of electrical noise.
(d) Relays have shorter-life than semiconductor devices.
(e) The contacts create sparking upon opening; this is highly undesirable in many industrial environments.

These disadvantages are largely overcome by devices called *optical isolators* or *optoisolators*, which use light energy to couple the control signal to the load. Optoisolators consists of a light-source (usually an infra-red emitting diode, IRED), a light sensitive device (e.g., a phototransistor) and a switching device. In most cases the light sensor and switching device are one and the same.

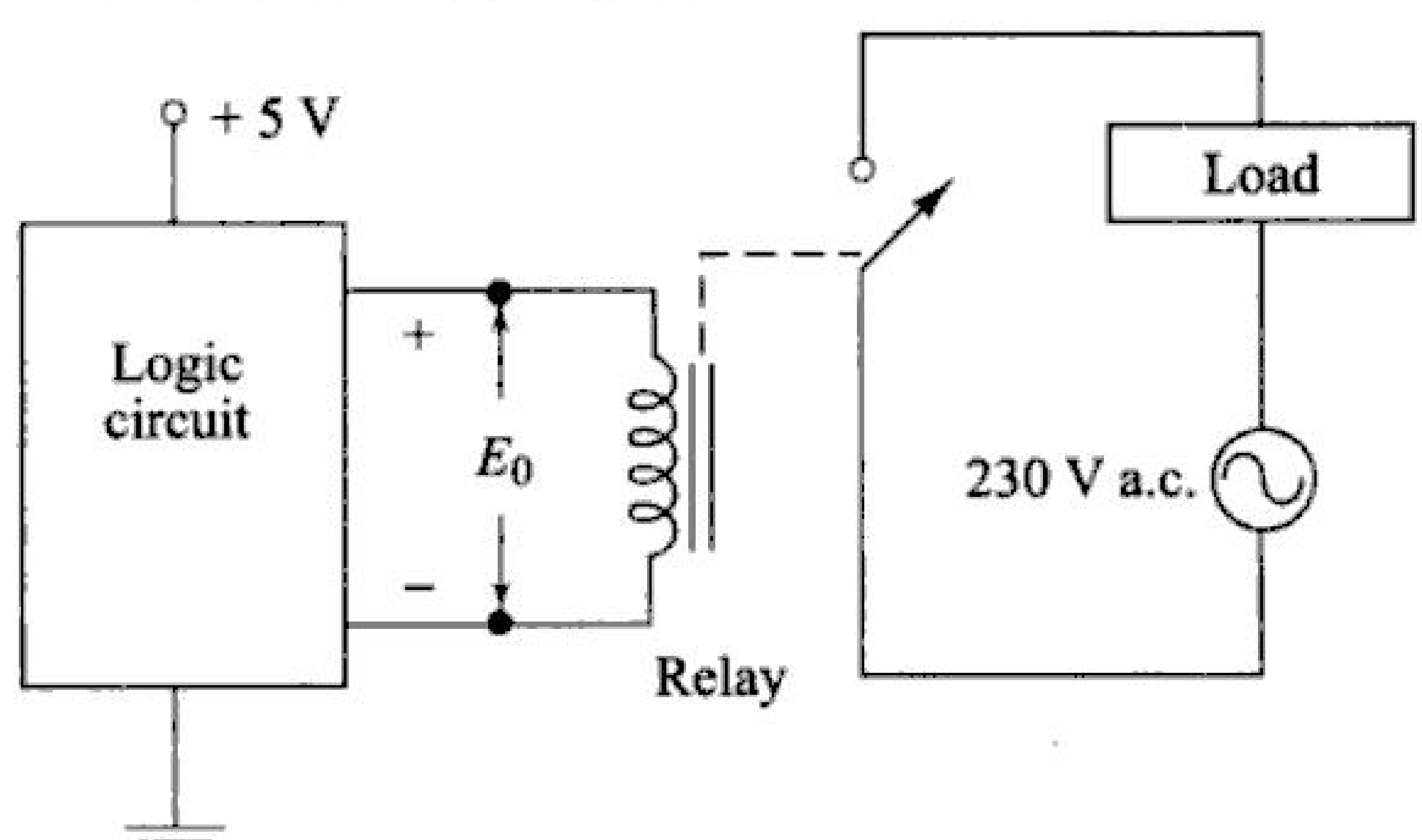


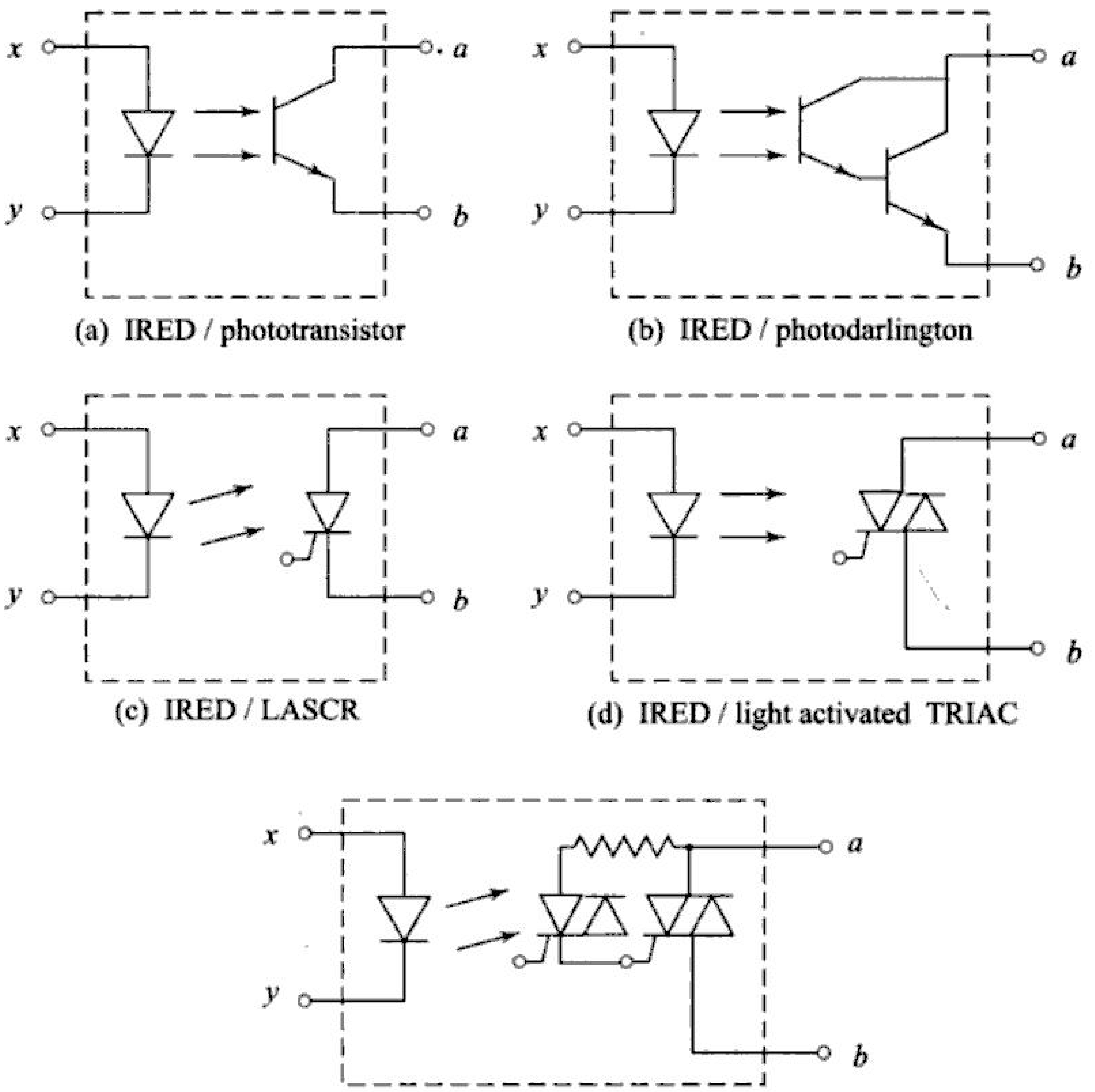
Fig. 3.6 *Electrical isolation provided by relay*

Figure 3.7 shows some of the available optoisolators. In each case, the devices inside the dotted lines are integrated into a single light-tight package with only input terminals x and y, and output terminals a and b accessible to the user. The input circuit is simply an IRED which emits IR radiation when it is sufficiently forward biased. This radiation is focused on a light sensitive device so that it switches "on" whenever sufficient current flows through the IRED. The opto-isolators in Figs 3.7 (a), (b) and (c) are used to switch d.c. power to a load, while those in Figs 3.7 (d) and (e) can switch a.c. power.

The various opto-isolators have different output current capabilities. The IRED-phototransistor combination can switch output currents of only around 10 mA, while the IRED/photodarlington can typically switch 500–100 mA. The darlington transistor coupler in Fig. 3.7(b) can be used when increased output current capability is needed beyond that provided by the phototransistor output. The disadvantage is that the photodarlington has a switching speed less than that of the phototransistor.

An LASCR output coupler is shown in Fig. 3.7(c), while a phototriac output coupler is shown in (d). Both combinations can typically switch 500 mA currents. For heavier current loads, the device in (e) can be used. It uses a light-activated TRIAC to trigger a high current TRIAC that switches currents of over 1A.

Figure 3.8 illustrates how an optoisolator can be used to isolated low-power control circuitry from a high power load. The output voltage from the logic circuit provides the relatively low current needed to activate the IRED, which in turn controls the light activated TRIAC. When E_0 is 0 V, the IRED is nonconducting and the TRIAC is held "off", so the load receives no a.c. voltage. When E_0 is + 5 V, the IRED conducts and its radiant energy turns the TRIAC "on" switching the a.c. voltage across the load. The load receives a.c. power as long as E_0 remains at + 5 V. Note that there is no direct electrical connection between the logic circuit and load circuit.



(a) IRED / phototransistor

(b) IRED / photodarlington

(c) IRED / LASCR

(d) IRED / light activated TRIAC

(e) IRED / Triac / Triac for high current a.c.

Fig. 3.7 *Common optoisolators*

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(b) When the emitter diode becomes forward biased, R_{B1} drops to a very low value (reason to be explained later) so that the total resistance between E and B_1 becomes very low, allowing emitter current to flow readily. This is the "on" state.

Circuit-operation The UJT is normally operated with both B_2 and E biased positive relative to B_1 as shown in Fig. 3.16. B_1 is always the UJT reference terminal and all voltages are measured relative to B_1. The V_{BB} source is generally fixed and provides a constant voltage from B_2 to B_1. The V_{EE} source is generally a variable voltage and is considered the input to the circuit. Very often, V_{EE} is not a source but a voltage across a capacitor.

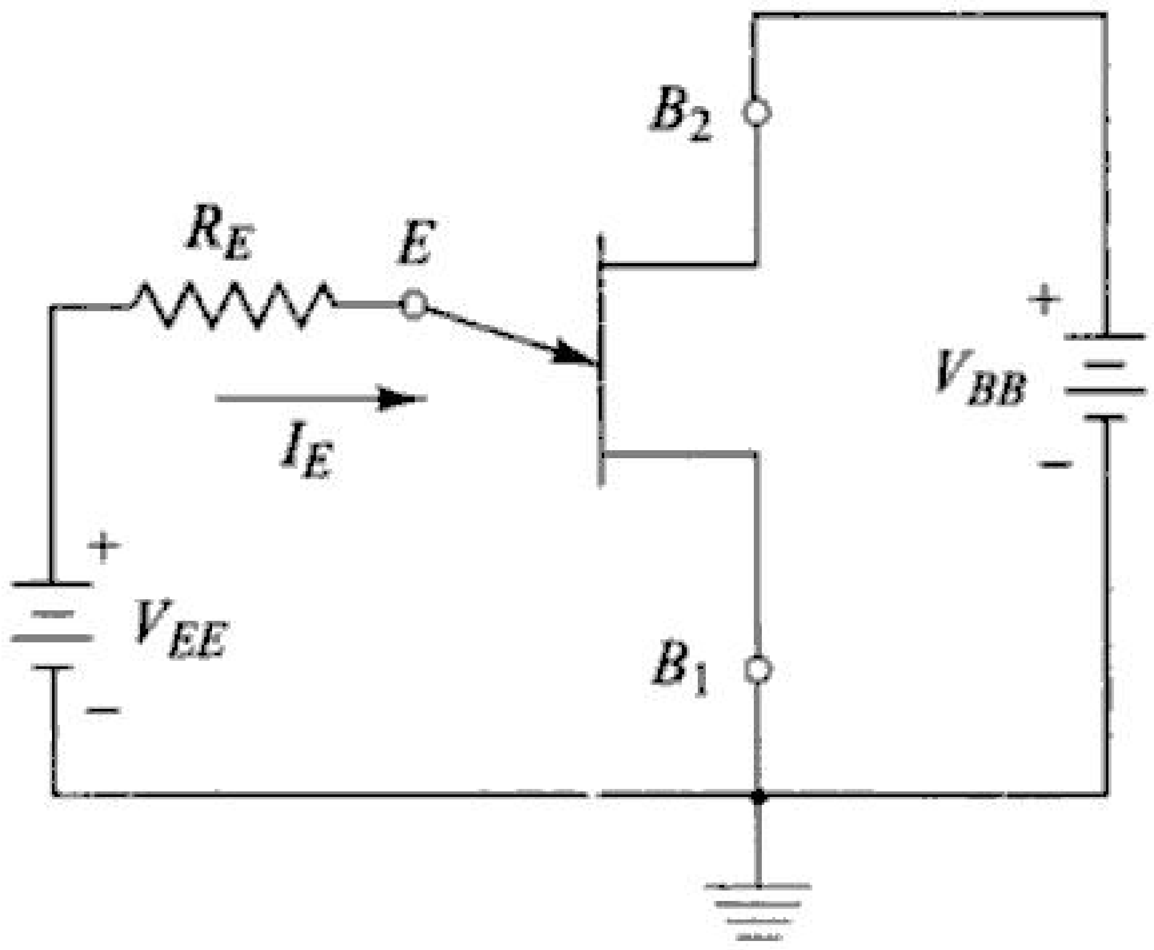

Fig. 3.16 *Normal UJT biasing*

We will analyze the UJT circuit operation with the aid of the UJT equivalent circuit, shown inside the dotted lines in Fig. 3.17(a). We will also utilize the UJT emitter-base-1 V_E-I_E curve shown in Fig. 3.17(b). The curve represents the variation of emitter current I_E, with emitter-base-1 voltage, V_E, at a constant B_2-B_1 voltage. The important points on the curve are labelled, and typical values are given in parentheses.

The "Off" state If we neglect the diode for a moment, we can see in Fig. 3.17(a) that R_{B_1} and R_{B_2} form a voltage divider that produces a voltage V_x from point x relative to ground.

$$\because \qquad V_x = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \times V_{BB} = \underbrace{\frac{R_{B_1}}{R_{BB}}}_{\eta} \times V_{BB}$$

or simply,

$$V_x = \eta\, V_{BB} \tag{3.9}$$

where η (the greek letter "eta") is the internal UJT voltage divider ratio $\dfrac{R_{B_1}}{R_{BB}}$ and is called the *intrinsic stand off ratio*.

Values of η typically range from 0.5 to 0.8 but are relatively constant for a given UJT.

The voltage at point x is the voltage on the N-side of the P-N junction. The V_{EE} source is applied to the emitter which is the P-side. Thus, the emitter diode will be reverse-biased as long as V_{EE} is less than V_x. This is the "off" state and is shown on the V_E–I_E curve as being a very low current region. In the "off" state, then, we can say that the UJT has a very high resistance between E and B_1, and I_E is usually a negligible reverse leakage current. With no I_E, the drop across R_E is zero and the emitter voltage, V_E, equals the source-voltage.

The UJT "off" state, as shown on the V_E–I_E curve, actually extends to the point where the emitter voltage exceeds V_x by the diode threshold voltage, V_D, which is needed to produce forward current through the diode. The emitter voltage and this point, P, is called the *peak-point voltage*, V_p, and is given by

$$V_p = V_x + V_D = \eta\, V_{BB} + V_D \qquad (3.10)$$

where V_D is typically 0.5 V. For example, if $\eta = 0.65$ and $V_{BB} = 20$V, then $V_p =$ 13.5 V. Clearly, V_P will vary as V_{BB} varies.

The "On" state As V_{EE} increases, the UJT stays "off" until V_E approaches the peak-point value V_p, then things begin to happen. As V_E approaches Vp, the *P-N* junction becomes forward biased and begins to conduct in the opposite direction.

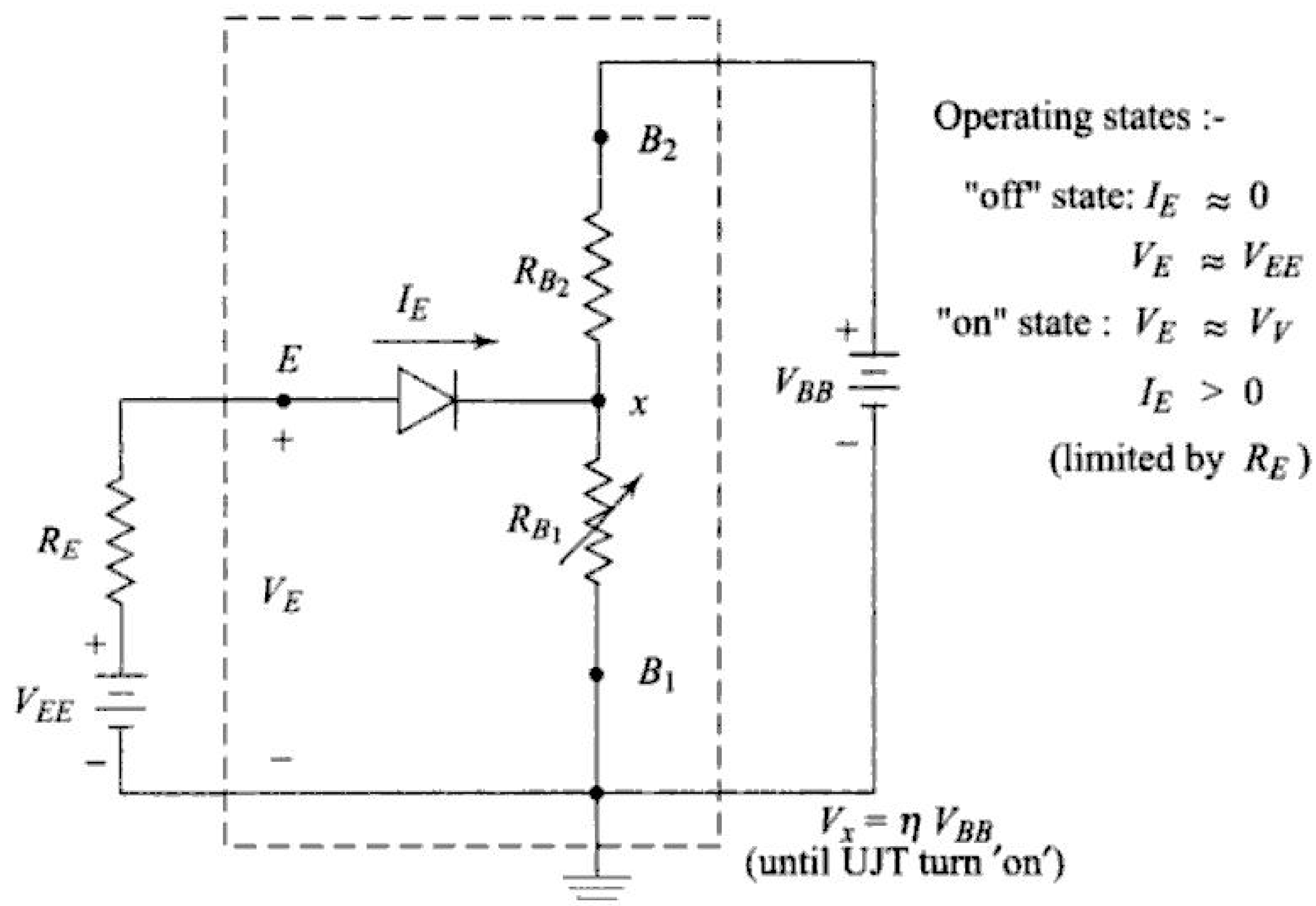

Fig. 3.17 ***(a)*** *Equivalent-circuit for UJT analysis*

Note on the V_E–I_E curve that I_E becomes positive near the peak point P. When V_E exactly equals V_p, the emitter current equals I_P, the *peak-point current*. At this point, holes from the heavily doped emitter are injected into the *N*-type bar, specially into the B_1 region. The bar, which is lightly doped, offers very little chance for these holes to recombine. As such, the lower half of the bar becomes replete with additional current carriers (holes) and its resistance R_{B_1} is drastically reduced. The decrease in R_{B_1} causes V_x to drop. This drop in turn causes the diode to become more forward biased, and I_E increases even further. The larger I_E injects more holes into B_1, further reducing R_{B_1}, and so on. When this *regenerative* or *snowballing* process ends, R_{B_1} has dropped to a very small value (2–25 Ω) and I_E can become very large, limited mainly by external resistance R_E.

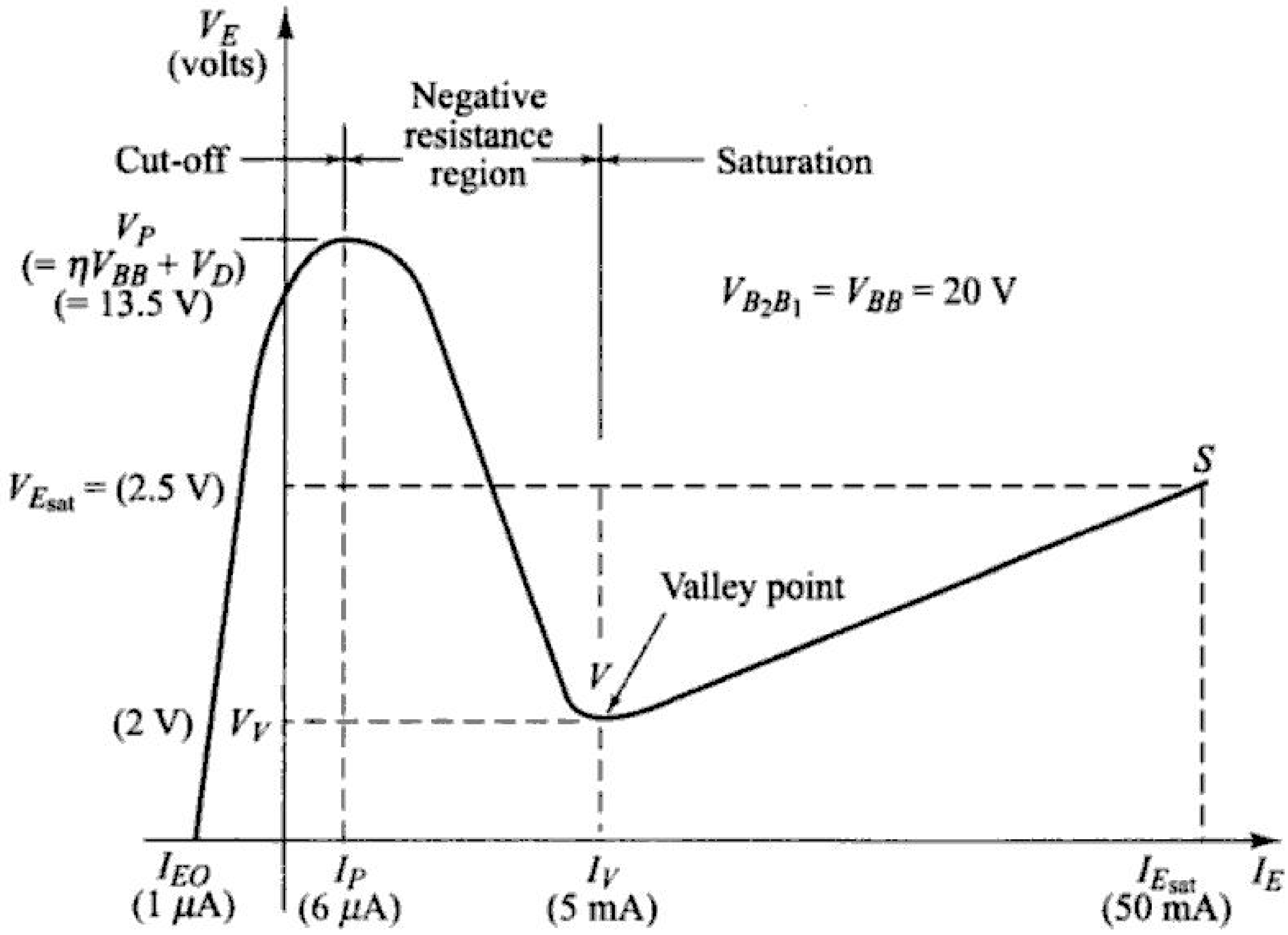

Fig. 3.17 ***(b)*** *Typical UJT V-I characteristic curve*

The UJT operation has switched to the low-voltage, high-current region of its $V_E - I_E$ curve. The slope of this "on" region is very steep, indicating a low resistance. In this region, the emitter voltage V_E, will be relatively small, typically 2 V, and remains fairly constant as I_E is increased up to its maximum rated value, $I_{E(sat)}$. Thus, once the UJT is "on," increasing V_{EE} will serve to increase I_E while V_E remains around 2V.

Turning "Off" the UJT Once it is "on," the UJT's emitter current depends mainly on V_{EE} and R_E. As V_{EE} decreases, I_E will decrease along the "on" portion of the $V_E - I_E$ curve. When I_E decreases to point V, the valley point, the emitter current is equal to I_V, the *valley current*, which is essentially the holding current needed to keep the UJT "on". When I_E is decreased below I_V, the UJT turns "off" and its operation rapidly switches back to the "off" region of its $V_E - I_E$ curve, where $I_E \approx 0$ and $V_E - V_{EE}$. The valley current is the counterpart of the holding current in *PNPN* devices, and generally ranges between 1 and 10 mA.

3.6.2 UJT Parameters and Ratings

A set of parameter and ratings for a typical UJT (2N2646) are listed in Table 3.1. Some of the entries were defined earlier. Those which require explanation are:

(a) *Maximum reverse emitter voltage* V_{B_2E}. This is the maximum reverse bias which the emitter-base-2 junction can tolerate before breakdown occurs.

(b) *Maximum interbase voltage.* This limit is caused by the maximum power that the *N*-type base bar can safely dissipate.

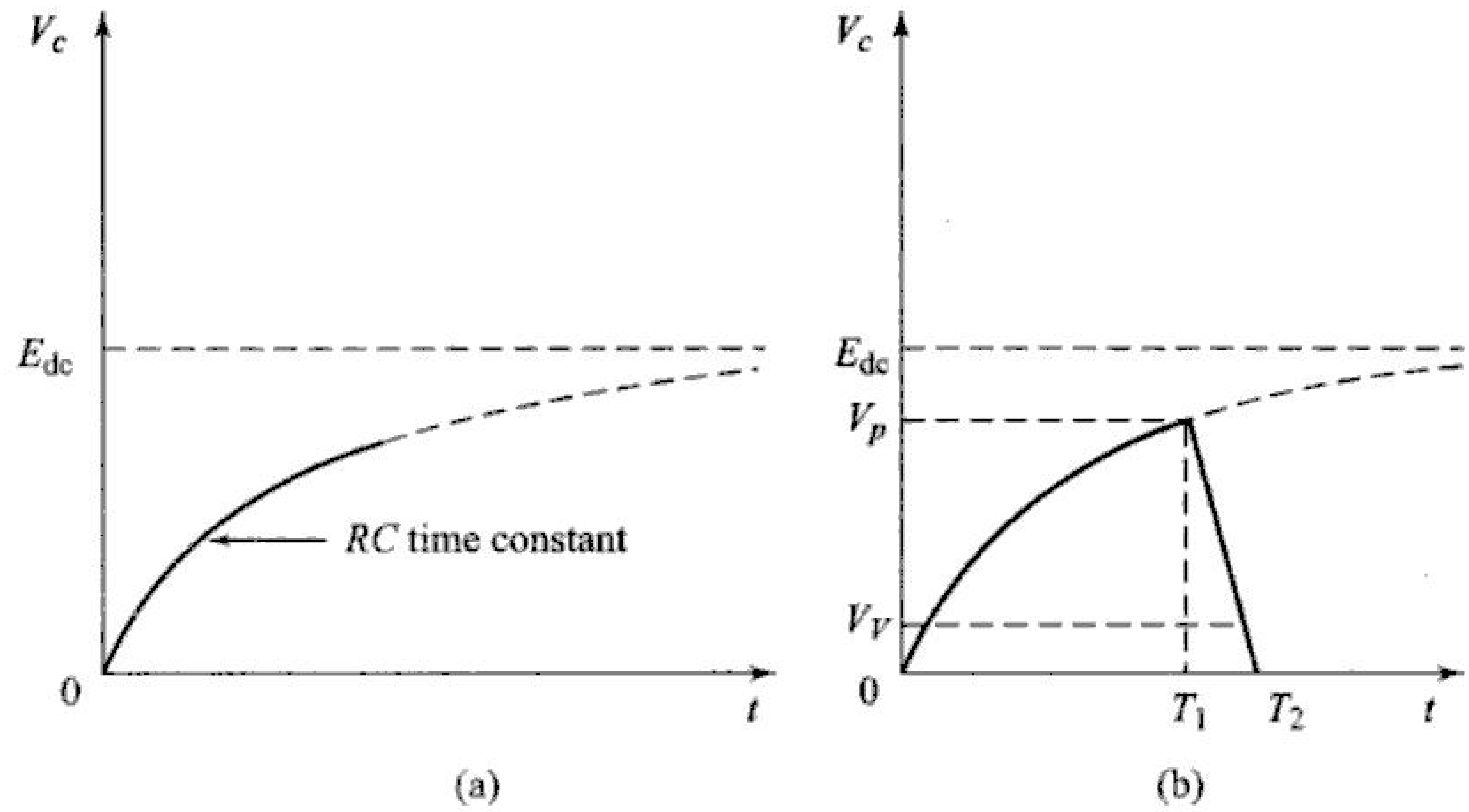

Fig. 3.19 *Capacitor waveform*

The capacitor will begin charging towards E_{dc} once again and the previous chain of events will repeat itself indefinitely as long as power is applied to the circuit. The result is a periodic sawtooth type waveform as shown in Fig. 3.20 (a).

To calculate the frequency of this waveform, we first calculate the period of one cycle. The length of one period, T_1, is essentially the time it takes for the capacitor to charge to V_p since the discharge time T_2 is usually relatively short. Thus $T \approx T_1$ and is given by

$$T = R.C.\ \log_e \left(\frac{E_{dc}}{E_{dc} - V_p} \right) \tag{3.12}$$

In most cases, $V_p \approx \eta\, E_{dc} + V_0$ and the period can be written as

$$T \approx R.C.\ \log_e \left[\frac{E_{dc}}{E_{dc}(1-\eta) - V_D} \right] \tag{3.13}$$

The small diode drop V_D can often be ignored if $E_{dc} > 10$ V, resulting in the more approximate expression,

$$T \approx R.C.\ \log_e \left[\frac{1}{1-\eta} \right] \tag{3.14}$$

Examination of Eq. 3.14 brings out an important point, namely that T is relatively independent of supply voltage E_{dc}. This characteristic is important when designing a stable oscillator circuit. The oscillator frequency is given by $1/T$ and can be obtained by using either of the three previous equations for T.

Pulse outputs The UJT relaxation oscillator circuit can also supply pulse waveforms. If the output is taken from B_1, the result is a train of pulses occurring during the discharge of the capacitor through the UJT emitter. The waveforms of V_{B_1} is illustrated in Fig. 3.20(b). The amplitude of the B_1 pulses is always less than $V_{p'i}$ but is greater for larger values of C. The voltage at B_1 during the UJT "off" time will be very small and is determined by the voltage divider formed by R_1, R_{BB} and R_2 [see Fig. 3.18(b)] That is,

$$V_{B1}\text{ (off)} = \left(\frac{R_1}{R_1 + R_{BB} + R_2}\right)E_{dc} \tag{3.15}$$

The rise time of the pulses at B_1 is very short (less than 1 μs), but the fall time depends on the values of C and R_1. A larger value of C or R_1 will cause a slower capacitor discharge and a longer fall-time.

If the output is taken at B_2, a waveform of negative going pulses is obtained as shown in Fig. 3.20(c). This results from the decrease in R_{B_1} when the UJT turns "on". This increases I_{B_2} which increases the drop across R_2 and thus reduces V_{B_2}. The amplitude of this pulses is usually about a couple of volts, but can be increased by increasing R_2.

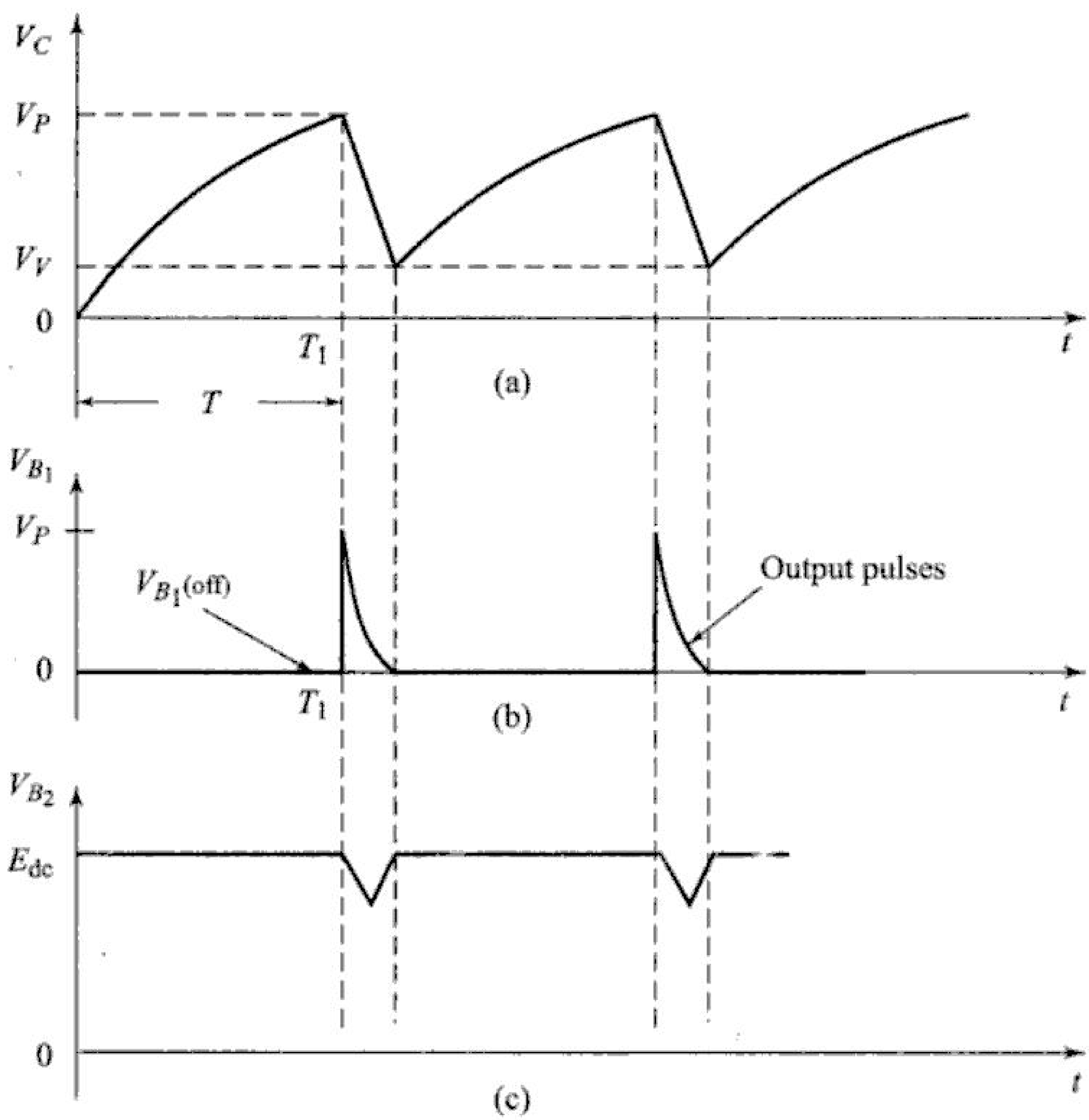

Fig. 3.20 *Waveform for UJT relation — oscillator*

The pulses at B_1 are usually the ones of most interest, they are of relatively high amplitude and are not affected by loading since they appear across a low-valued resistor R_1. These positive pulses are often used to trigger SCRs or other gated *PNPN* devices. The amplitude of these pulses is to some degree dependent on the value of C. For values of C of 1 μF or greater, the amplitude of the pulses is approximately equal to V_P (less than 2–3 V VJT drop). As C becomes smaller, the B_1 pulse decrease in amplitude. The reason for this is that the smaller value for C discharges a significant amount during the time that the UJT is making its transition from the "off" to "on" state. Thus, when the UJT finally reaches the "on" state, C has lost some of its voltage (V_p) and less voltage can appear across R_1 as the capacitor continues its discharge.

Varying the frequency The frequency of oscillations is normally controlled by varying the charging time constant RC. There are, however, limits on R. These limits are:

$$R_{\text{min}} = \frac{E_{\text{dc}} - V_v}{I_v} \tag{3.16}$$

$$R_{\text{max}} = \frac{E_{\text{dc}} - V_p}{I_p} \tag{3.17}$$

Keeping R between these limits will ensure oscillations. If R is greater than R_{max}, the capacitor never reaches V_p since the current through R is not large enough to both charge the capacitor and supply I_P to the UJT. The UJT will stay in the "off" state, and V_c will charge to a value just below V_P. (Fig. 3.21(a))

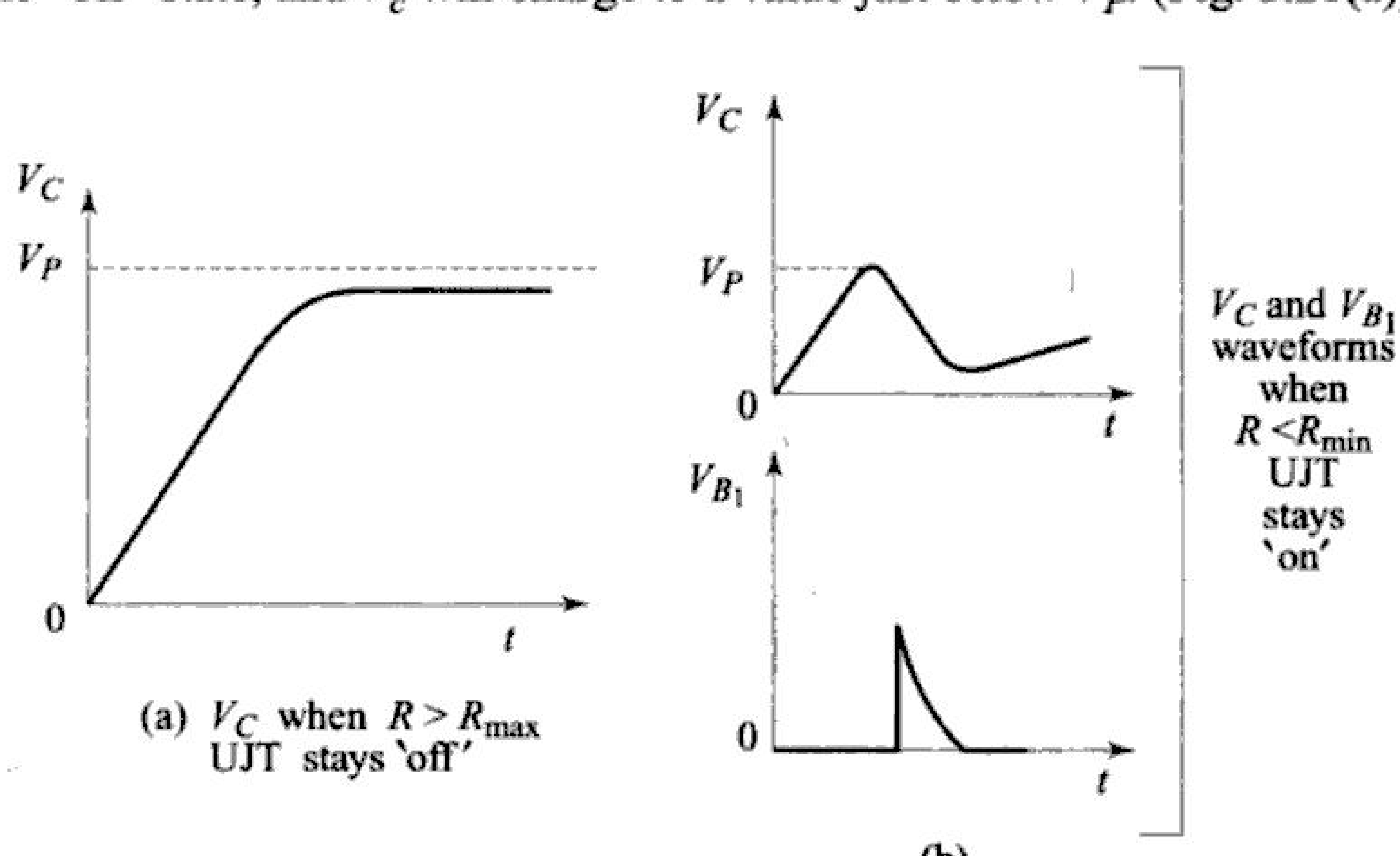

Fig. 3.21 ***(a)*** *V_c waveform when $R > R_{max}$;* ***(b)*** *V_c and R_{B_1} when $R<R_{min}$*

If R is smaller than R_{min}, the capacitor will reach V_P and discharge through the UJT, but the UJT will not turn "off" since the current through R is greater than the I_V needed to hold the UJT "on". The capacitor and V_{B_1} waveforms will consists of a single (Fig. 3.21(b)) representing one charge and discharge interval. This single pulse operation is sometimes used in time delay applications. The time delay is given by Eq. 3.12.

Examination of Eq. 3.16 indicates that to obtain a greater upper limit on frequency (a lower R_{min}) the value of I_V should be made larger. Similarly, to obtain a smaller lower limit on frequency (a higher R_{max}) the value of I_p should be made smaller. UJTs with I_v as high as 20 mA and I_p as low as 1 μA are presently available, resulting in a possible frequency range of 4000 : 1.

The frequency may also be varied by varying C. The lower limit on C is normally around 0.001 μF, while the upper limit depends on the size of R_1 (which limits on discharge current). In most applications of this circuit, the value of C is kept fixed and a variable resistor is used for R.

The temperature stability of the UJT relaxation oscillator frequency is normally very good. This is because η varies only slightly with temperature and the only variation in V_p is due to the small decrease in VD (2 mV/°C) with temperature. Its stability of frequency with variations in temperature and supply voltage coupled with its simplicity and low cost make the UJT oscillator a popular circuit for timing and pulsing applications.

3.6.4 The UJT as an SCR Trigger

The circuit examined in the previous section is often used as the gate trigger source in SCR applications. The basic circuit is shown in Fig. 3.22 when the B_1 pulse output is used to trigger the SCR a predetermined interval of time after the

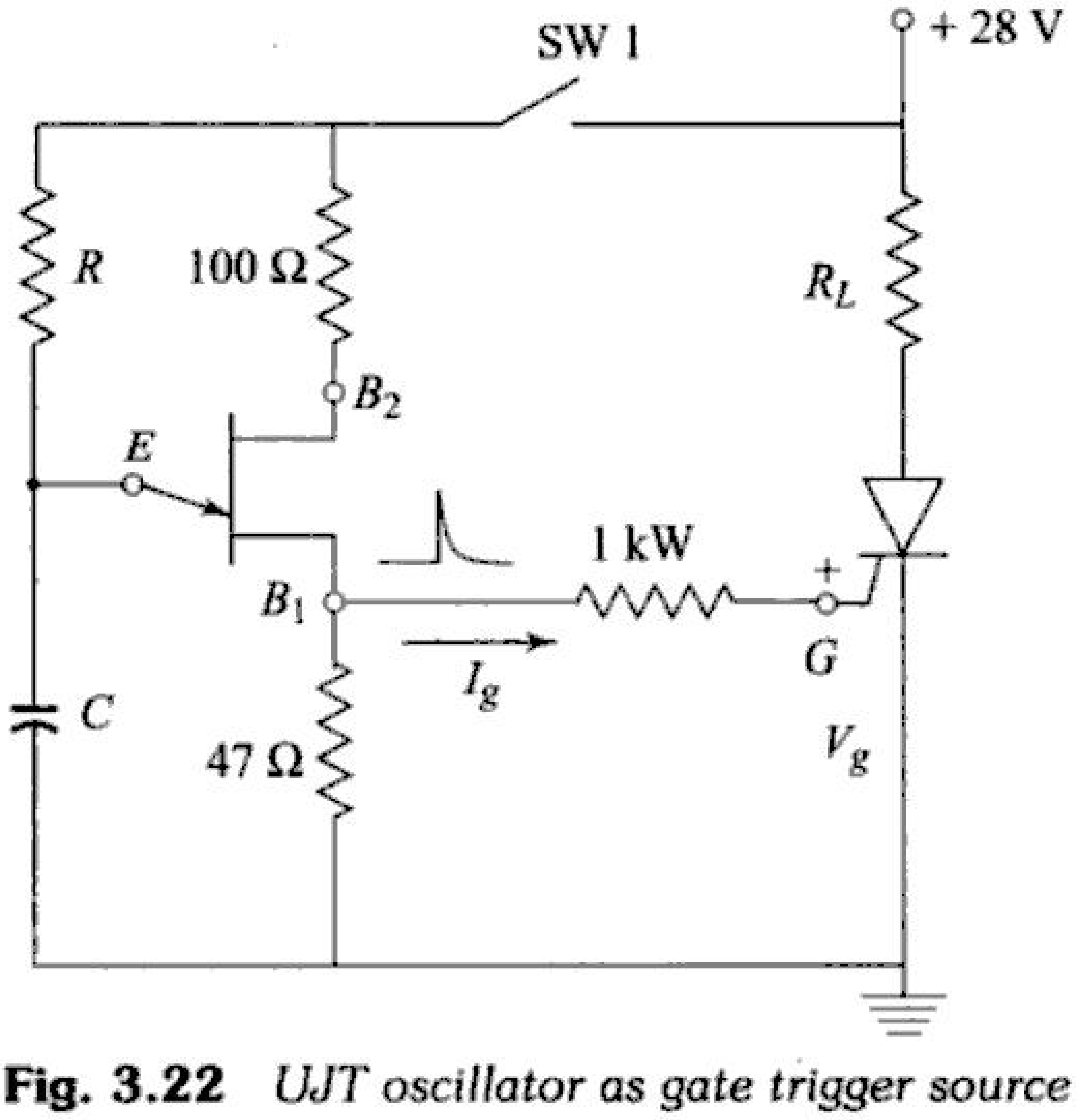

Fig. 3.22 *UJT oscillator as gate trigger source*

switch is closed. That is, the first B_1 pulse occurs T seconds after the 28 V is supplied to the UJT circuit. After the SCR has been triggered "on," subsequent pulses at its gate have no effect.

An important design consideration in this type of circuit concerns premature triggering of the SCR. The voltage at B_1 when the UJT is "off" (Eq. 3.15) must be smaller than the voltage needed to trigger the SCR, otherwise the SCR will be triggered immediately upon switch closure. Thus, we have the requirement

$$V_{B_1}(\text{off}) < (I_g \times 1\ \text{k}\Omega + V_g) \tag{3.18}$$

3.6.5 Synchronized UJT-Triggering (Ramp Triggering)

Synchronized UJT triggering circuit is shown in Fig. 3.23. The diode bridge $D_1 - D_4$ rectifies a.c. to d.c. Resistor R_s lowers E_{dc} to a suitable value for the zener diode and UJT. The zener diode D_z is used to clip the rectified-voltage to a fixed voltage V_z. This voltage V_z is applied to the charging circuit RC. Capacitor C charges through R until it reaches the UJT trigger voltage V_p. The UJT then turns "on" and C discharges through the UJT emitter and primary of the pulse-transformer. The windings of the pulse transformer have pulse voltages at their secondary terminals. Pulses at the two secondary windings feed the same inphase pulse to two SCRs of a full wave circuit. SCR with positive anode voltage would turn ON. Rate of rise of capacitor voltage can be controlled by varying R. The firing angle can be controlled up to about 150°. This method of controlling the output power by varying charging resistor R is called as ramp control, open loop control or manual control.

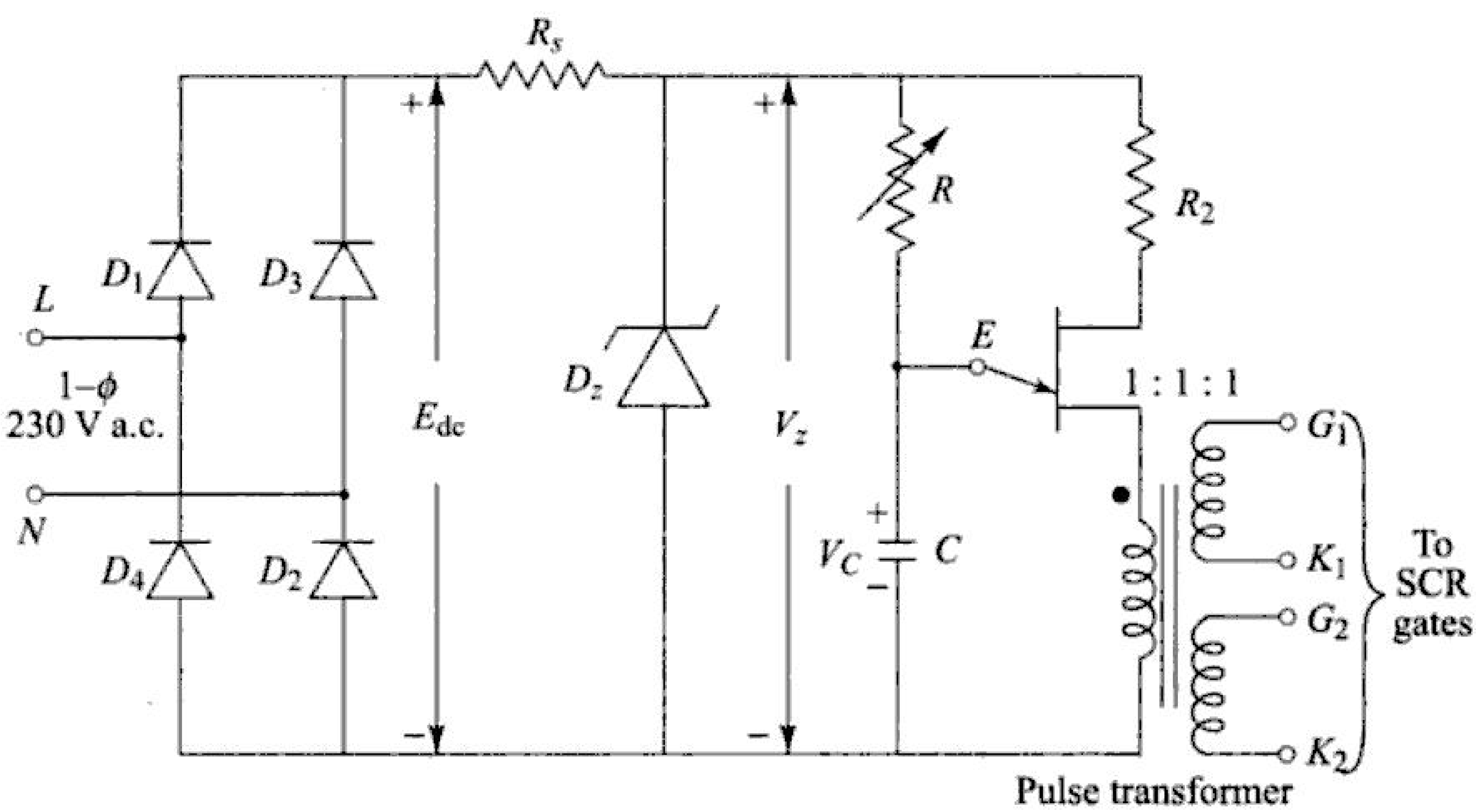

Fig. 3.23 *Synchronized UJT trigger-circuit*

As the zener diode voltage V_z goes to zero at the end of each half cycle, the synchronization of the trigger circuit with the supply voltage across SCRs is achieved. Thus the time t, equal to α/ω, when the pulse is applied to SCR for the first time, will remain constant for the same value of R. The various voltage waveforms are shown in Fig. 3.24.

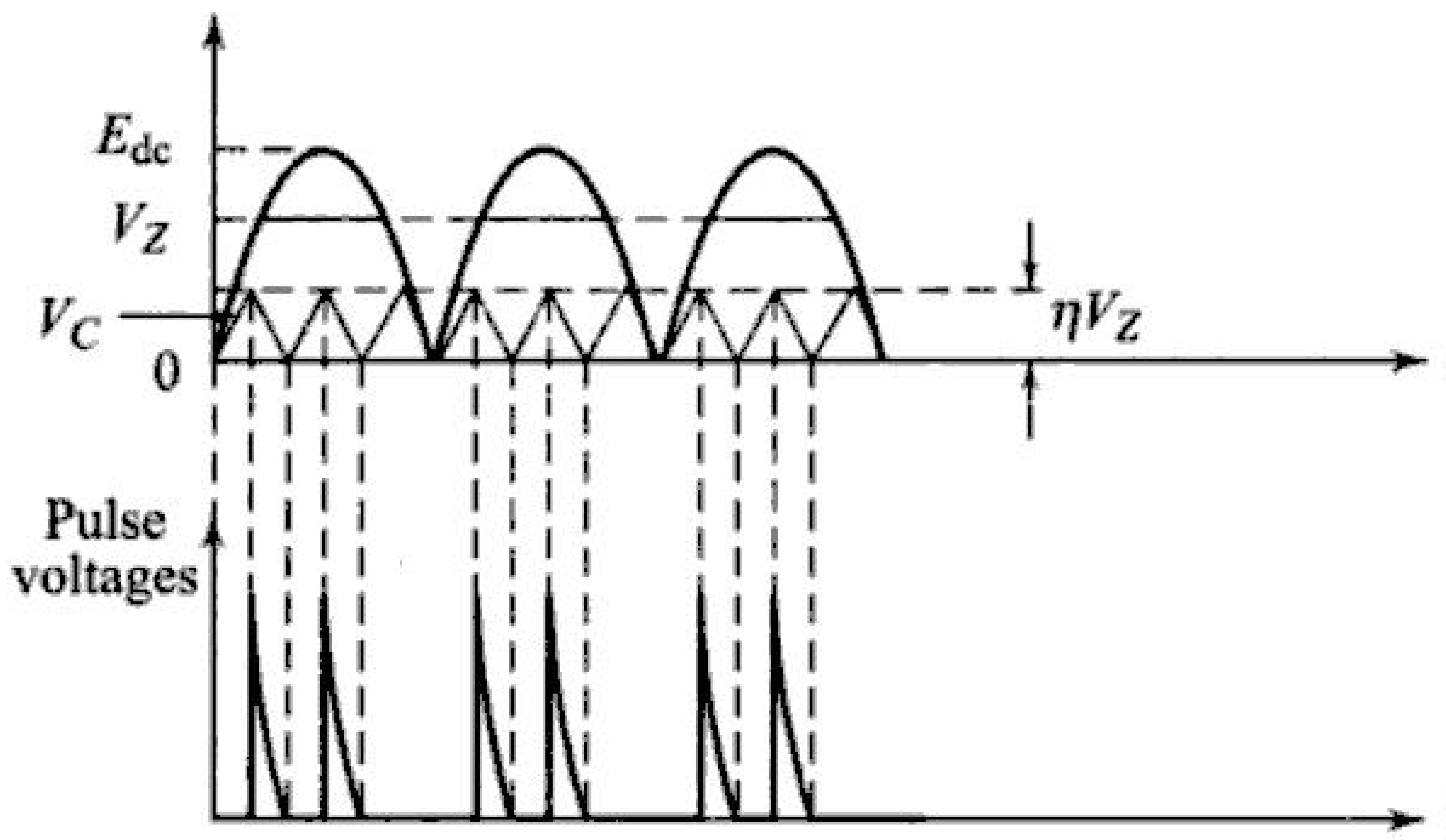

Fig. 3.24 *Generation of output pulses*

SOLVED EXAMPLES

Example 3.2 If $R_E = 1$ kΩ and $I_V = 5$ mA, determine the value of V_{EE} which will cause the UJT to turn "off."

Solution: At the valley point, $V_E = V_V = 2$ V and $I_E = I_V = 5$ mA.
Thus, using KVL, $V_{EE} = I_E R_E + V_E = 7$ V

is the value of V_{EE} below which the UJT will switch back to the "off" state.

Example 3.3 Design a UJT relaxation oscillator using UJT 2N2646, for triggering an SCR. The UJT has the following characteristics.

$$\eta = 0.7, I_P = 50\ \mu\text{A}, V_v = 2\text{V}, I_V = 6\text{ mA},$$

$$V_{BB} = 20\text{ V}, R_{BB} = 7\text{ K}\Omega, I_{E0} = 2\text{ mA}.$$

Also, determine the limits for the output frequency of the oscillator.

Solution: Let us assume $C = 0.1\ \mu$F.

$$\therefore\quad R_{max} = \frac{20(1-0.7)}{50} \times 10^6 = 120\text{ k}\Omega. \quad \text{and} \quad R_{min} = \frac{20-2}{6\times 10^{-3}} = 3\text{ k}\Omega.$$

The approximate value of R_2 is given by $R_2 = \dfrac{10^4}{\eta V_{BB}}$

$$\therefore\qquad R_2 = \frac{10^4}{0.7\times 20} = 714.29\ \Omega.$$

Figure 3.25 shows the *PNPN* structure and the circuit symbol for the PUT. The anode (A) and cathode (K) are the same as for any *PNPN* device. The gate (G) is connected to the *N*-region next to the anode. Thus, the anode and gate constitute a *P-N* junction. It is this *P-N* junction which controls the "on" and "off" states of the PUT. The gate is usually positively biased relative to the cathode by a certain amount, V_g. When the anode voltage is less than V_g, the anode-gate junction is reverse-biased and the *PNPN* device is in the "off" state, acting as an open-switch between anode and cathode. When the anode voltage exceeds V_g by about 0.5 V, the anode gate junction conducts, causing the *PNPN* device to turn "on" in the same manner as does forward biasing the gate cathode junction of an SCR. In the "on" state, the PUT acts like any *PNPN* device between anode and cathode (low resistance and $V_{AK} \approx$ 1V). The PUT is also referred to as a complementary SCR (CSCR).

The normal bias arrangement for the PUT is shown in Fig. 3.26. The voltage divider, R_1 and R_2 sets the voltage at the gate V_g. Note that R_1 and R_2 are external to the device and can therefore be chosen to produce any desired value of V_g. The anode cathode bias is provided by E_{dc}. As long as $E_{dc} < V_g$, the device is "off" with $I_A = 0$ and all of E_{dc} present across the anode cathode ($V_{AK} = E_{dc}$). The "off" state is summarized in part (a) of the figure.

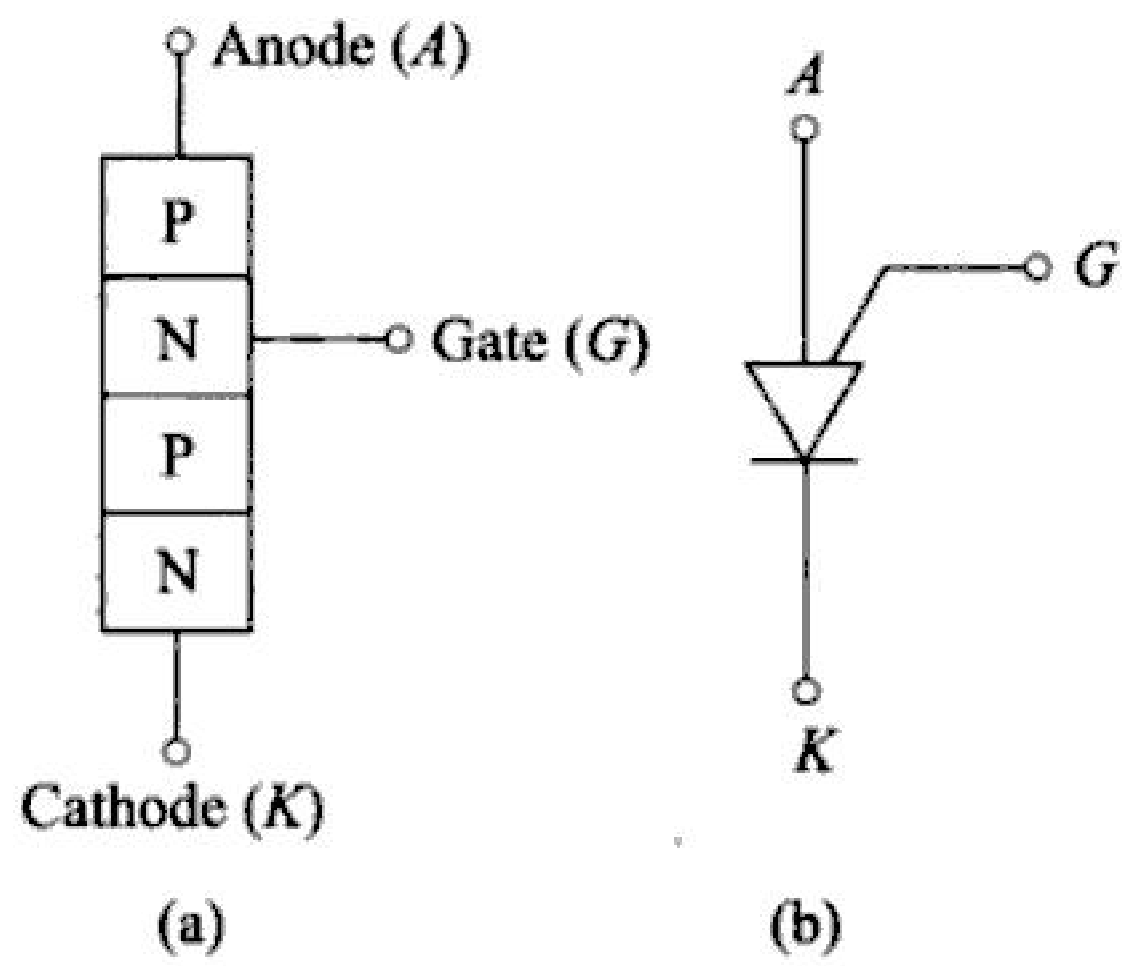

Fig. 3.25 ***(a)*** *PUT structure* ***(b)*** *circuit symbol*

If E_{dc} is increased to about 0.5V greater than the V_g bias value, the device turns "on". In other words, the peak-point voltage V_p for the PUT is given by

$$V_p = V_g = 0.5 \text{ V} \tag{3.19}$$

In the "on" state, the anode–cathode voltage, V_{AK}, drops to $\approx$ 1V and the anode current, I_A, is essentially equal to E_{dc}/R_1 being limited by R. In addition, V_g drops to a very low value ($\approx$ 0.5 V) since R_2 is now shunted by the "on" *PNPN* structure. The PUT will remains in the "on"-state until the anode current is decreased below the valley-current, I_V. The "on" state is summarized in part (b) of the figure.

3.7.1 PUT Relaxation Oscillator

Figure 3.27 shows the relaxation oscillator, whose operation is very similar to the UJT oscillator. The various circuit waveforms are shown in part (b) of the figure. These waveforms reveal the following important points:

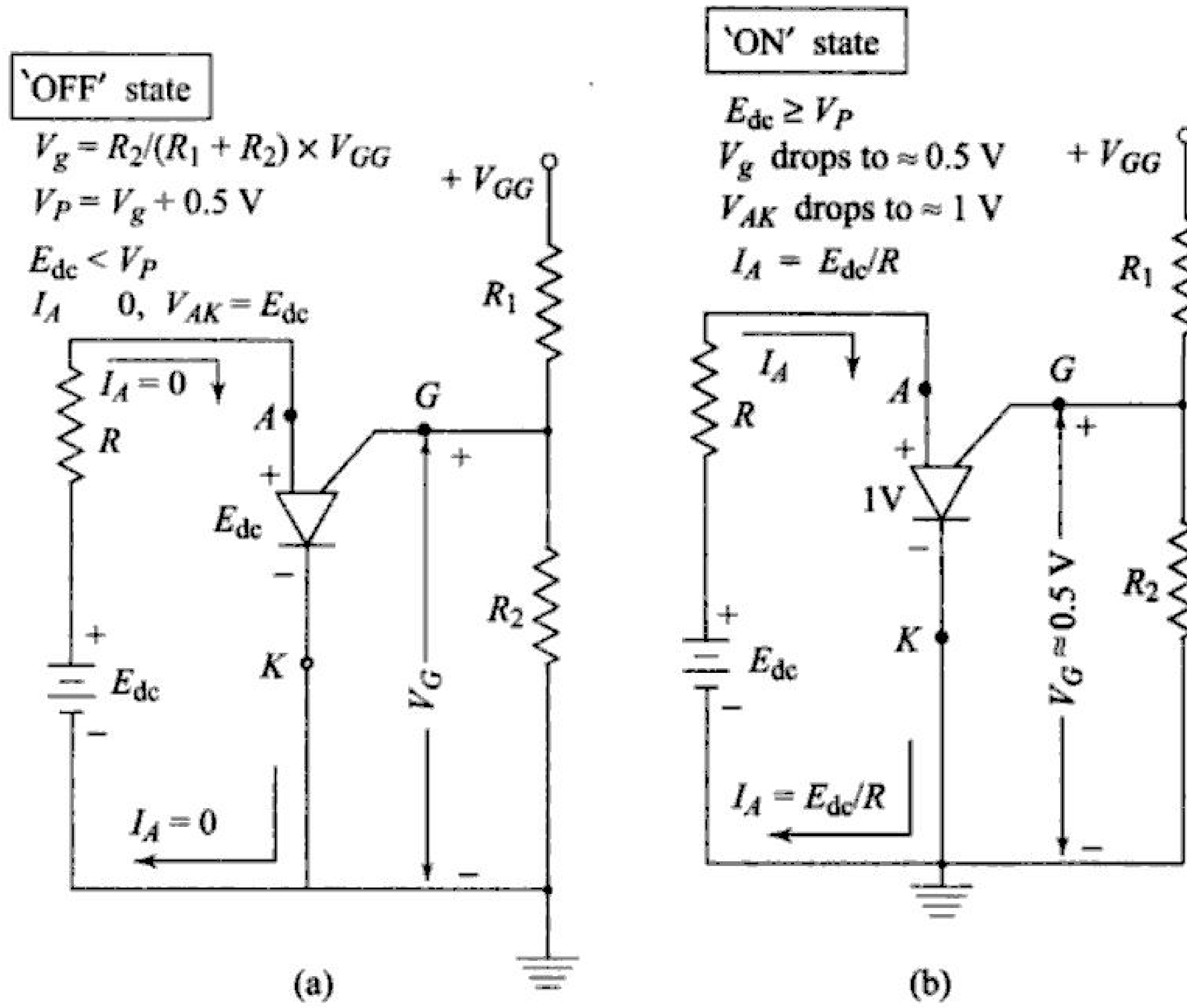

Fig. 3.26 *(a) Circuit with PUT in "off" state* *(b) PUT in "on" state*

(a) The capacitor voltage charges towards the 20 V supply voltage E_{dc} through the 10 kΩ resistor R until it reaches $V_p = 10.5$ V. At that point, the PUT turns "on" and the capacitor discharges rapidly through the PUT and the 100 Ω resistor R_s. The trigger voltage of 10.5 V is set by the voltage divider consisting of the two 20 kΩ resistors (R_1 and R_2) which bias V_g at + 10 V.

(b) The voltage at G remains at 10 V, while the capacitor charges and the PUT is "off." When the PUT turns "on," V_g drops to approximately zero. After the capacitor discharges, the PUT turns "off" (assuming current through 10 kΩ is less than I_V) and V_g returns to 10 V. This results in a negative going pulse at G.

(c) A positive pulse is produced across the 100 Ω resistor R_s as the capacitor discharges. The amplitude of this pulse is slightly lower than the capacitor peak voltage due to the anode cathode "on" voltage of ≈ 1V. The period of oscillator waveforms can be calculated from

$$T = R.C.\log_e\left(\frac{E_{dc}}{E_{dc} - V_p}\right) \tag{3.20}$$

The frequency is simply $1/T$. Note that the above expression and the expression for the conventional UJT oscillator are exactly the same. The R_{min} and R_{max} limits for the charging resistor are determined just as they were for the UJT.

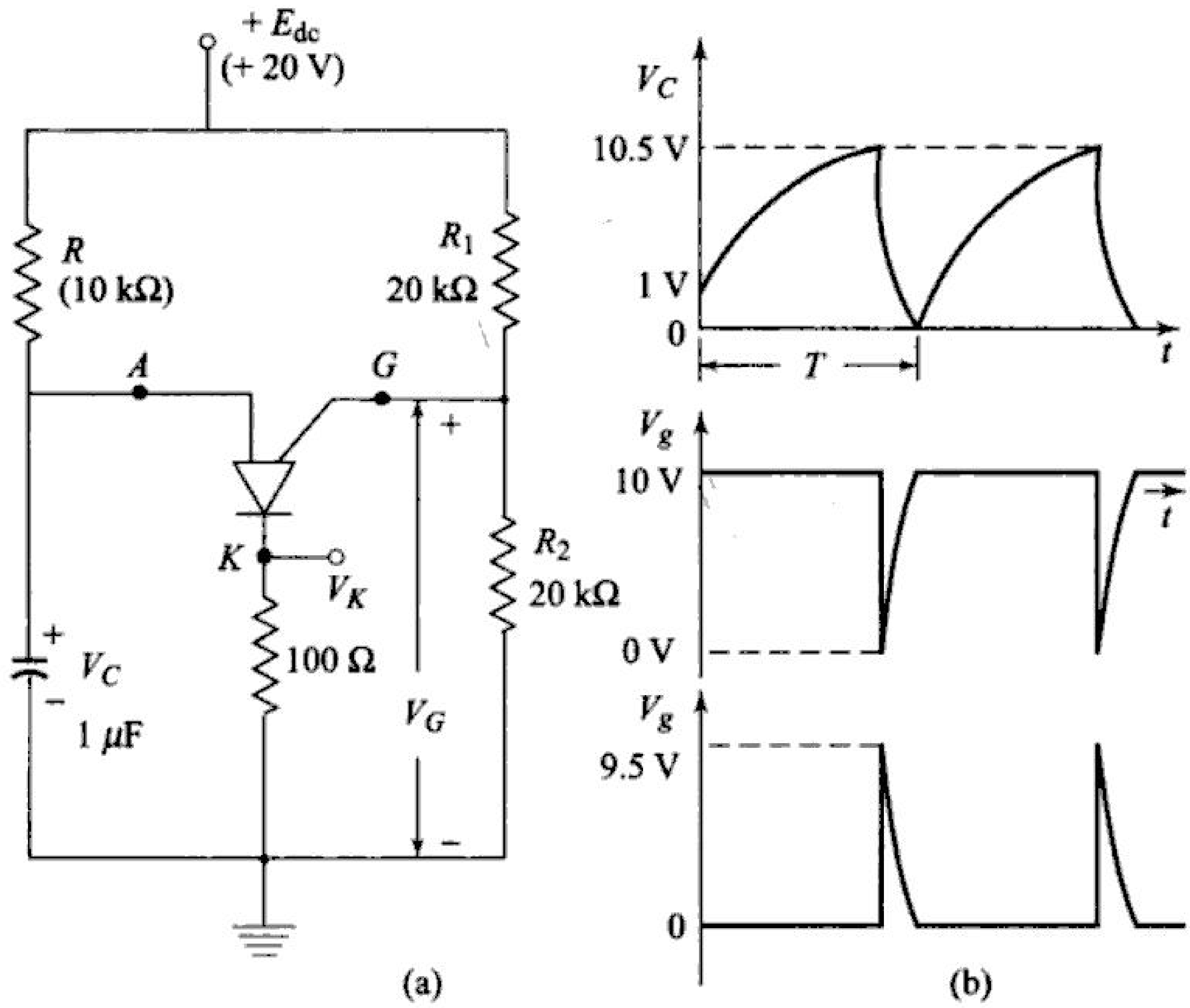

Fig. 3.27 ***(a)*** *PUT oscillator* ***(b)*** *circuit waveforms*

3.7.2 Advantages of the PUT

The PUT operation, though similar to the conventional UJT, has several important advantages over its predecessor. First, the switching voltage is easily varied by changing V_g through the voltage divider ratio. Second, the PUT can operate at low voltages (down to 3 V) making it compatible with integrated circuits.

Probably, the most important advantage of the PUT is its low peak point current, I_p. Recall from our earlier discussion of the UJT oscillator that the maximum charging resistor which could be used dependent on I_p. The PUT can be made to have a very low I_P (0.1 μA) by using large resistors for the gate bias voltage divider with a lower I_p, it is possible to use a much larger charging resistor. This is distinct advantage in long time-delay applications since a larger R would reduce the required value of C. The following example illustrates.

Figure 3.28 is a PUT time delay circuit similar to its UJT counterpart. Note that the voltage divider resistors are very large so that the PUT's I_p will be very low. Since $R_g = R_1 \parallel R_2 \approx 1$ M Ω, we can expect an I_p of around 0.1 μA. The value of V_g is easily seen to be

$$V_g = \frac{3\text{ M}\Omega}{5\text{ M}\Omega} \times 10\text{ V} = 6\text{ V}.$$

$$R_{\max} = \frac{E_{dc} - V_p}{I_p} = \frac{(10 - 6)\ \text{V}}{1.1\ \mu\text{A}} = 40\ \mu\Omega$$

To be conservative, R should be kept well below $R_{\max}$ to ensure proper operation. The value of 20 mΩ is chosen. The value of C can now be found by satisfying

$$RC = 1713\ \text{s} \quad \therefore \quad C = \frac{1713}{R} = \frac{1713}{20 \times 10^6} = 85.7 \times 10^{-6}\text{F} = 85.7\ \mu\text{F}$$

Thus, a 100 μF capacitor can be used, and R can be varied to obtain the required delay.

If the same circuit were designed using a conventional UJT, the values of R and C might be 1 MΩ and 2000 μF. The higher I_p of the UJT results in a lower $R_{\max}$.

Solved Example

Example 3.5 Design a free-running relaxation oscillator using a PUT to operate at a frequency of 5 to 50 Hz. DC supply is 12 V and I_p is 80 mA. It is used for triggering an SCR which will require 8 μs charge rate pulse. The voltage drop across PUT is 1 V.

Solution: Let us assume $R_s = 39\ \Omega$.

Since $$T = R_s C = 8\ \mu\text{s} \quad \therefore \quad C = \frac{8 \times 10^{-6}}{39} = 0.21\ \mu\text{F}$$

The peak triggering current of 80 mA determines V_P, namely,

$$V_P = I_P R_s + 1\text{V} = (80\ \text{mA})\,(39\ \Omega) + 1 = 4.12$$

where 1 V is the approximate PUT on-state voltage.

Now, $$V_P = \eta E_{dc} + V_D$$

Neglecting V_D,

$$V_P = \eta E_{dc} \quad \therefore \quad \eta = \frac{V_P}{E_{dc}} = \frac{4.12}{12} = 0.34.$$

Now, the timing resistor R can be found from Eq. (3.20),

$$\therefore \quad R_{\max} = \frac{T_{\max}}{C \log_e\left(\dfrac{E_{dc}}{E_{dc} - V_p}\right)} = \frac{1}{C \log_e\left(\dfrac{E_{dc}}{E_{dc} - V_p}\right) f_{\min}}$$

$$= \frac{1}{0.21 \times 10^{-6} \times \log_e\left(\dfrac{12}{12 - 4.12}\right) \times 5} = 2.26\ \text{M}\Omega$$

and $$R_{\min} = \frac{1}{0.21 \times 10^{-6} \times 50 \times \log_e\left(\dfrac{12}{12 - 4.12}\right)} = 0.23\ \text{M}\Omega$$

The maximum anode current occurs at the maximum frequency when R is a minimum:

$$I_{V(\max)} \approx \frac{E_{dc}}{R_{\min}} \approx \frac{12\times10^{-6}}{0.23} \approx 52.17\,\mu\text{A}$$

$I_{V(\min)}$ of the 2N6027 is 70 μA for $I_g = 1$ mA which should allow adequate safety margins. Therefore, to find R_1 and R_2, the following equations must be solved.

For $$\eta = 0.34, \qquad I_g = \frac{2\eta E_{dc}}{R_g}$$

$$1\times10^{-3} = \frac{2\times12\times0.34}{R_g} \qquad \therefore \quad R_g = 8.16\ \text{k}\Omega$$

Now, $$\eta = \frac{V_p}{E_{dc}} = \frac{R_2}{R_1 + R_2}$$

The solutions for R_1 and R_2 are:

$$R_1 = \frac{R_g}{\eta} = \frac{8.16K}{0.34} = 24\ \text{k}\Omega. \quad \text{and} \quad R_2 = \frac{R_g}{1-\eta} = \frac{8.16K}{1-0.34} = 12.36\ \text{k}\Omega.$$

3.8 PHASE CONTROL USING PEDESTAL-AND-RAMP TRIGGERING

Figure 3.29 shows the circuit for ramp-and-pedestal triggering of two thyristors connected in antiparallel for controlling power in an ac load. Ramp and pedestal triggering is an improved version of synchronized-UJT-oscillator triggering. The various voltage-waveforms are shown in Fig. 3.30.

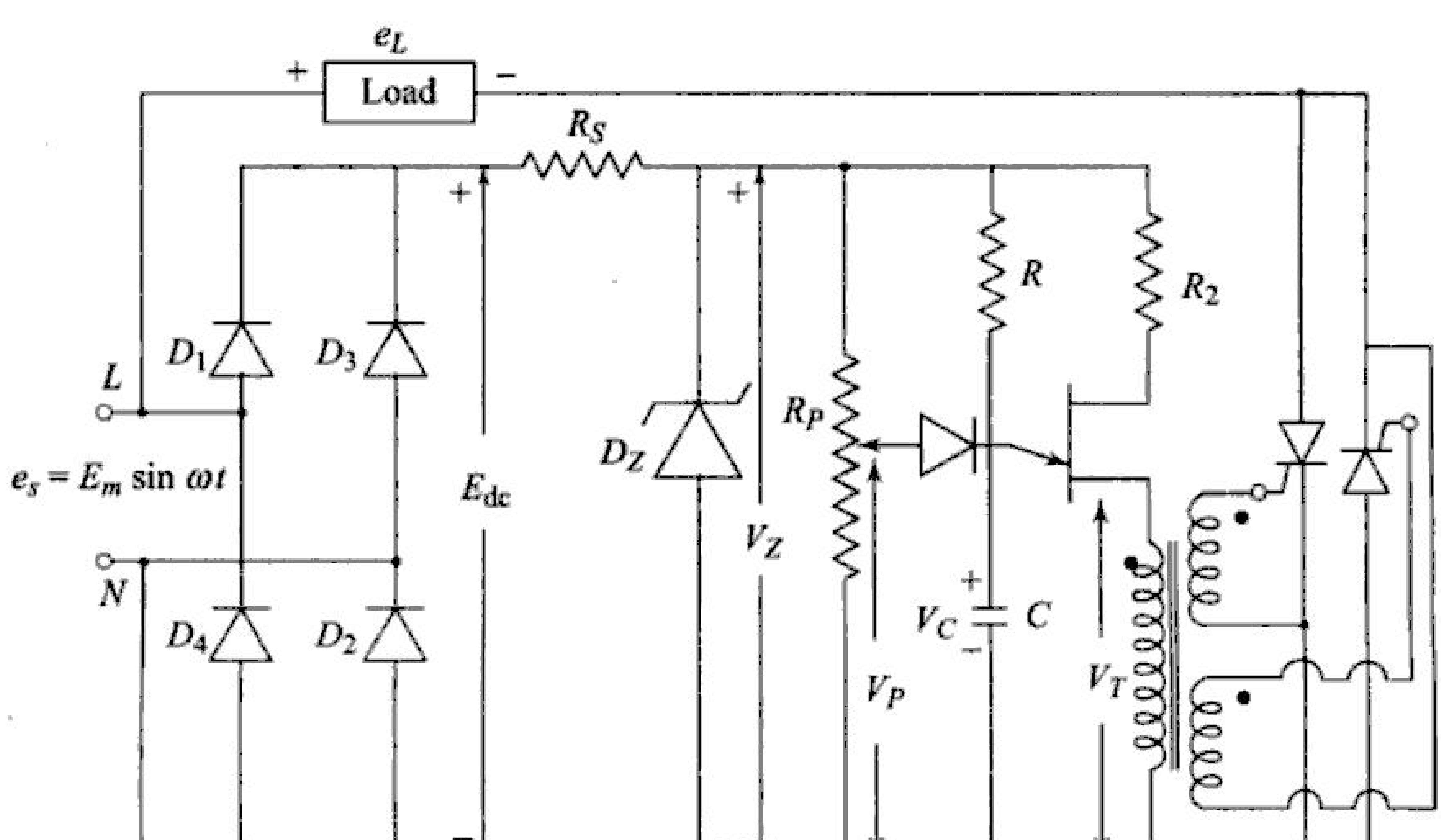

Fig. 3.29 *Ramp and pedestal trigger circuit for a.c. load*

Zener-diode voltage, V_z, is constant at its threshold-voltage. R_p acts as a potential divider. Wiper of R_P controls the value of pedestal voltage V_p. Diode D allows C to be quickly charged to V_p through the low-resistance of the upper portion of

R_p. The setting of wiper on R_p is such that, this value of V_p is always less than the UJT firing point voltage ηV_z. When wiper setting is such that V_P is small (See Fig. 3.3(a), voltage V_z charges C through R. When this ramp voltage V_C reaches ηV_z, UJT fires and voltage V_T, through the pulse transformer, is transmitted to the gate circuits of both thyristors T_1 and T_2. During first positive half-cycle, SCR T_1 is forward biased and is therefore, turned-on. After this, V_c reduces to V_P and then to zero at $\omega t = \pi$. As V_c is more than V_P, during the charging of capicitor C through charging resistor R, diode D is reverse-biased. Thus, V_P does not effect in anyway the discharge of C through UJT emitter and primary of pulse transformer. From period 0 to π, SCR T_1 is forward biased and is turned-on. From π to 2π, T_2 is turned-on. In this manner, load is subjected to alternating e_L, as shown in Fig. 3.30.

With the setting of wiper on R_P pedestal voltage V_P on C can be adjusted.

With low pedestal voltage across C, ramp charging of C to η V_z takes longer time (Fig. 3.30(a)), and firing angle delay is, therefore, more and output voltage is low. With high pedestal on C, voltage-ramp charging of C through R reaches η V_z faster, firing angle delay is smaller (Fig. 3.30(b)) and output voltage is high. This shows that output voltage is proportional to the pedestal voltage.

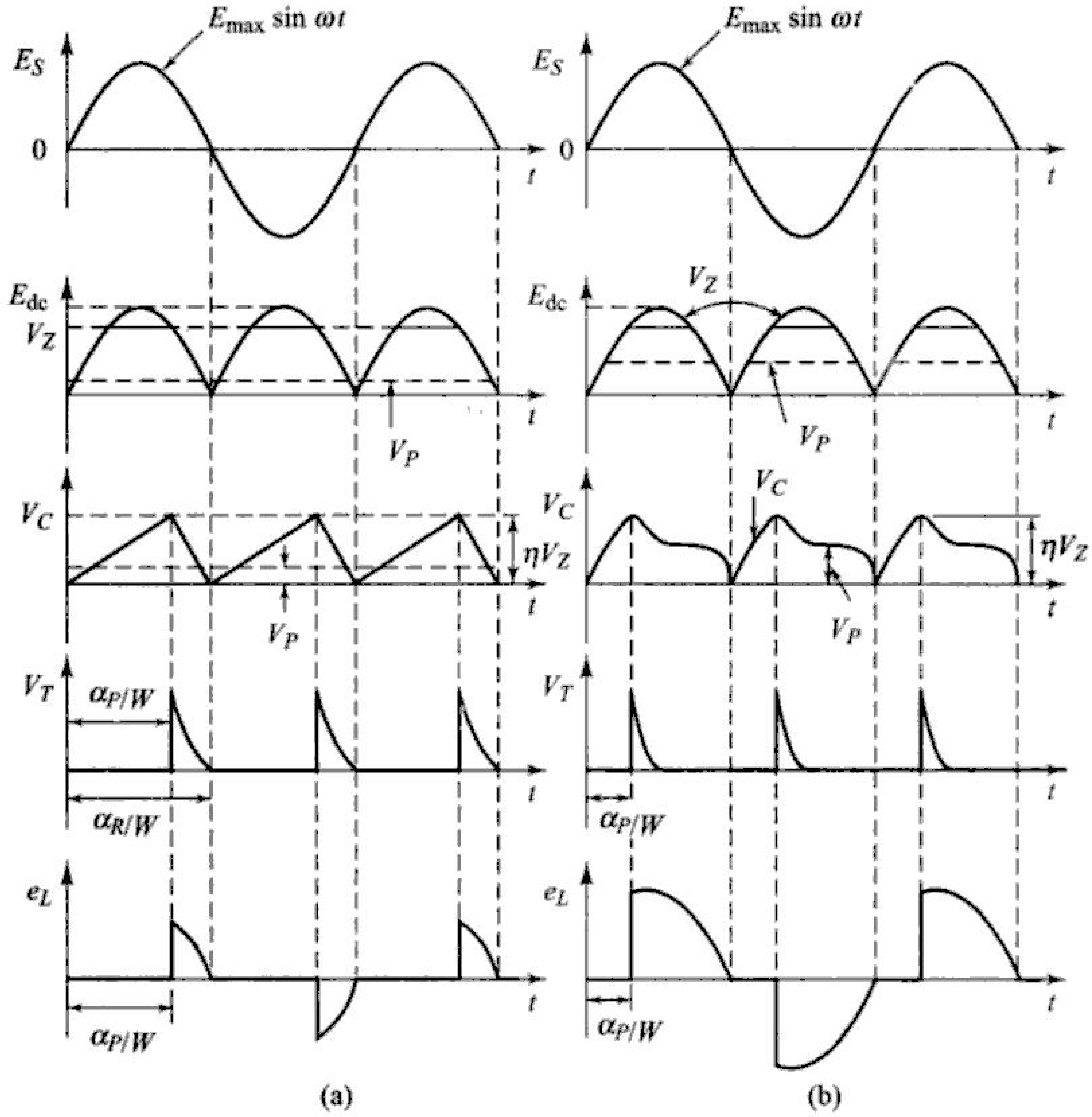

Fig. 3.30 *Waveform for ramp and pedestal control*

The time T required for capacitor to charge from pedestal voltage V_P to ηV_z can be obtained from the relation

$$\eta V_z = V_P + (V_z - V_P)\,(1 - e^{-T/RC})$$

Note that $(V_z - V_P)$ is the effective voltage that charges C from V_P to ηV_z. From above,

$$T = RC \ln \frac{V_z - V_P}{V_z(1-\eta)} \tag{3.21}$$

and the firing angles are given by

$$\alpha_p = \omega R.C \ln \frac{V_z - V_p}{V_z(1-\eta)} \tag{3.22}$$

and

$$\alpha_R = \omega \cdot RC \ln \frac{1}{1-\eta} \tag{3.23}$$

where ω is the input frequency and η is the intrinsic stand off ratio of the UJT.

3.9 MICROPROCESSOR INTERFACING TO POWER THYRISTOR

Microprocessor/microcontrollers are used to control the firing angle of the thyristors. In order to design a gate interface circuit, both the logic and thyristor gate requirements must be specified. Figure 3.31 shows the microprocessor interface circuit for power thyristor. Microprocessor used here has the following specifications: $V_{CC} = 5$ V

$V_{OH} = 2.4$ V, $I_{OH} = 0.3$ mA

$V_{OL} = 0.4$ V, $I_{OL} = 1.8$ mA

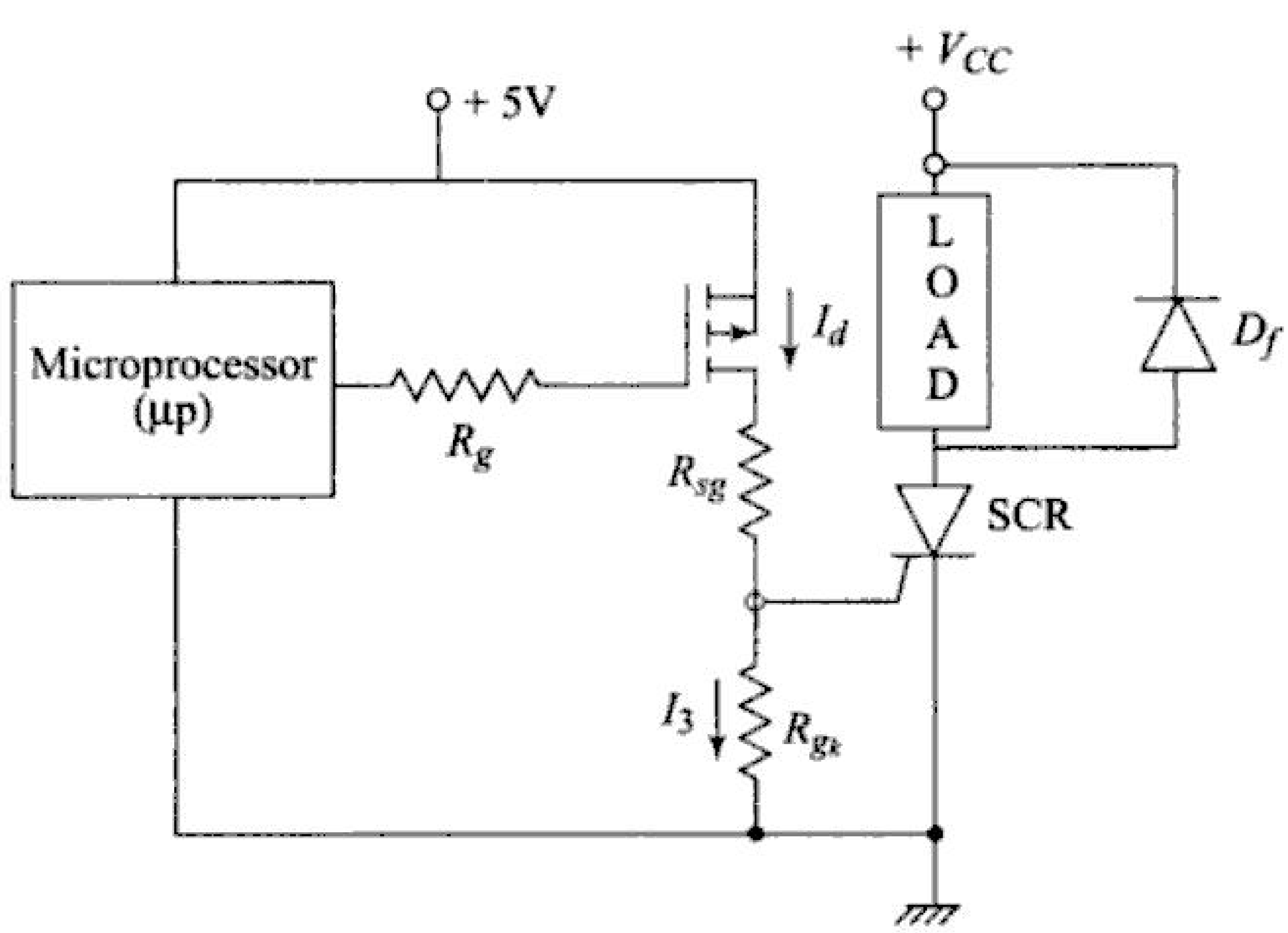

Fig. 3.31 *μp interfacing to SCR*

With these specifications, microprocessor cannot directly drive the power-thyristor. Therefore power interfacing circuitry is used. As shown, *p*-channel MOSFET is used as a interfacing device. MOSFET used has the following specifications: $V_{TH} = 3$ V, $I_d = 0.5$ A, $C_{gs} = 400$ pF

$$R_{ds(on)} = 10 \text{ ohms}$$

(i) Selection of Resistance Rg:

Resistor R_g limits the charging current of the capacitance C_{gs} and also decides the turn-on time of the MOSFET. From Fig. 3.31,

$$R_g = \frac{(V_{CC} - V_{OL})}{I_{OL}} \text{ ohms} = \frac{(5 - 0.4)}{1.8} = 2.7 \text{ k}\Omega$$

The MOSFET will not turn-on until C_{gs} has charged to 3V or, with a 5V supply, approximately one R-C time constant, that is

$$t_{\text{delay}} = R_g \cdot C_{gs} = 2.7 \times 10^3 \times 400 \times 10^{-12} = 1 \ \mu\text{sec}$$

(ii) Section of resistance R_{gk} and R_{sg}:

The MOSFET must provide the thyristor gate current and the current through resistor R_{gk} when the gate is at 3V.

When $R_{gk} = \infty$, R_{sg} has the maximum value and is given by

$$R_{sg} \le \frac{V_{CC} - V_{GT} - I_{GT} \cdot R_{ds(on)}}{I_{GT}} \ \Omega \ \le \frac{5 - 3 - 75 \times 10^{-3} \times 10}{75 \times 10^{-3}} = 16.6 \ \Omega$$

Choose $R_{sg} = 10$ ohms.

Since resistor R_{gk} provides a low cathode-to-cathode impedance in the off-state, hence improves SCR noise immunity.

When $V_{GT} = 3$V, $I_d = \dfrac{V_{CC} - V_{GT}}{R_{ds(on)} + R_{sg}} = 100$ mA

But $\quad I_d = I_g + I_3$

$\therefore \quad 100 \text{ mA} = 75 \text{ mA} + I_3 \quad \therefore \quad I_3 = 25$ mA

$$\therefore \quad R_{gk} = \frac{V_{GT}}{I_d - I_{GT}} = \frac{3}{25 \times 10^{-3}} = 120 \ \Omega$$

After turn-on, the gate voltage will be about 1 V. Therefore, the MOSFET current will be 200 mA.

$\therefore \ I^2 R_{sg} = (200 \text{ mA})^2 \times 10 = 0.4$ W $\quad \therefore \quad$ Select $R_{sg} = 10 \ \Omega/1$ W

REVIEW QUESTIONS

3.1 Explain the basic requirements for the successful firing of thyristor in detail.

3.2 With the help of neat diagram, explain the operation of resistance firing circuit. Also, draw and explain the associated waveforms. Also, for the same circuit, show that firing angle delay is proportional to the variable resistance.

3.3 Explain with the help of neat circuit diagram, the use of pulse-transformer in triggering circuits.

3.4 Explain in brief, the prime requirement of a trigger pulse transformer.

3.5 Under what circumstances should one consider using an optoisolator?

3.6 What advantages do opto-isolators have over electromechanical relays?

3.7 Why can't the circuit of Fig. 3.11 produce a trigger angle greater than 90°?

3.8 The circuit of Fig. 3.12 is adjusted to have a trigger angle of 90°?

(a) Sketch e_L, V_{AK}, and V_c.

(b) Sketch e_L if R_V is decreased.

(c) Sketch e_L, if C_1 is increased

(d) Sketch e_L if the amplitude of e_s is doubled.

3.9 Suppose the load voltage in Fig. 3.13(a) always has a trigger angle of 0° regardless of the setting of R. Which of the following could be a cause of this malfunction? Explain your choice (s):

(a) C_1 is open.

(b) SCR is shorted between anode and cathode.

(c) One of the diodes in the bridge is shorted.

(d) R is open.

(e) The four layer diode is shorted.

3.10 After the UJT is turned "on," what happens to the value of R_{B1}? How can the value of V_P be varied for a given UJT? How is the UJT turned- "off"?

3.11 Consider the circuit of Fig. P.3.11. The oscillator is suppose to produce pulses at a rate of 10 kHz. When power is applied to the circuit, however, the circuit fails to osciliate. The technician testing the circuit notices that when the power is turned-off, the circuit temporarilly oscillates as the power-supply voltage drops to zero. Explain these observations and determine what is wrong with the circuit. How should the circuit be modified for proper operation?

3.12 Suppose that when the switch is closed in Fig. P. 3.12, the motor goes on instantly (no time delay). Which of the following reasons could be cause for the malfunction? (There may be more than one possible answer). Explain each choice:

(a) The capacitor is shorted.

(b) R_1 is too large.

(c) The supply voltage is too large.

(d) The SCR is too-sensitive.

(e) The UJT is shorted from B_2 to B_1.

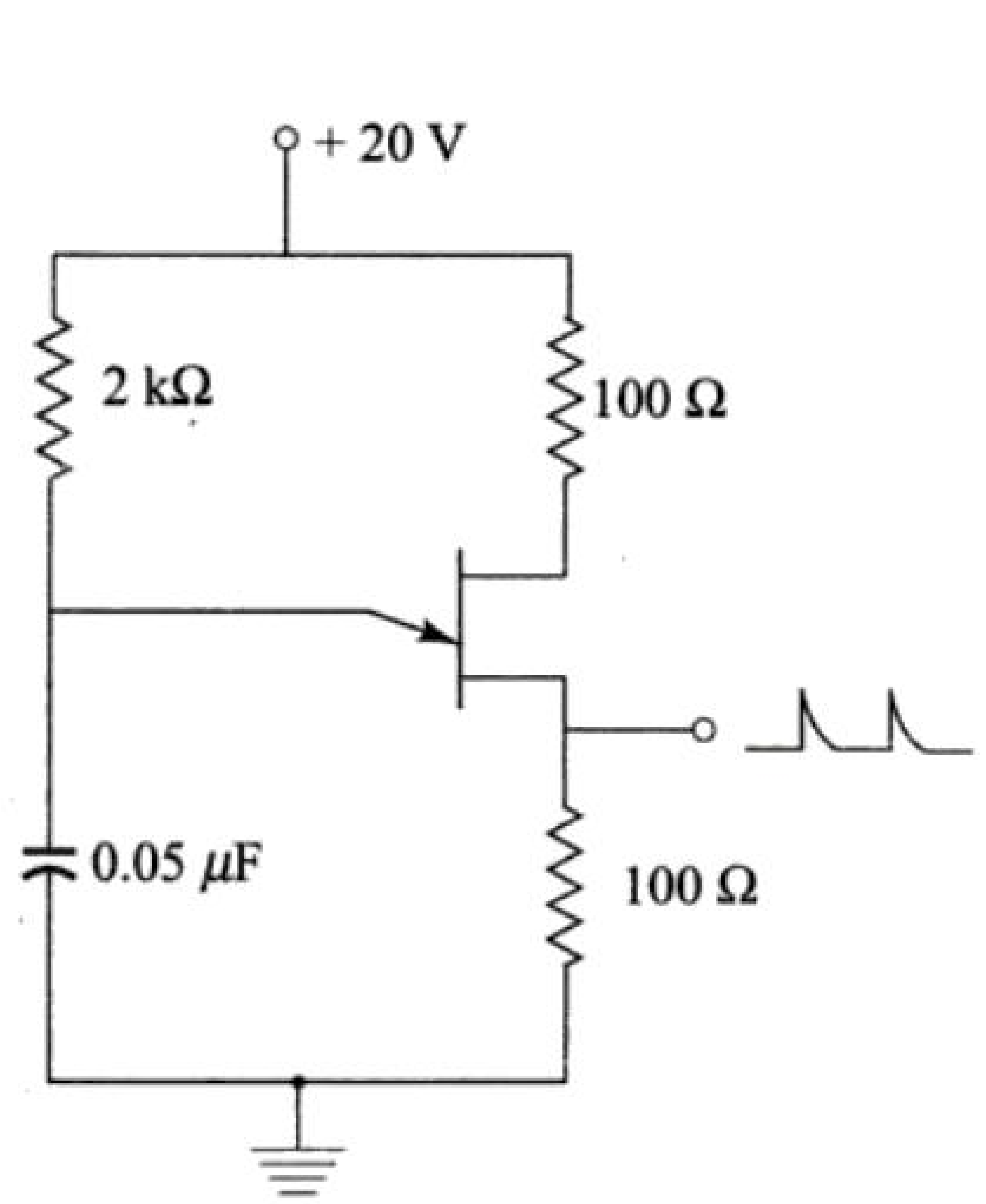

Fig. P.3.11

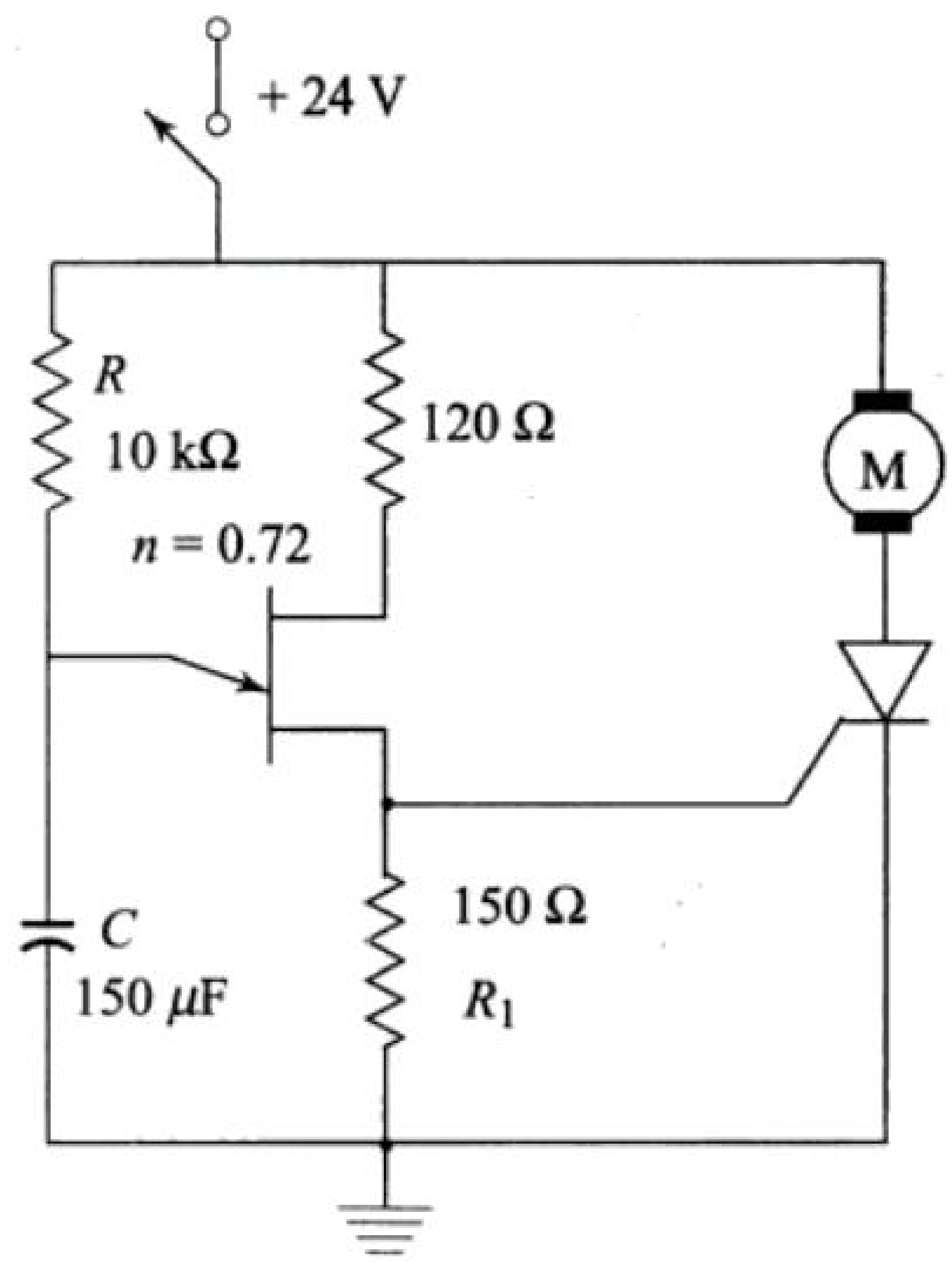

Fig. P. 3.12

3.13 Explain how the operation of PUT differ from that of the UJT. What are the advantages of PUTs over UJTs?

3.14 Draw and explain the general block-diagram of a thyristor trigger circuit.

3.15 Draw RC half-wave trigger-circuit for one SCR and discuss the function of the various components used. Describe with the help of waveforms how the output voltage is controlled by varying the resistance.

3.16 Explain with neat circuit diagram and waveforms the PUT relaxation oscillator.

3.17 Describe the RC full-wave trigger circuit for one SCR when the load is a.c. Also, draw the related voltage waveforms.

3.18 Explain the working of an oscillator employing an UJT. Derive expression for the frequency of triggering.

3.19 Draw and explain the equivalent circuit and *V–I* characteristic of the UJT in detail.

3.20 Draw and explain circuit diagram for the synchronized UJT triggering. Also, draw and explain the associated voltage waveforms.

3.21 Draw a circuit diagram for the ramp-and-pedestal trigger circuit used for the single-phase semiconverter. Describe its operation with appropriate waveforms.

3.22 Design the PUT 30 minute time-delay circuit.

3.23 Explain the PUT circuit operation in ''on'' state and ''off'' state.

3.24 With the help of neat diagram, explain the working of microprocessor interfacing to power thyristor.

PROBLEMS

3.1 The circuit of Fig. 3.11 utilizes an SCR with $I_{g(min)} = 0.1$ mA and $V_{g(min)} = 0.5$ V. If $R_2 = 10$ kΩ and the diode is silicon, determine the value of R_{min} needed to cause triggering when e_s reaches 3.2 V. [*Ans.* 10 kΩ]

3.2 If e_s in Problem 3.1 is a 40 V_{p-p} sine wave, determine the trigger angle. As R_{min} is increased, what happens to the trigger-angle? To the load-power?

[*Ans.* 5.10]

3.3 Consider the circuit of Fig. P.3.3. The optoisolator is used to change the voltage levels forming from the logic circuit to higher voltage levels required by other circuitry. The logic circuit E_o levels are 0 V and 5 V. Q_1 has $B_{dc} = 200$ and the LED has $V_F = 1.5$ V @ 10 mA. The phototransistor sensitivity is 10 mA of collector current per mA of LED current. Determine the values E_x of for the two values of E_0.

[*Ans.* 50 V, 0 V]

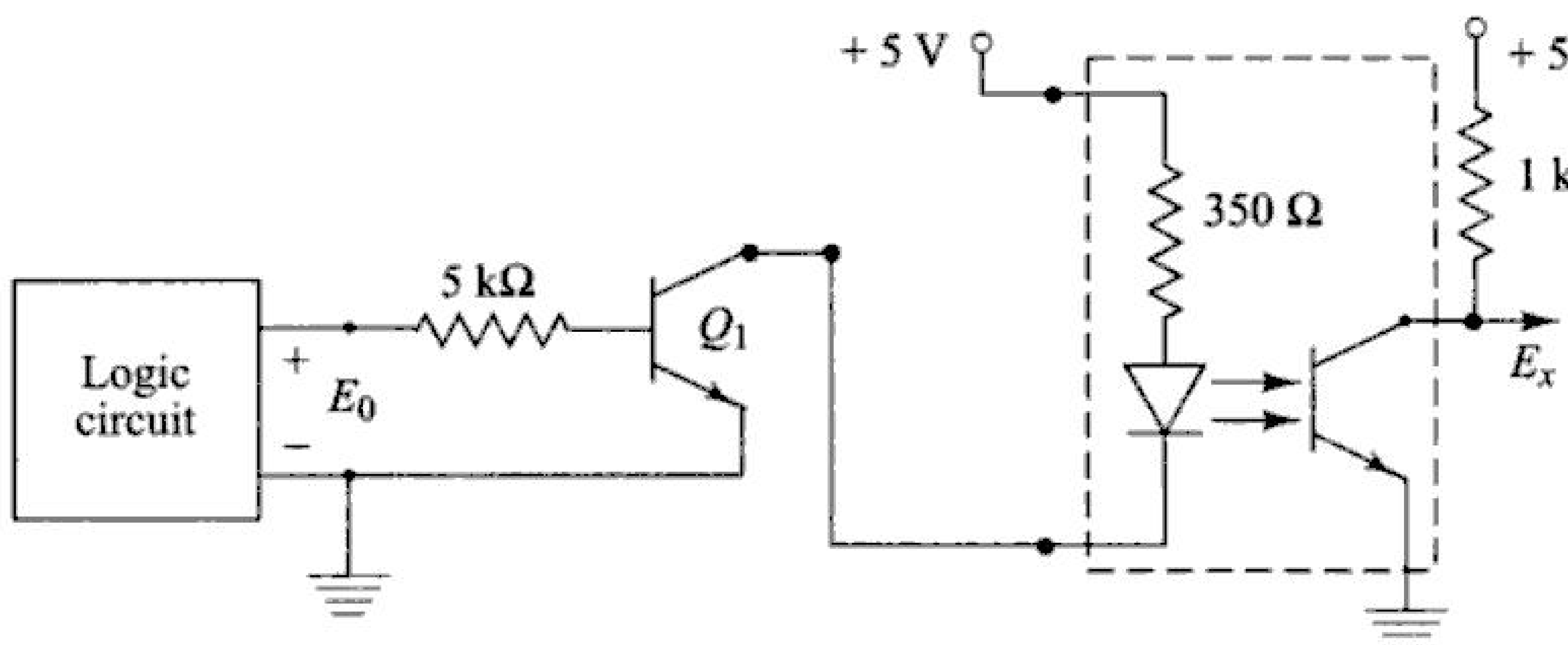

Fig. P.3.3

3.4 The optical coupler shown in Fig. P.3.4 is required to deliver at least 10 mA to the external load. If the current transfer ratio (it is the ratio of the output current to the input current through the LED. It is usually expressed as a percentage) is 60 per cent, how much current must be supplied to the input?

[*Ans.* 16.67 mA]

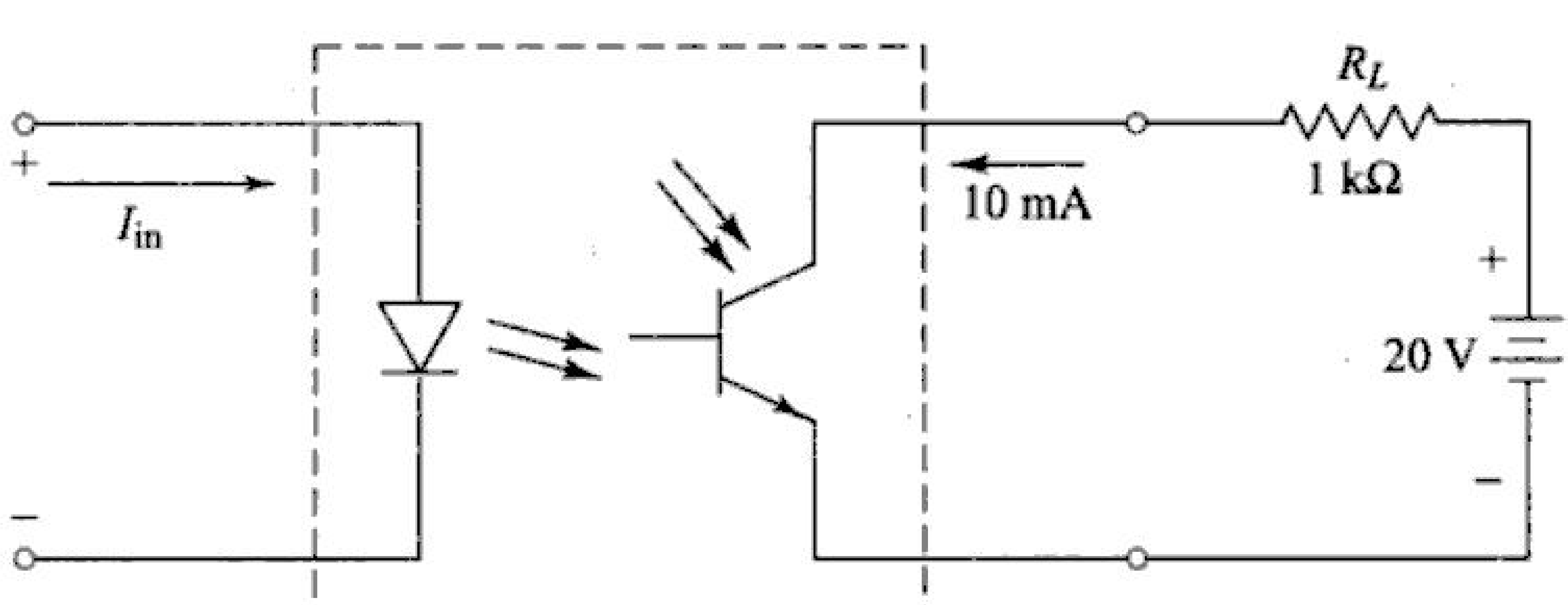

Fig. P.3.4

3.5 A UJT with the following parameters is used in the circuit of Fig. .3.16:

$$\eta = 0.66, V_D = 0.7\text{V}, I_V = 4 \text{ mA}$$

$$V_v = 1 V, I_P = 10\,\mu\text{A}.$$

(a) Assume that the UJT is initially "off". To what value must V_{EE} be raised to turn "on" the UJT? Use $V_{BB} = 20$ V.

(b) If $R_E = 1\ \text{k}\Omega$, to what value must V_{EE} be reduced before the UJT turns "off"? [*Ans.* (a) 13.91 V (b) 5 V]

3.6 The UJT of Problem 3.5 is used in the oscillator circuit of Fig. 3.18. The circuit values are $R_1 = 100\ \Omega$, $R_2 = 50\ \Omega$, $R = 10\ \text{k}\Omega$, $C = 2\ \mu\text{F}$ and $E_{dc.} = 24$ V.

(a) Determine V_p

(b) Determine whether the circuit will oscillate. If it oscillates, determine its frequency.

(c) Accurately sketch and label the capacitor waveform.

[*Ans.* (a) 16.7 V. (b) ≈ 45 Hz]

3.7 For the oscillator of Example 3.6, determine the range of frequencies which can be obtained by varying *R*. How may this range of frequencies be changed without changing the UJT?

[*Ans.* ≈ 0.62 Hz to 68.6 Hz].

3.8 In Fig. P.3.12, how long after the switch is closed will the motor be energized?

[*Ans.* 1.9 Sec].

3.9 Determine the period and frequency of the oscillator of Fig. 3.38. Sketch the waveforms of V_c, V_g, and V_K, showing appr-oximate amplitude. Also, indicate the three waves to decrease the frequency of the oscillator of Fig. P.3.9.

[*Ans.* 5.2 kHz]

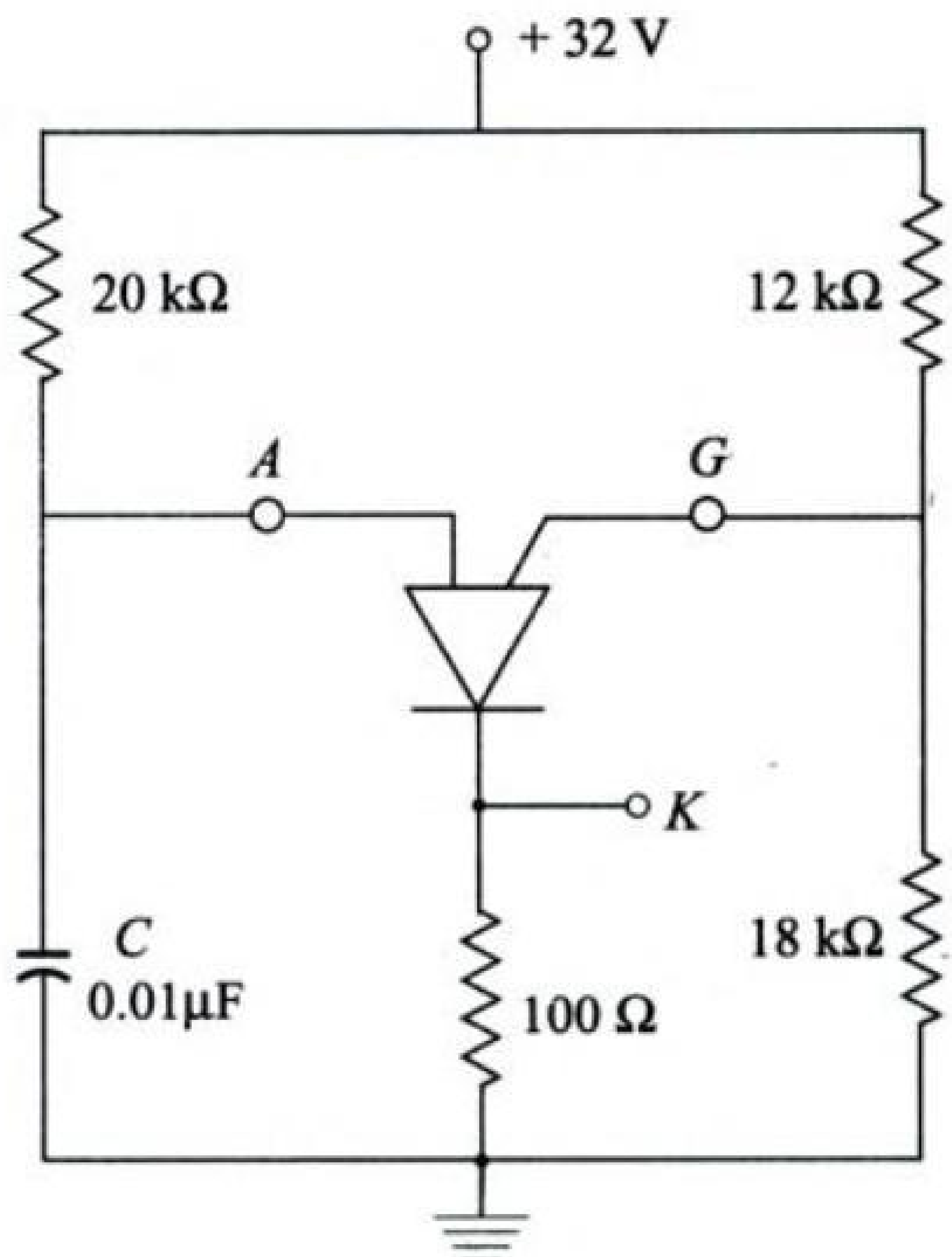

Fig. P.3.9

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Chapter 4

Series and Parallel Operation of Thyristors

LEARNING OBJECTIVES:

- To examine the operation of series and parallel connected SCRs.
- To consider the problems associated with series and parallel connection of SCRs.
- To introduce the static-equalising and dynamic equalising networks.
- To examine the basic-techniques of triggering series and parallel connected SCRs.
- To define string-efficiency and derating factor in relation to a series and parallel connected thyristor circuits.

4.1 INTRODUCTION

The maximum power which can be controlled by a single solid-state power device (SCR) is determined by its rated blocking voltage and by its rated forward-current. To maximise either of these two ratings requires some compromise in the other rating. Also, laboratory devices can always be cited with capabilities considerably beyond those of devices which are commercially available at any particular time.

Thyristor ratings have considerably improved since its introduction in 1957. Presently, SCRs with voltage and current ratings of 10 kV and 3.5 kA are available. However, for many industrial applications and also in terminal of HVDC transmission-lines, a single SCR cannot meet the power-requirements. Therefore, for controlling the power, in high-voltage low-current circuits, low-voltage high-current circuits, SCRs have to be connected in series and parallel combinations. SCRs are connected in series for high-voltage operation, whereas they are connected in parallel for high-current operation. In this chapter, we will consider the problems associated with series and parallel connections of SCRs, and discuss the measures adopted to overcome these problems.

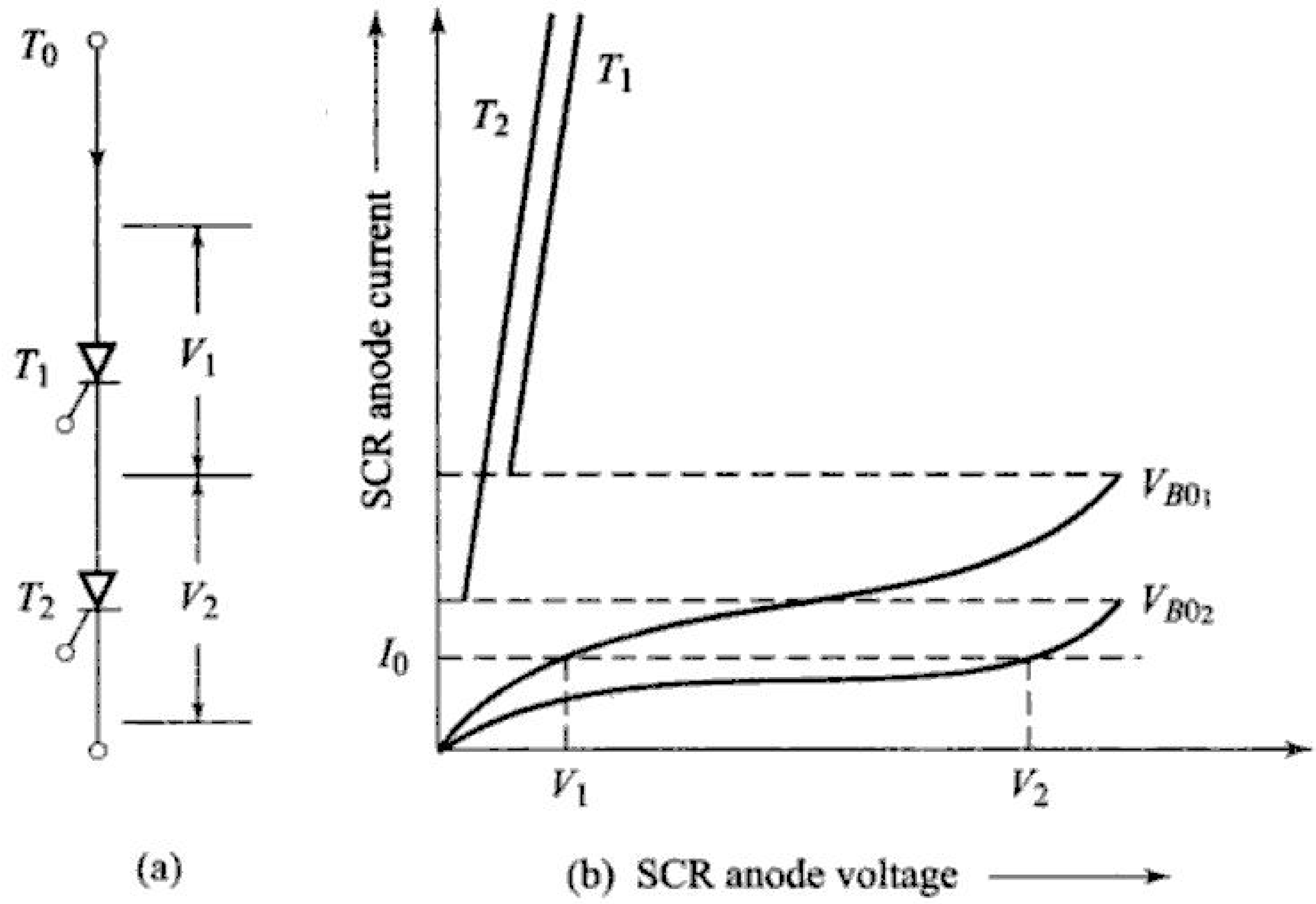

Fig. 4.1 *Distribution of voltage between two series connected SCRs*

4.3.2 Difference in Reverse Recovery Characteristics

The unequal distribution of voltages among thyristors in series also occurs during the transient conditions of turn-off, turn-on and high-frequency operation. A thyristor which has the largest turn-on time in the series string will have to momentarily support the full-string voltage. One method that can be used to minimise the unbalance caused by dissimilar turn-on delays is to apply high enough gate-drive with fast rise-time to minimise turn-on differences. If one thyristor in the string has short reverse-recovery time, it will alone support the string reverse-voltage. The problem of unequal voltage sharing among the series connected SCRs, due to difference in reverse recovery characteristics of the two unmatched SCRs, of the same type, can be understood by referring to Fig. 4.2.

As shown in Fig. 4.2, SCR T_1 is assumed to have less reverse-recovery time than that of SCR T_2. As a result, SCR T_1 recovers faster than SCR T_2 and it limits the reverse-current immediately. Therefore, SCR T_1 will share the maximum string voltage as SCR T_2 is not recovered. Hence, unequal voltage distribution occurs due to the difference in the reverse-recovery currents of the SCRs of the same time. Here, shaded area ΔQ represents the difference in reverse recovery charges of two thyristors. During turn-off, the capacitance of the reverse-biased junction determines the voltage distribution across SCRs in a series-connected string. As reverse-biased junctions are likely to have different capacitances, called self capacitances, the voltage distribution during turn-on and turn-off periods would be unequal. Voltage equalisation under these conditions can, however, be achieved by connecting shunt-capacitors as shown in Fig. 4.3. This capacitor removes inequalities in thyristor self-capacitances. Therefore, during turn-off periods, the resultant of self-capacitance and shunt capacitance of each thyristor in a string becomes equal.

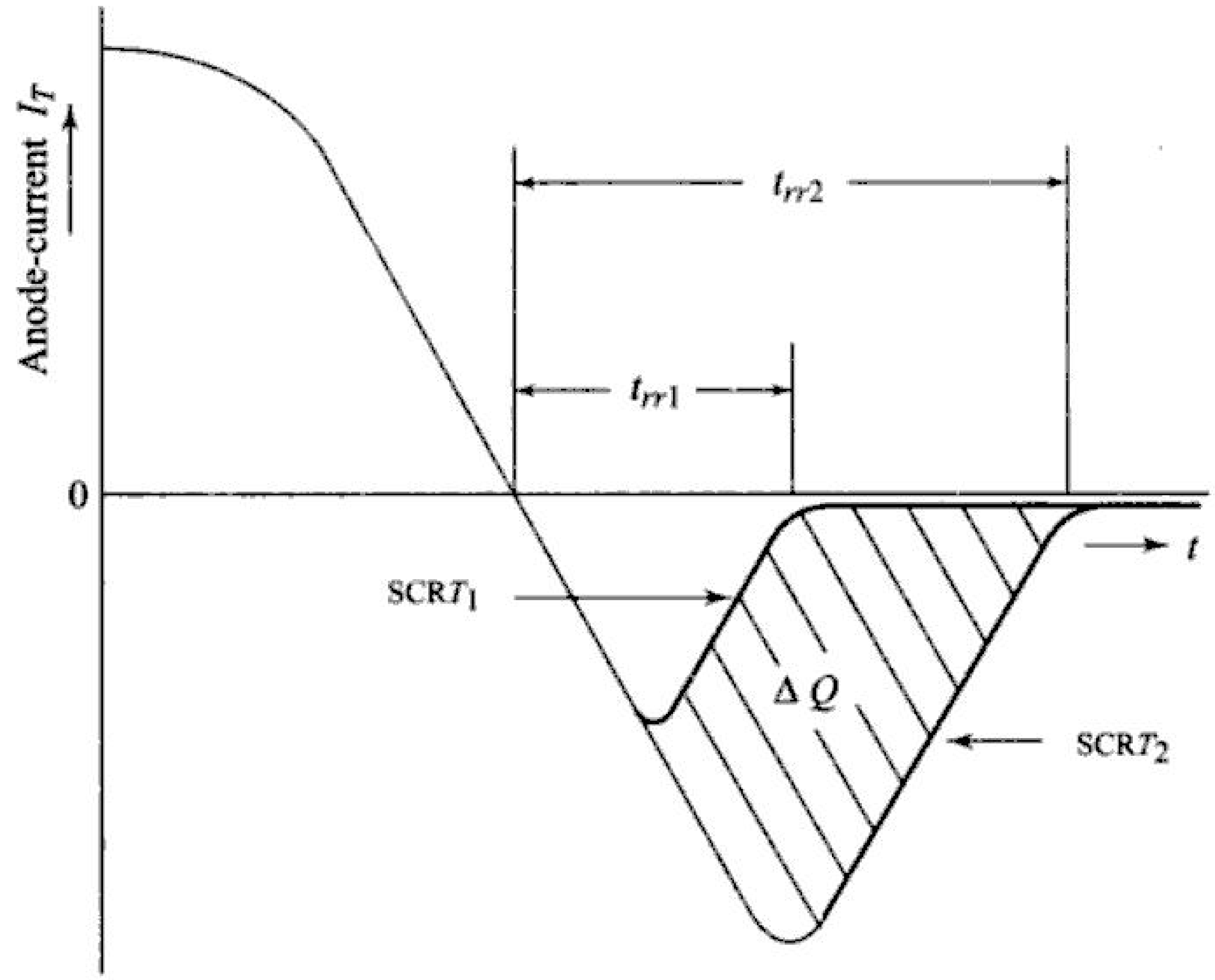

Fig. 4.2 *Reverse recovery currents of two SCRs (T_1, T_2) of the same type*

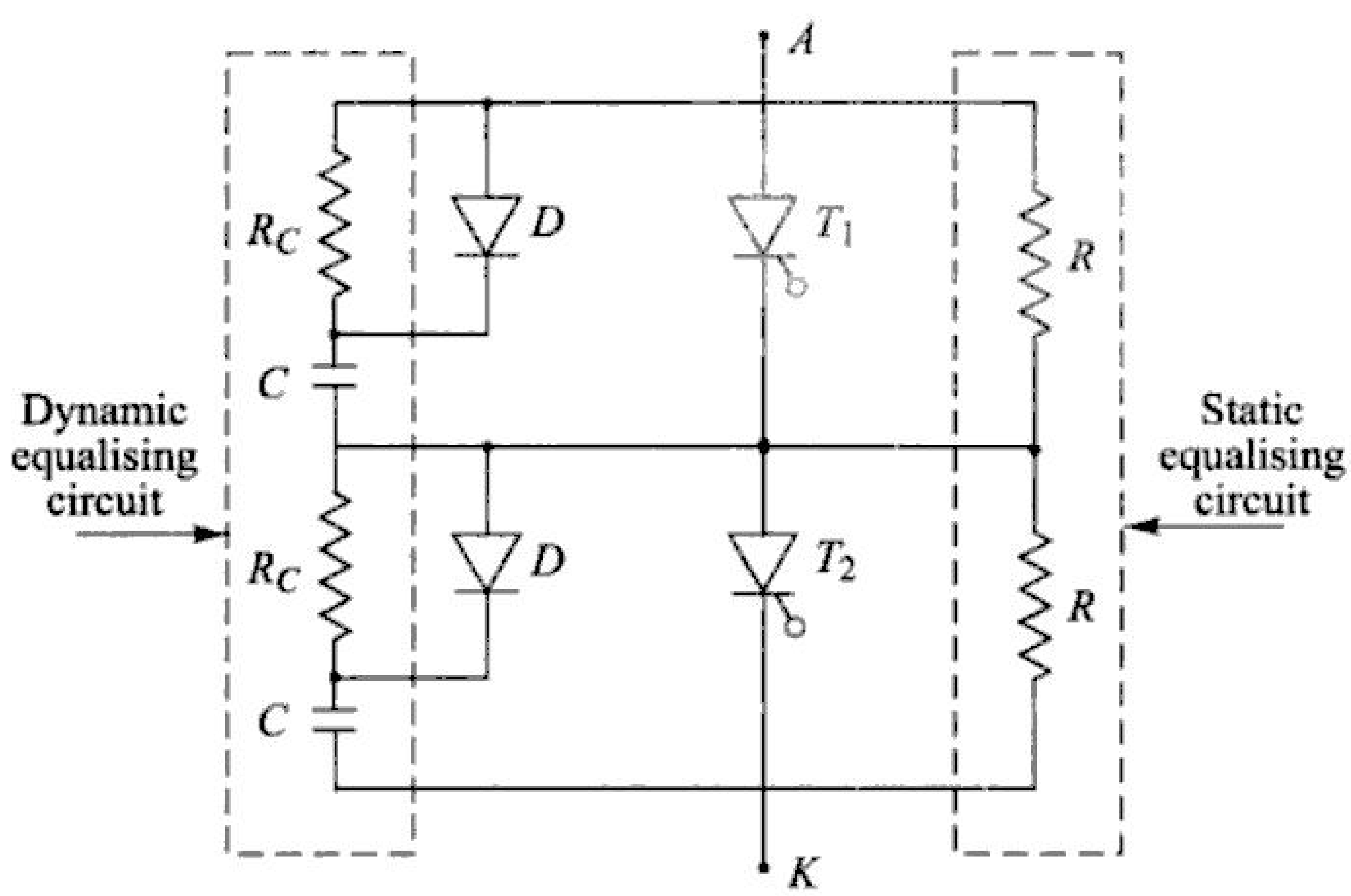

Fig. 4.3 *Equalising circuit for series operation*

During the period for which any of the SCR is in the blocking state, the corresponding capacitor will get charged to the voltage existing across that SCR. When this SCR is turned ON, the capacitor discharges heavy current through this SCR. To limit this discharge current, a damping resistor, R_C, is used in series with each capacitor as shown in Fig. 4.3. The value of these damping resistors much be kept to a reasonably low value in order not to reduce the effectiveness of the capacitors in equalising voltage during the reverse recovery interval. Resistor R_C also damps out the high-frequency oscillations that may arise due to the ringing of shunt capacitor with circuit inductance. The combination of R_C and C is called as the dynamic equalising circuit and is shown in Fig. 4.3.

A diode D is also connected across damping resistor R_C. This diode D provides the path for charging the capacitor, when forward voltage appears across the device. Hence, diode D bypasses the resistor R_C during charging interval of capacitor C and makes the capacitor more effective in voltage equalisation and for controlling $\frac{dV}{dt}$ across the SCR. In order to prevent ringing, small amount of damping resistance should still be used in series with the diode. While selecting diodes, care must be taken that these diodes must have soft recovery characteristics to avoid high voltage spikes which may be generated due to the abrupt recovery action of diodes. The criteria for selecting the required capacitor in dynamic equalising network is given in Section 4.4.

4.4 EQUALISING NETWORK DESIGN

4.4.1 Static Equalising Network

It is very clear from Section 4.3 that, a uniform voltage distribution in steady state can be achieved by connecting a suitable resistance across each SCR, such that each parallel combination has the same resistance. This will require different value of resistance for each SCR which is a difficult task. A more practical way of obtaining a reasonably uniform voltage distribution is to connect the same value of resistance R in parallel with each SCR, as shown in Fig. 4.4. This shunt resistance R is called as the static equalising circuit. The value of this shunt resistance can be obtained as follows:

Let n_s be the number of thyristors connected in series, as shown in Fig. 4.4. Recall that, in a series string, thyristors with lower leakage current (blocking-current) will have to share greater portion of a steady state blocking voltage than will units with higher blocking current. If the range of blocking-current is defined as $I_{b(max)} - I_{b(min)} = \Delta I_b$, it is observed that the maximum unbalance in blocking-voltage to SCRs of a series string occurs when one member has a blocking-current of $I_{b(min)}$ and all the remaining SCR's have $I_{b(max)}$. Figure 4.4 shows such a worst condition.

From Fig. 4.4, we can write

$$I_{b(min)} + I_1 = I_{b(max)} + I_2$$

or

$$I_{b(max)} - I_{b(min)} = I_1 - I_2 = \Delta I_b \tag{4.1}$$

Let E_D be the maximum permissible blocking voltage, then

$$E_D = I_1 . R. \tag{4.2}$$

Now, we can write string voltage E_s as

$$E_s = E_D + (n_s - 1) R I_2 \tag{4.3}$$

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$$R = \frac{(18 \times 500 - 7500)}{[(81-1) \times 1 \times 10^{-3}]} = 88.24\ \text{k}\Omega$$

Now,
$$C = \frac{(n_s - 1)\,\Delta Q_{max}}{(n_s E_D - E_s)} = \frac{(18-1) \times 30 \times 10^{-6}}{(18. \times 500 - 7500)} \quad C = 0.34\ \mu\text{F}.$$

4.5 TRIGGERING OF SERIES CONNECTED THYRISTORS

Series operation of thyristors takes place satisfactorily only if all the thyristors are *fired* at the *same instant*. Even differences of few microseconds in the gate pulses to different thyristors can have a major influence on *the voltage* sharing in series operation.

Consequently, in most equipment using multiple-operation of thyristors, all the thyristors are *fired* from the same pulse-amplifier source. Usually, pulse transformers with separate secondary winding for each thyristor or separate pulse transformers per thyristor are used.

With series operation of thyristors, the following points need to be considered when selecting the firing system to be employed:

(1) All the thyristors must act as one. If one SCR of a series string is not *fired* when it should be, *the full circuit will be impressed across* it causing it to breakover and fail due to excessive di/dt.

(2) The thyristors will all be at different *voltage levels* with *respect to earth* and high voltage *insulation will be required* between all the gate circuits. This complicates pulse-transformer design, as more the insulation used, the slower the rate of rise of gate pulse, and this will affect the transient sharing of the total voltage.

This leads to the use of fiber-optic light guides as a means of obtaining the necessary insulation level. Unfortunately, the guides can only pass a small amount of energy to the gate and so a power-source local to the thyristor is required.

(3) All the thyristors must turn-off at the same instant or else the last to turn-off will be exposed to the full circuit voltage. Due to variation of holding currents, this can only be guaranteed if the gate-pulses continue for the whole of the conduction period.

The following are the primary methods in common use for triggering series-connected SCRs:

(1) Simultaneous triggering.
(2) Sequential triggering.
(3) Optical triggering.

4.5.1 Simultaneous Triggering

Figure 4.5 shows the circuit of simultaneous triggering of series connected SCRs. All the thyristors are triggered simultaneously and independently with the help of pulse-transforming. Hence, this method is also called as independent or individual *firing* method. Most of the trigger pulse transformers are provided with two secondary windings and these can be used for two series connected thyristors. For more than two thyristors, special triggering transformer has got to be made with sufficient number of secondaries.

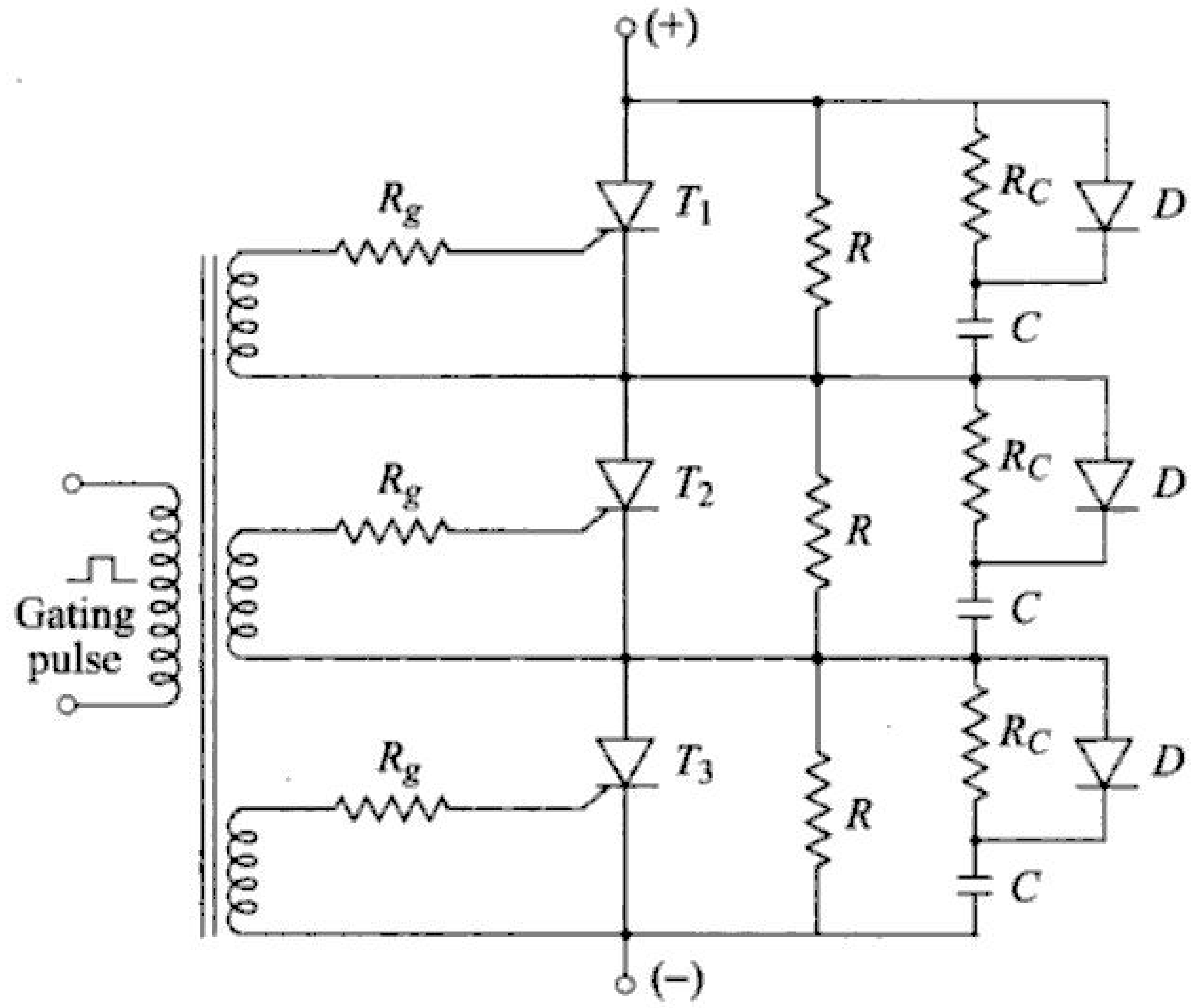


Fig. 4.5 *Simultaneous triggering*

The main triggering pulse is applied to the primary of the transformer. Each of the secondary winding is connected to the individual gates of respective SCRs in the string as shown in Fig. 4.5. Triggering requirements may differ quite widely between individual SCRs. To equalise the gate current in each SCR, a resistor R_g is connected in series with the secondary winding for swamping out any difference in a gate-to cathode impedance of individual units. Also, when using pulse transformer particular attention should be given to the insulation between windings. This insulation must be able to support at least the peak of the supply voltage.

4.5.2 Sequential Triggering

Figure 4.6 illustrates the sequential triggering technique. In this technique, one "master" SCR is triggered, and as its forward-blocking voltage begins to collapse, a gate signal is thereby applied to the "slave" SCR. Hence, this method is also referred to as slave-triggering method.

As shown in Fig. 4.6, the master SCR T_3 is turned-on by the external gate-pulse. The dynamic-equalising circuit is used for sequential turn-on. Initially, when supply voltage is applied to the SCR series string, all thyristors tranform in their forward-blocking state and all capacitors get charged with the polarity shown. Now, when gate pulse is applied to the master SCR T_3, turned-on. Capacitor C_3 starts discharging and the path of discharging becomes,

$$C_{3+} - R_{C_3} - R_{g_2} - T_{2_{(G-K)}} - T_{3_{(A-K)}} - C_3$$

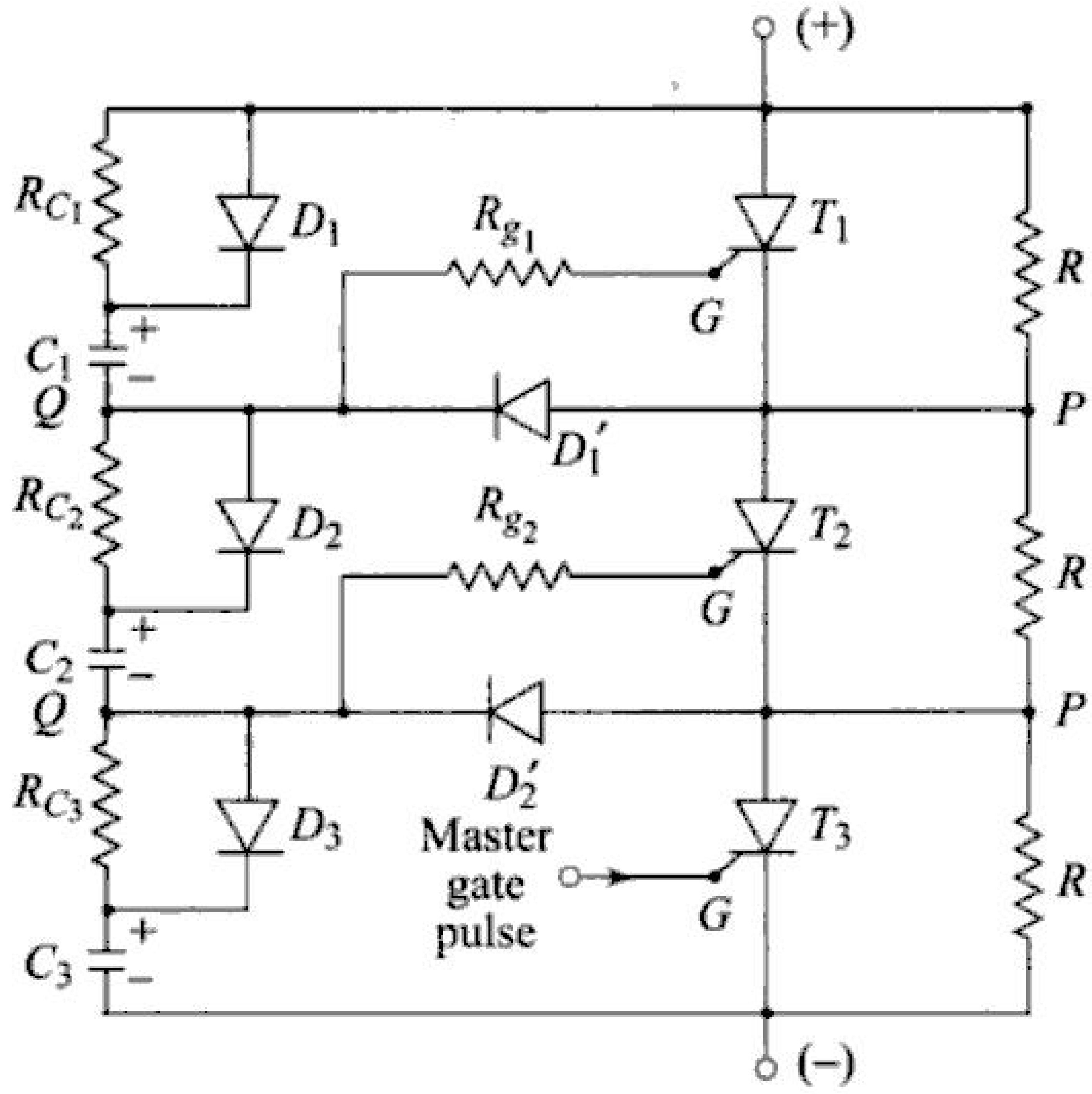


Fig. 4.6 *Sequential triggering*

Hence, thyristor T_2 turned ON. When T_2 turned-ON, its corresponding capacitor C_2 starts discharging and the path of discharging becomes,

$$C_{2+} - R_{C_2} - R_{g_1} - T_{1_{(G-K)}} - T_{2_{(A-K)}} - D_2^1 - C_{2-}.$$

Hence, thyristor T_1 turned-ON.

In this way, the discharge current of the shunt capacitor, through the SCR which is turned-on, will trigger the next SCR in the string. The process takes place very rapidly, and all the SCRs are turned-on in a very short time.

Here, the topmost SCR T_1 in the string will experience an increasing forward voltage due to the sequentially turning-on technique. This technique is generally used for generating impulse-voltages.

The minimum capacitance required to supply sufficient gate current to trigger under all conditions is given by:

$$C \geq \frac{10}{R_g + \dfrac{E_{GT(\max)}}{I_{GT(\max)}}} \mu F \tag{4.10}$$

where $E_{GT(\max)}$ = maximum gate triggering voltage, $I_{GT(\max)}$ = maximum gate triggering current, and R_g = gate – source resistance.

Because of diodes D'_1 and D'_2, potential of points P and Q will not be the same. The resulting circulating currents may turn-on the SCRs. These currents must be minimised by selecting appropriate equalising circuit parameters so that the string is turned-on only when a gate signal is applied to the master SCR T_3.

4.5.3 Optical Triggering

Figure 4.7 illustrates an optical triggering technique. In this technique, LASCR is connected in the gate circuit of each thyristor. Simultaneous triggering of SCRs is achieved by triggering LASCR. Therefore, this method provides the required gate isolation alongwith simultaneous turn-on when a single light source is used to turn ON all LASCRs. Here, the series resistance of R_1 and R_2 is made equal to the required shunt resistor R (static–resistance). Generally, R_2 is made small compared to R_1 so that low voltage LASCRs can be employed. The time constant R_1 C_1 must be made sufficient small so that C_1 is fully charged to the voltage dictated by R_2 at turn-on R_4 limits the peak-gate current.

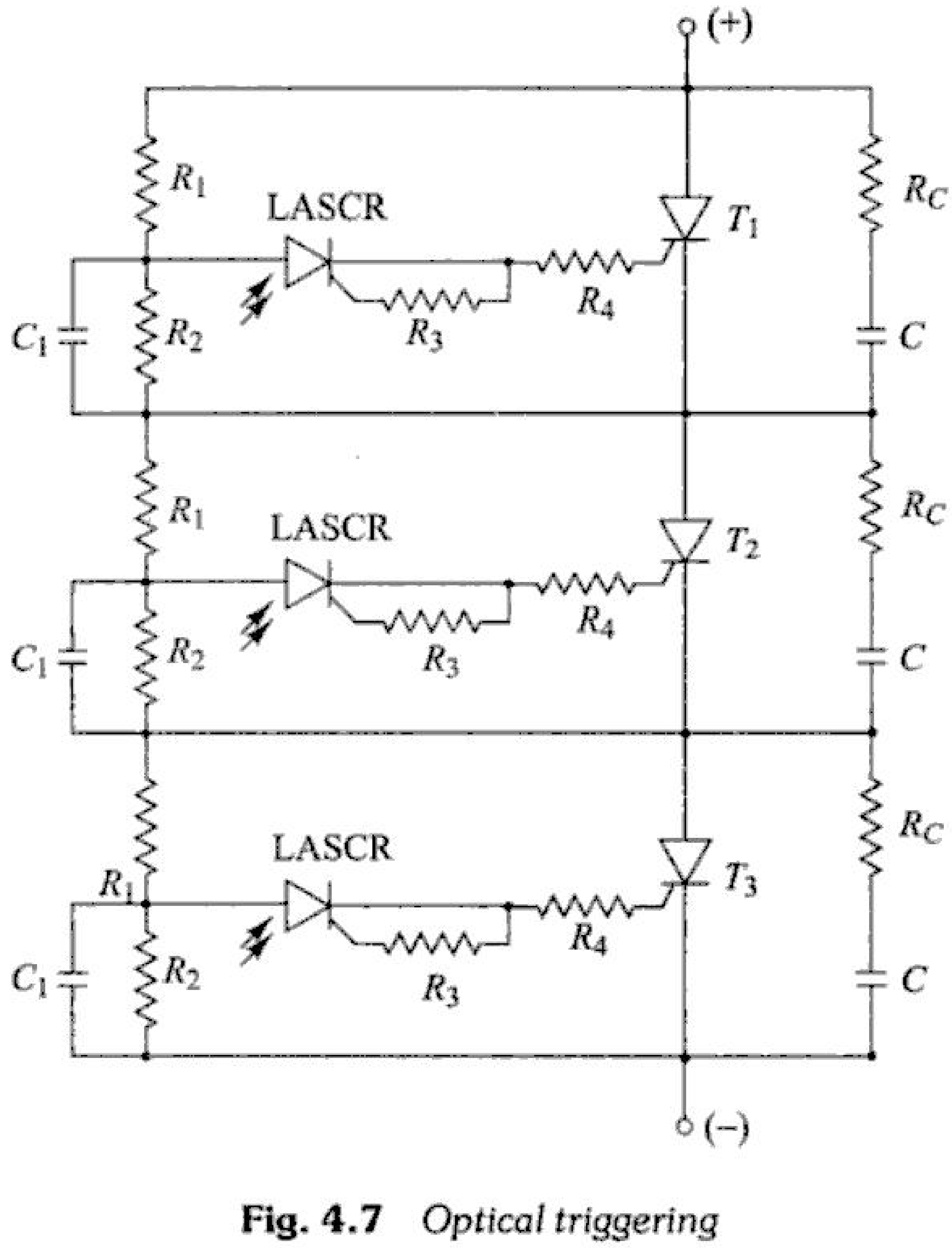


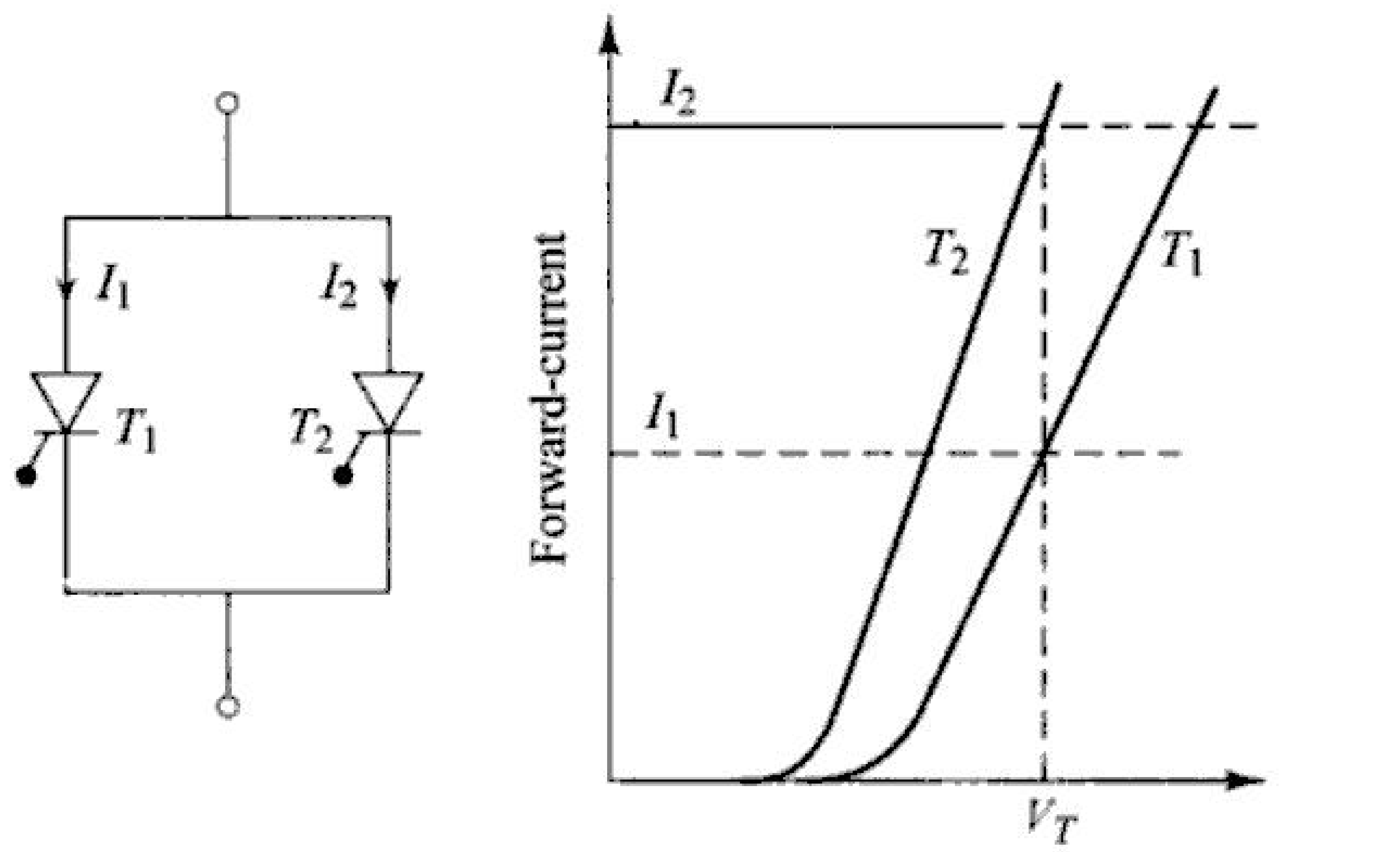
Fig. 4.7 *Optical triggering*

Therefore, in general for very high voltages, and particularly when trigger circuits is to be isolated from the power-circuit, triggering by a strong light source such as a Xenon flash tubes, phototransistor and fiber optic bundle is employed.

4.6 PARALLEL OPERATION OF THYRISTORS

The need to connect thyristors in parallel arises when the current or over current to be handled by the apparatus or equipment exceeds the rating of a single thyristor. Thyristors can be connected directly in parallel with each other if they have identical forward V–I characteristics. This is rarely the case unless very special selection of the thyristors is made to ensure good current sharing during normal load and under overload and faulty conditions.

The shape of the forward voltage of thyristors makes it difficult for them to achieve good sharing without assistance, as even quite a small voltage drop difference can result in a wide difference of load current, as shown in Fig. 4.8 shows the sharing of current between two parallel connected thyristors of same type.



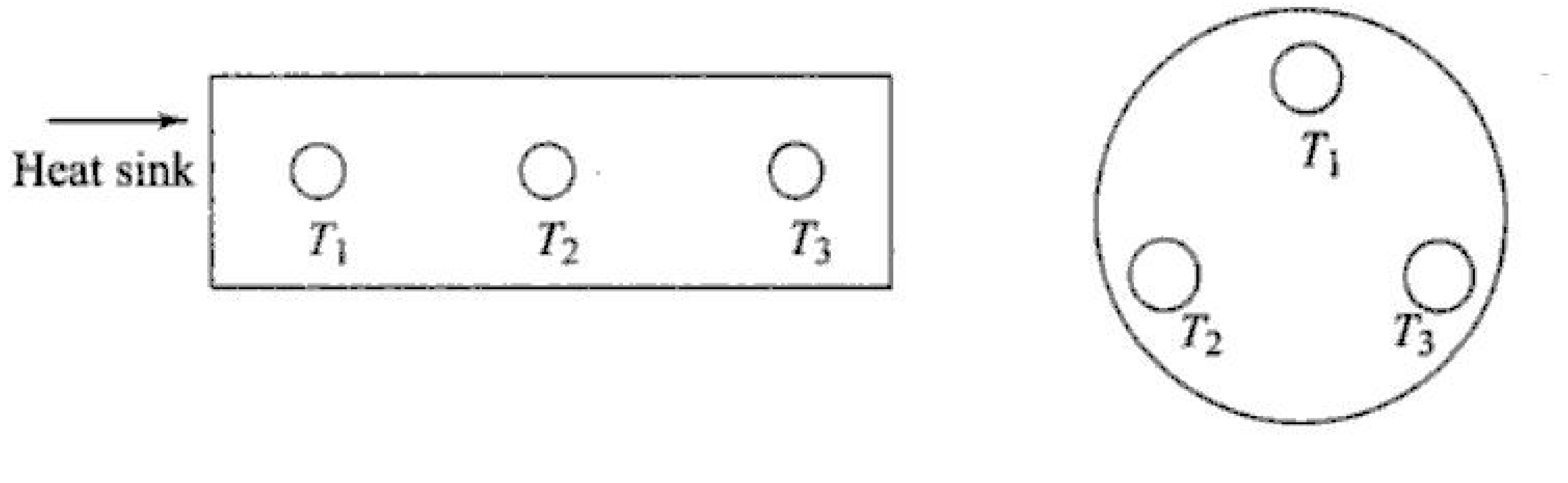
(a) Flat-arrangement (b) Forward-voltage drop

Fig. 4.8 *Parallel operation of two thyristors*

Figure 4.8(b) illustrates that for the same voltage drop V_T, SCR T_2 shares a rated current I_2, whereas SCR T_1 carries a current I_1 much less than the rated current I_2. Total rated current of the parallel unit is $(I_1 + I_2)$ instead of $2I_2$.

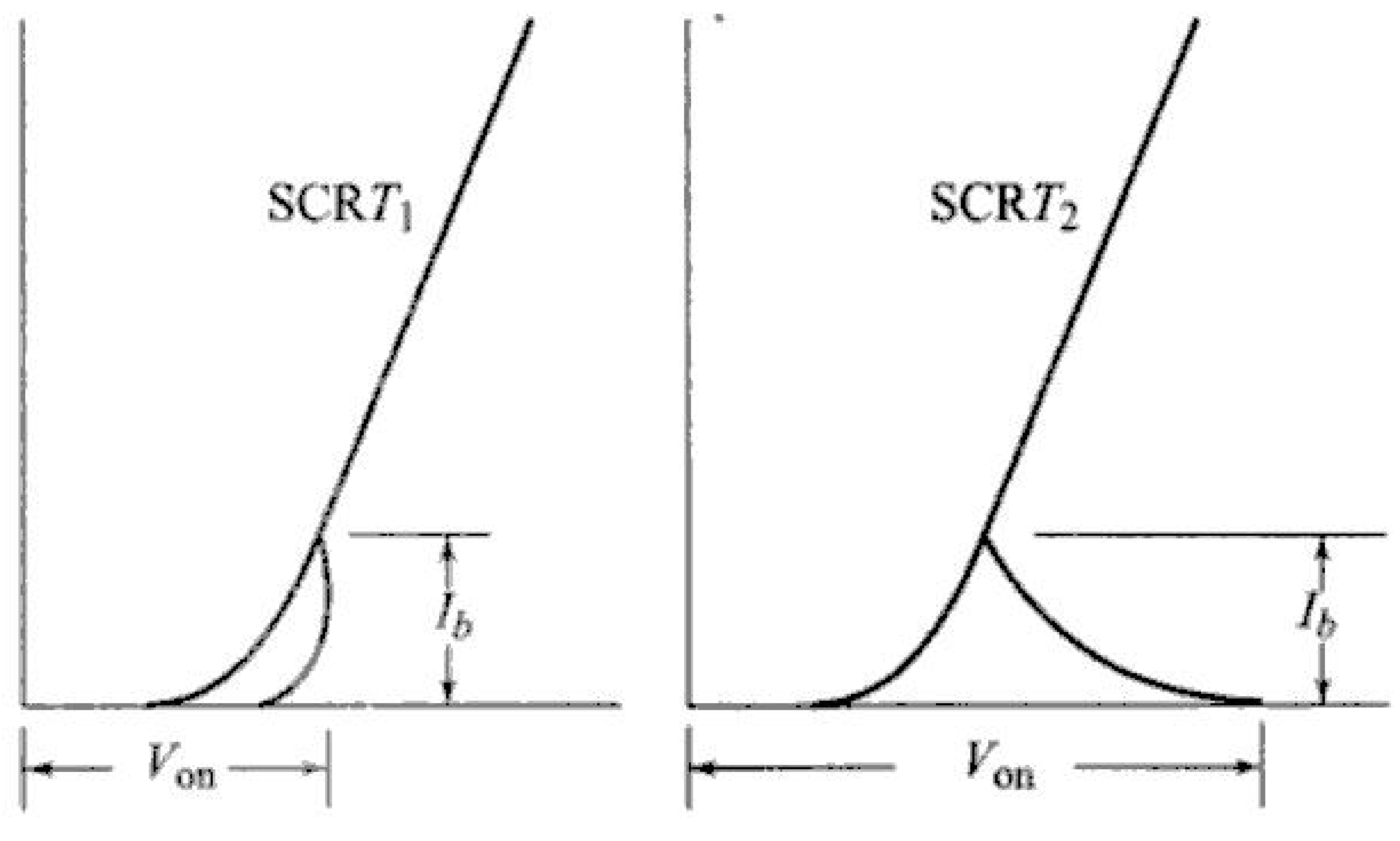
This unequal distribution of current in parallel connected thyristors leads to a thermal-runaway problem. For example, thyristor T_2 in Fig. 4.8 carries more current than the thyristor T_1. Due to large forward, current, its internal power dissipation will be more, thereby raising its junction temperature and reducing the dynamic resistance. This, in turn, will increase the current shared by SCR T_2 and the process becomes repetitive. The cumulative increase in current results in permanent damage to the SCR T_2, followed by the burning of SCR T_1. Therefore, all SCRs must operate at the same temperature when used in parallel connection. This can be done by a common heat-sink, as shown in Fig. 4.9.

The unequal distribution of current in a parallel unit is also caused by the inductive effect of current carrying conductors. When SCRs are arranged unsymmetrically, as shown in Fig. 4.9(a), the middle one will have more inductance due to more flux linkages. As a consequence, less current flows through the middle SCR as compared to outer two SCRs. This unequal current distribution can be avoided by mounting the SCRs symmetrically on the heat-sink as shown in Fig. 4.9(b).



(a) Unsymmetrical arrangement (b) Symmetrical arrangement

Fig. 4.9 *Mounting of thyristors on heat sink for parallel operation*



(a) (b)

Fig. 4.10 *Static thyristor turn-on-behaviour*

The difference in the turn-on characteristics can also influence the operation of thyristors in parallel. Differences in finger-voltages (the minimum forward anode voltage at which an SCR can be successfully turned-on with a trigger signal of sufficient magnitude) may prohibit the SCR with highest turn-on voltages to trigger. This is explained in Fig. 4.10. If SCRT_1 is directly connected in parallel with SCR T_2 having identical characteristics, SCRT_2 will never turn-on in application requiring zero voltage triggering. When SCRT_1 is switched ON, the anode voltage of SCR T_2 would be that of the on-state voltage of SCRT_1 and consequently, it will never equal or exceed the minimum required anode voltage to trigger SCR T_2 even if the width of the trigger pulse is greater than the delay-time of the SCR T_2. Hence, it is very essential that in direct paralleling of SCRs, the forward characteristic of each and every SCR must be properly matched. Matched thyristors are generally available for direct parallel operation.

4.7 METHODS FOR ENSURING PROPER CURRENT SHARING

In d.c. circuits, a series resistor R may be added to each arm of the parallel arrangement to improve the sharing of current. To force steady state current sharing, the resistors are connected as shown in Fig. 4.11. In other words, due to the connection of series resistor. The difference in the value of dynamic resistance R_T of thyristors is compensated.

If the two thyristors are of identical rating, then the two external series resistors R_1 and R_2 are chosen such that the total voltage drops are equal, that is, $R_1 + R_{T_1} = R_2 + R_{T_2}$, where R_{T_1} and R_{T_2} are the corresponding dynamic resistances of the two SCRs, at the rated current.

If two SCRs of different forward current ratings I_{T_1} and I_{T_2} are to be operated in parallel, then the same resistance R can be used for both units to ensure proper current sharing by the SCRs. Let V_{T_1} and V_{T_2} be the respective voltage drops across the two SCRs for forward currents I_{T_1} and I_{T_2}. In parallel units, their anode-to-cathode voltage drops are same, therefore,

$$V_{T_1} + I_{T_1}(R + R_{T_1}) = V_{T_2} + I_{T_2}(R + R_{T_2}) \tag{4.11}$$

Thus, from the knowledge of the spread of characteristics and the allowable power-loss in resistor R compatible with circuit conditions, the suitable value of R can be obtained from Eq. (4.11). Current equalisation by this method needs approximately 1.5 V voltage-drop across the series resistor at rated current. Obviously, such a addition of resistance affects overall efficiency and regulation.

Current sharing with reactors is a more efficient method than with resistors. In an a.c. circuit, the current distribution can be made more uniform by the magnetic coupling of the parallel paths as shown in Fig. 4.12. Figure 4.12 shows a 1:1 ratio reactor in bucking connection for two SCRs in parallel operation.

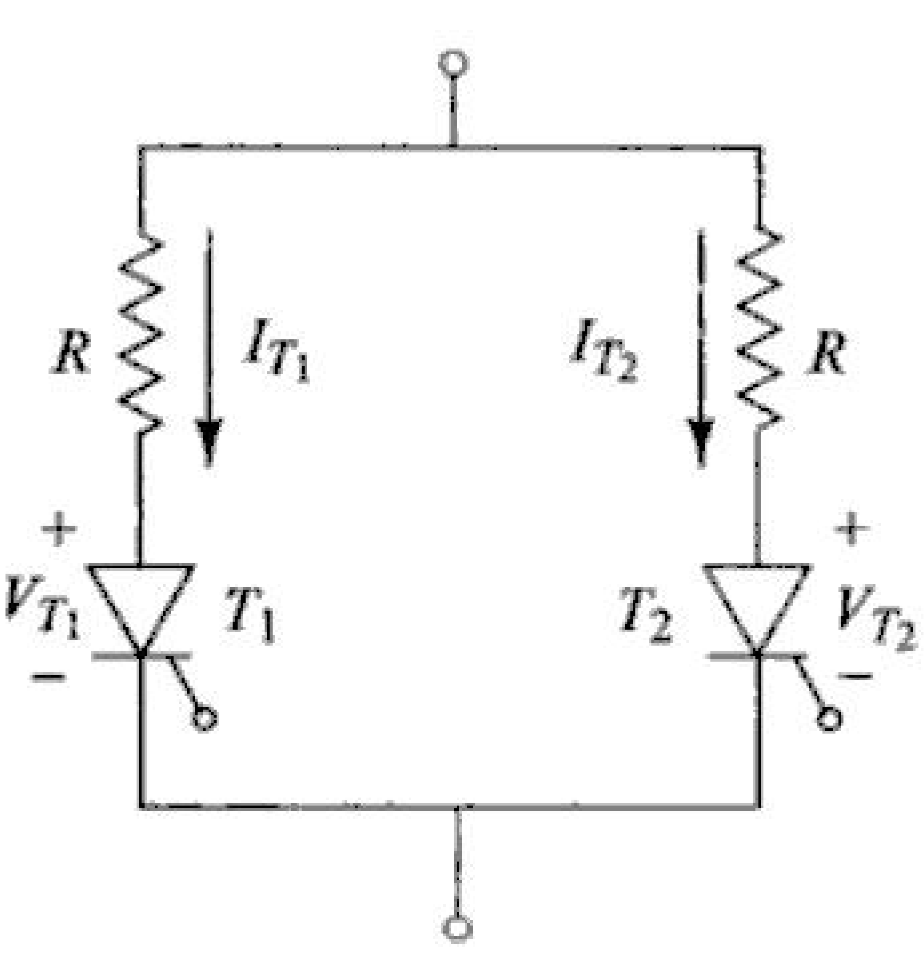


Fig. 4.11 *Current forcing using series resistor R*

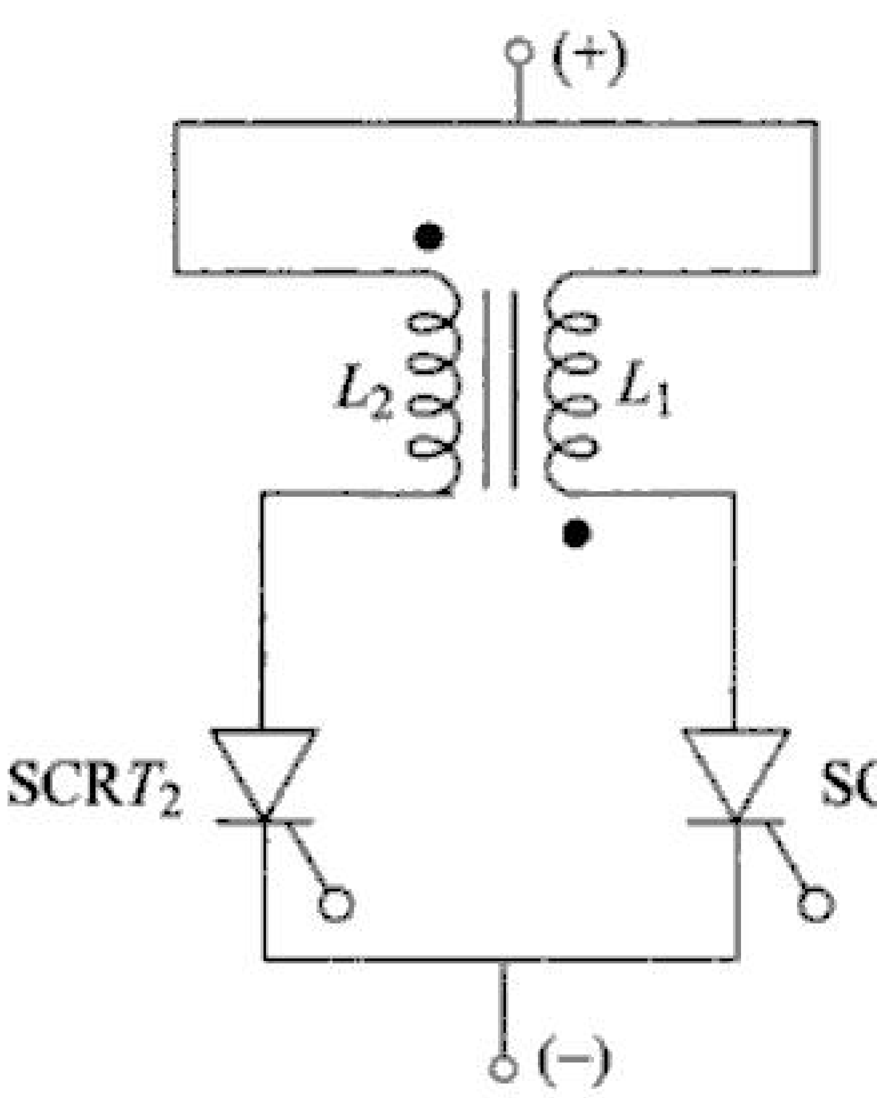


Fig. 4.12 *Current sharing using reactor*

If currents I_{T_1} and I_{T_2} are equal, then the voltage drop in the reactor will be zero because of the mutual cancellation of flux linkages in the coils. If the current through SCR T_1 tends to increase above the current through SCR T_2 (i.e., $I_{T_1} > I_{T_2}$), a counter EMF will be induced proportional to the unbalanced current and tends to reduce the current through SCR T_1. At the same time, a boosting voltage is induced in series with SCR T_2, increasing the current flow through the SCR T_2.

The most important magnetic requirements of such a reactor are high saturation and low residual flux densities in order to provide as great a change in total flux each cycle as possible. Introducing a reactor also improves the transient sharing of current. Equalising reactors can be used in parallel more than two SCRs. Figure 4.13 shows the current equalising reactors connections for three thyristors in parallel, whereas, Fig. 4.14 shows the current equalising reactor connections for four thyristors in parallel.

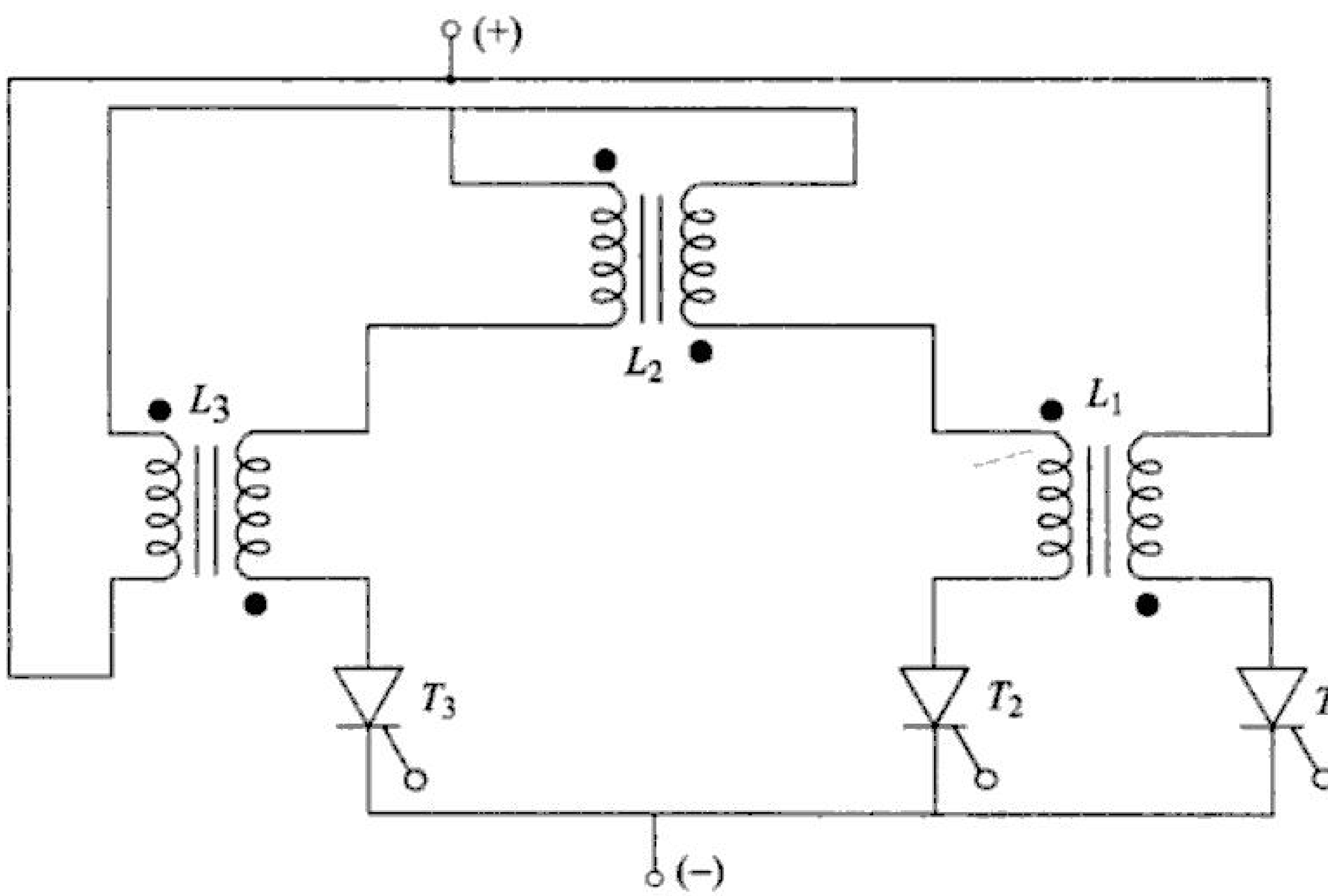


Fig. 4.13 *Current balancing reactor connections for three thyristor in parallel*

In Fig. 4.14, each thyristor has reactor that is magnetically, coupled with two different reactors. The reactor halves in series with T_1 are coupled with T_2 and T_4 and so on. These arrangements may be physically cumbersome and relatively expensive but they are highly reliable when continuous operation under partial fault conditions is needed to be provided.

SOLVED EXAMPLE

Example 4.2 A 100 A SCR is to be used in parallel with a 150 A SCR. The on-state voltage drops of the SCRs are 2.1 and 1.75 V, respectively. Calculate the series resistance that should be connected with each SCR if the two SCRs have to share the total current 250 A in proportion to their ratings.

Solution: Given

$$I_{T_1} = 100\text{ A},\quad V_{T_1} = 2.1\text{ V},\quad R = ?$$
$$I_{T_2} = 150\text{ A},\quad V_{T_2} = 1.75\text{ V}$$

Using the relation,

$$V_{T_1} + I_{T_1}(R + R_{T_1}) = V_{T_2} + I_{T_2}(R + R_{T_2})$$

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blocking voltage of 200 V. Hall also used the recently developed theories of carrier recombination, generation, and current flow to successfully model the electrical characteristics of power rectifiers and transistors.

In the mid 1950s, power device characteristics capitalized on the development of single-crystal silicon technology. The larger band gap of silicon rectifiers resulted in higher reverse voltage capability and higher operating temperatures. By the late 1950s, 500 V rectifiers were available in alloy junctions. The introduction of diffused junctions combined with mesa technology in the late 1950s proved to be the step necessary to realize reverse blocking capability of several kilovolts in later years. By the mid 1960s, theoretical avalanche breakdown voltages of upto 9000 V had been achieved by optimized contouring of mesa junctions. Increased current handling capability became a possibility by optimizing device packaging for minimum thermal and mechanical stress on the chip. Today, 77-mm diameter silicon rectifiers are available with continuous current ratings of 5000 A and a reverse voltage of 3000 V.

To put this development in perspective, while the first commercially available silicon transistors were announced by *TI* in 1954, it was almost a decade later that their practical application to high power conversion and control began. Emitter current crowding, reliability, and materials processing challenges precluded economic justification. The introduction of the planar process by Fairchild plus the application of photolithography techniques to wafer processing resulted in the birth of the power transistor business in the 1960s. A decade of effort in the industry related to second breakdown, power/speed performance and unique process such as epitaxy deposition, paid off. By the late 1970s, 200 A-500 V bipolar Darlington transistors with a gain of 50 were available together with 100 V–10 A transistors which could operate at frequencies upto 1 MHz. Since then, however, the application of MOS technology to power transistors has been a major focus of the industry due to the promise of high speed and high input impedance in many low voltage applications.

Beyond the important developments in material and process technology described above, there have been many significant device developments. One of the first of these was the publication of the *P-N-P-N* transistor switch concept in 1956 by Moll *et al.* Although, probably envisioned to be used for Bell's signal applications, engineers at General Electric quickly recognized its significance to power conversion and control, and within nine months announced the first commercial silicon controlled rectifier in 1957. This three-terminal power switch was fabricated using 5-mm square alloy-diffused mesa silicon chip and had a current rating of 25 A, and a blocking voltage capability of 300 V. The shorted emitter concept plus the planar process resulted in planar diffused SCRs in 1962. These processes resulted in high voltage blocking capability at junction temperatures of 125°C and made practical power control and conversion possible.

Since the early 1960s, thyristor producers have capitalized upon the process innovations of the signal industry while introducing new devices or structural improvements to existing devices. In 1961, a gate turn-off thyristor (GTO) was disclosed which combined the switching properties of a transistor with the low conduction losses of an SCR. In 1964, a bidirectional a.c. switch (TRIAC) was introduced by General Electric principally for 60-cycle consumer lighting and motor speed control. In 1965, light triggered thyristors were developed which later found significant application in optoelectronic couplers. In the late 1960s, a number of advances were made in the design of thyristor—cathode gate structures. Incorporation of interdigitated gates made possible high power 20 kHz inverters. Similarly, the inclusion of pilot gating techniques decreased the gating requirements as well as improved high frequency and pulse duty operation. The reverse conducting thyristor (RCT) and asymmetrical SCR were developed in 1970 to provide higher speed capability in those inverter applications where reverse blocking voltage was not required. In the mid 1970s, thyristor designers were intrigued with electric (or voltage) controlled thyristors which held promise for higher speed performance. The later, however, never came to fruition and the application of MOS concepts has proven to offer similar benefits but with greater ease in manufacture.

5.3 POWER SEMICONDUCTOR DEVICES

The power conversion world is a permanent quest for the ideal switch. Such a switch, in general terms, has the following requirements:

- high currents (turn-off, rms, average, peak, surge)
- high voltage (peak repetitive, surge, dc-continuous)
- fast switching (short on/off delays short rise/fall times, short turn-on/off times)
- low losses (conduction, switching)
- high frequency (fast switching, low switching losses)
- high reliability (low random failures, high power and temperature cycling, high blocking stability), low parts count)
- Compact constructions (low losses, low parts count).

Broadly, the power semiconductor devices can be classified into two main types according to the nature of their controllability:

1. Type I: Thyristors There are many different devices available today which can meet one or more of these requirements, but, as always, an improvement in one characteristic is usually gained at the expense of another. As a result, different devices have been optimized for different applications namely:

(i) Phase-Control Thyristors
(ii) Inverter-Grade Thyristors (fast-switching SCRs)
(iii) Asymmetrical-Thyristors (ASCRs)
(iv) Reverse-conducting Thyristors (RCTs)
(v) Gate-Assisted Turn-off Thyristors (GATTs)
(vi) Bidirectional Diode Thyristors (DIACs)

(vii) Bidirectional Triode Thyristors (Triacs)
(viii) Silicon Unilateral Switch (SUS)
(ix) Silicon Bilateral Switch (SBS)
(x) Silicon-Controlled Switch (SCS)
(xi) Light-Activated Silicon Controlled Rectifiers (LASCRs)

In general, the turn-on operation of the devices of this type is controllable using a trigger signal. However, the turn-off operation depends upon the condition of the power circuit. Hence, in this type, only turn-on switching is externally controllable.

2. Type II: Gate/Base Commutating Devices Both turn-on and turn-off operations of the device under this type are externally controllable by base or gate signals. High switching frequency devices which belongs to this type are:

(i) Power-BJT
(ii) Power-MOSFETs
(iii) Gate-Turn-off Thyristors (GTOs)
(iv) Static-Induction Thyristors (SITHs)
(v) Static-Induction Transistors (SITs)
(vi) Field-Controlled Thyristors (FCTs)
(vii) MOS-Controlled Thyristors (MCTs)
(viii) MOS-Turn-off Thyristors (MTOs)
(ix) Integrated Gate Commutated Thyristors (IGCTs)
(x) Emitter Turn-off thyristors (ETOs)

The power device design is pursued basically in two areas: that of the *transistor structure* and that of the *thyristor structure* whereby thyristors are generally preferred for their low conduction loses and transistors for their rugged turn-off capabilities. Numerous devices have been proposed, divided along these lines. Some strive to have the best of both worlds, exploiting the rugged on-state performanc of thyristors, while reverting to transistor-like behaviour prior to the critical turn-off phase.

Power BJT, MOSFET and IGBT has the transistor structure whereas GTO, FCT, MCT, IGCT, MTO and ETO has the thyristor structure.

As can be seen from the above paragraph, thyristor structures dominate in the number of proposed devices because of their inherent ability to conduct large current, with minimal losses. However, until recently, the only serious contenders for high power applications were the GTO (thyristor), with its cumbersome snubbers, and the IGBT (transistor), with its inherently high losses. Recent developments, however, have led to a device which successfully combines the best of thyristor and transistor characteristics, while fulfilling the additional requirements of manufacturability and high-reliability.

The salient design features, structures and applications of these different devices are discussed in the following sections.

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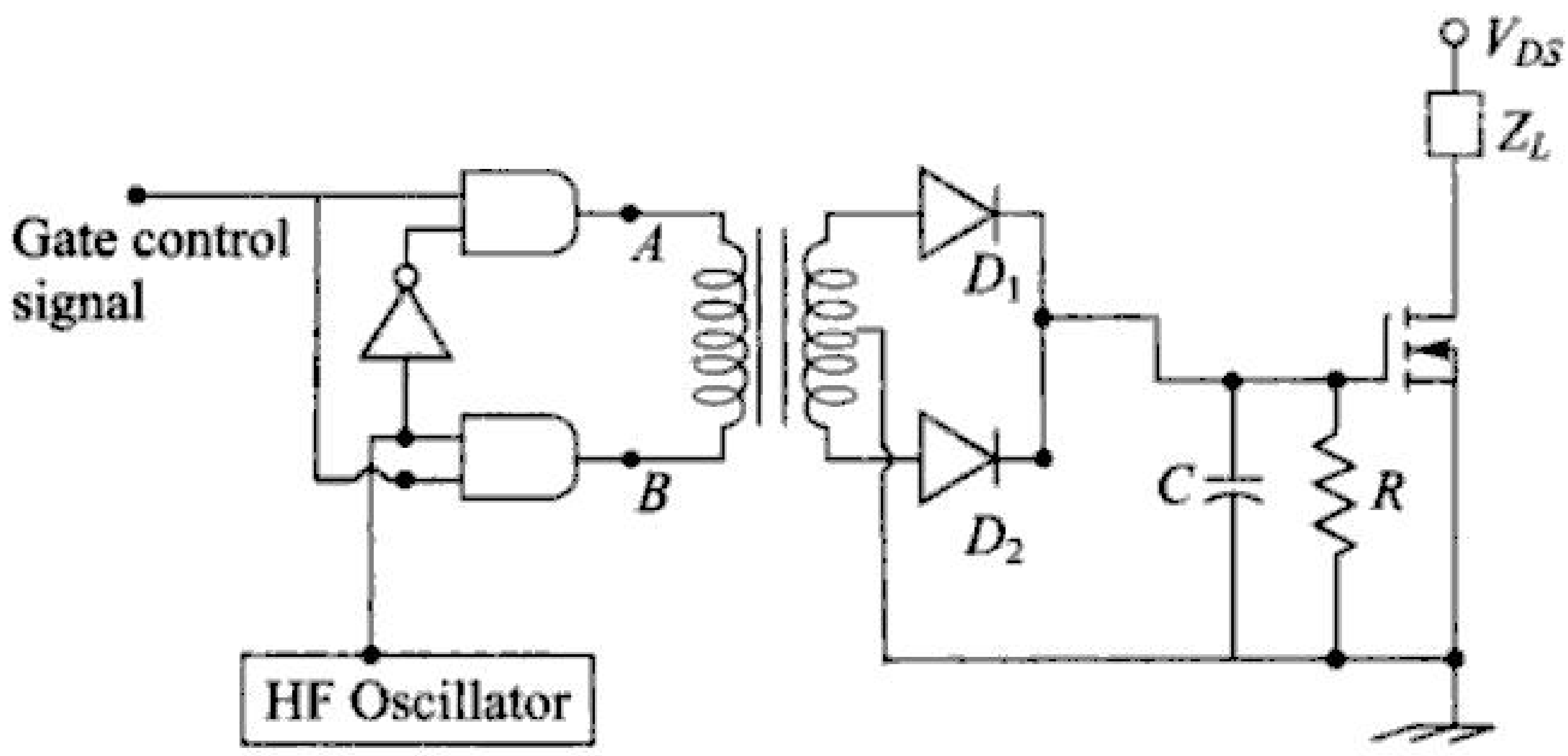

Fig. 5.44 *Pulse-transformer based drive circuit*

Since current (hence power) requirement for the gate-driver-circuit is very small at a steady state condition (few microwatts), a separate driver circuit and additional power supply are not required. However, during turn-on or turn-off transitions, a large current is required for fast switching. Another limiting factor is the switching capability of the diode. Thus Schottky diode can be used whose turn-off time is very small (0.23 μsec). Here high-frequency carrier signal reaches the logic gates when the input drive control signal is high. The output voltage of logic gates becomes alternately high and low. Therefore, current flows in the primary of the transformer from A to B and vice-versa. The voltage generated in the secondary winding of transformer is rectified and filtered. This d.c. voltage is used for driving a MOSFET.

Figure 5.45 shows an opto-coupler based gate driver circuit. Since the output current of the photo-transistor is not sufficient to drive a power-MOSFET, an additional transistor is used for amplification.

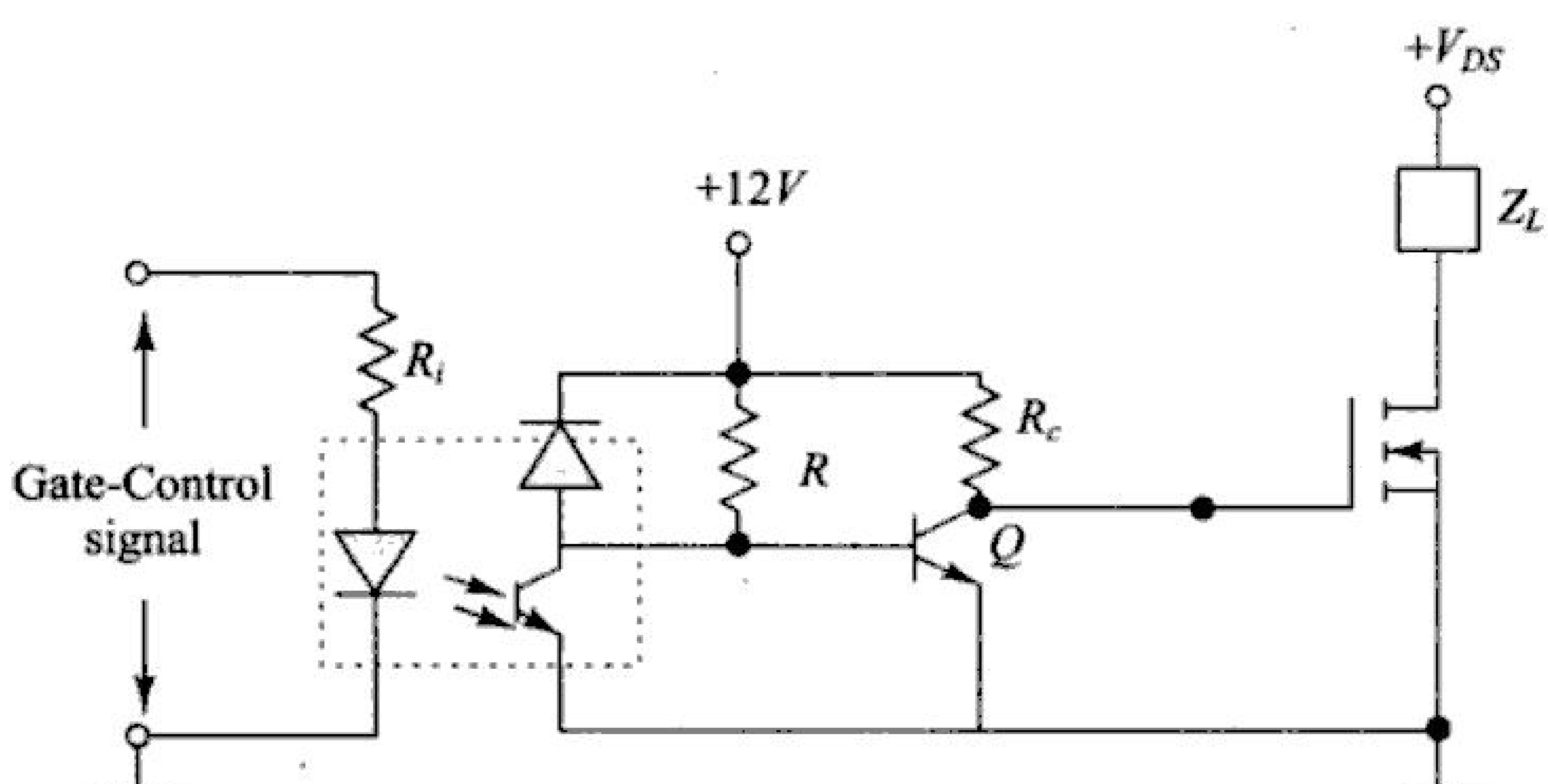

Fig. 5.45 *Opto-coupler based drive circuit*

5.14.9 MOSFET Losses

Following are the sources of power-losses in the switching MOSFET:

(i) On-state Loss (conduction loss):

A MOSFET has relatively high-on-state losses given by:

$$P_{on} = I_D^2 \cdot R_{DS(on)} \cdot \frac{t_{on}}{T} \quad (5.39)$$

where T is the total time period

(ii) Off-state Loss:

The off-state loss is given by, $P_{off} = V_{DS(max)} \cdot I_{DSS} \frac{t_{off}}{T}$ (5.40)

(iii) Turn-on Switching Loss:

The energy loss in the MOSFET while switching from off-state to on-state is given by

$$P_{sw_{on}} = \frac{V_{DS(max)} \cdot I_D \cdot t_r}{6} \quad (5.41)$$

$$= [P_{sw_{on}} = (0.637) \times (1/2\ V_{DS(max)} \cdot \left(\frac{1}{2} I_D\right) \cdot t_r\ ]$$

(iv) Turn-off Switching Loss:

The energy loss in the MOSFET when it switches from the on-state to the off-state is given by

$$P_{sw_{off}} = \frac{V_{DS(max)} \cdot I_D \cdot t_f}{6} \quad (5.42)$$

(v) Switching Power Loss:

The switching power loss is given by

$$P_{SW} = \left(P_{s.}W_{on} + P_{s.}W_{off}\right) \cdot f \quad (5.43)$$

where f is the switching frequency

(vi) Total Power-Loss in MOSFET:

Tower power-loss in MOSFET is given by

$$P_T = P_{on} + P_{off} + P_{sw} \quad (5.44)$$

Total power loss in a MOSFET is higher than in a BJT at low switching frequency. However, as the switching frequency is increased, BJT switching losses increase more than those of the MOSFET. Therefore, for high frequency applications, it is desirable to use a MOSFET.

SOLVED EXAMPLES

Example 5.6 For the circuit shown in Fig. E 5.6, determine:

(a) Power-loss in the on-state

(b) Power-loss during the turn-on interval

MOSFET parameters are: $t_r = 2\ \mu s$, $R_{DS(on)} = 0.2\ \Omega$, duty cycle $D = 0.7$ and $f = 30$ kHz.

Solution

Drain current given by, $I_D = \frac{V_{DS}}{R_L + R_{DS(on)}} = \frac{100}{12 + 0.2} = 8.2$ A

(a) Switching period $T = \frac{1}{f} = 1/30 = 33.33\ \mu$sec.

On-time is given by t_{on} = D.T. = $0.7 \times 33.33 \times 10^{-6} = 23.33\ \mu s$
Energy loss during on-time, $W_{on} = I_D^2\ R_{DS(on)} \cdot t_{on}$
$= (8.2)^2 \times (0.2)\ (23.33 \times 10^{-6}) = 313.74\ \mu J$

Now, power loss during on-time $P_{on} = W_{on} \cdot f$
$= 313.74 \times 10^{-6} \times 30 \times 10^3 = 9.41$ W

(b) Energy loss during turn-on, W_{on} =

$$\frac{100 \times 8.2}{6} \times 2 \times 10^{-6} = 273.33\ \mu J$$

Power loss during turn-on, $P_{on} = W_{on} \cdot f$ = $273.33 \times 10^{-6} \times 30 \times 10^3 = 8.2$ W

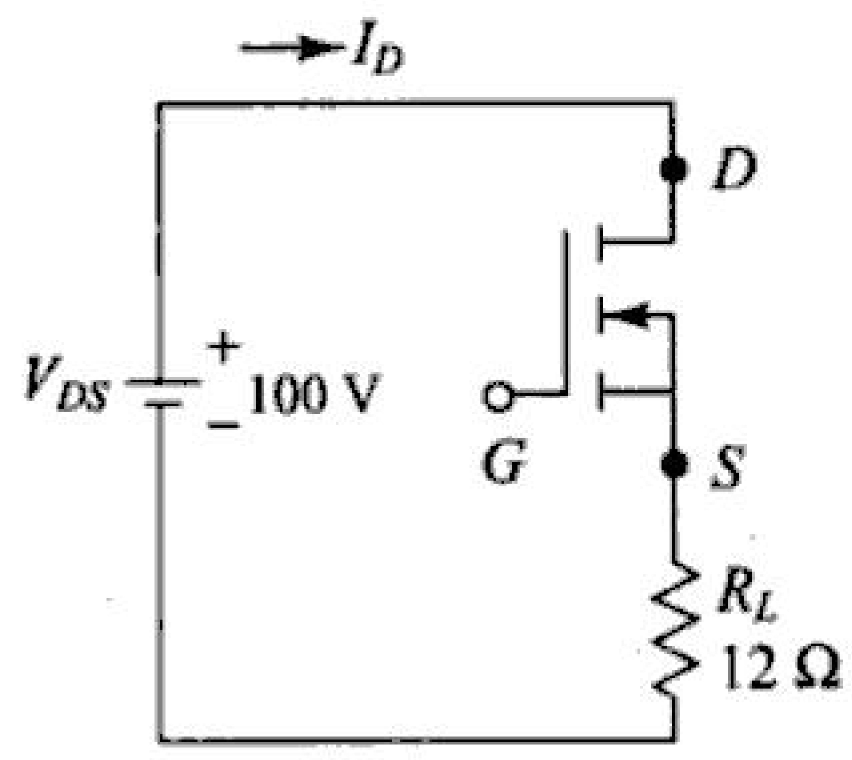

Fig. E 5.6

Example 5.7 Calculate the total power loss for the MOSFET having following para-meters:

V_{DS} = 120 V, I_D = 4 A, t_r = 80 ns, t_f = 120 ns, I_{DSS} = 2 mA, $R_{DS(on)} = 0.2\ \Omega$, duty-cycle D = 50%, $F_{switching}$ = 45 kHz.

Solution

(i) Total period $T = 1/f = 22.22\ \mu s$
(ii) Period $T_{on} = t_{off}$ (for 50% duty-cycle) = 11.11 μsec.

(iii) On-state loss, $P_{on} = \dfrac{(4^2) \times 0.2 \times 11.11 \times 10^{-6}}{22.22 \times 10^{-6}} = 1.6$ W

(iv) Off-state loss, $P_{off} = \dfrac{120 \times 2 \times 10^{-3} \times 11.11 \times 10^{-6}}{22.22 \times 10^{-6}} = 0.120$ W

(v) Turn-on switching power loss, $P_{W_{on}} = \dfrac{120 \times 4 \times 80 \times 10^{-9}}{6} \times 45 \times 10^3 = 0.288$ W

(vi) Turn-off switching power-loss, $P_{W_{off}} = \dfrac{120 \times 4 \times 120 \times 10^{-9}}{6} \times 45 \times 10^3 = 0.432$ W

(vii) Total power loss, $P_T = P_{on} + P_{off} + P_{W_{on}} + P_{W_{off}} = 1.6 + 0.120 + 0.288 + 0.432 = 2.44$ W

5.14.10 Comparison between Power MOSFETs and Bipolar Transistors

Power MOSFETs have a number of major performance advantages over bipolar transistors. These are discussed in the following sections:

1. MOSFETs are voltage controlled To switch a MOSFET ON, it is necessary simply to apply a voltage, typically 10 V for "full enhancement" between gate and source. The gate is isolated by silicon oxide from the body of the device, and the d.c. gain is virtually infinite. Drive power is negligible, and drive circuitry is

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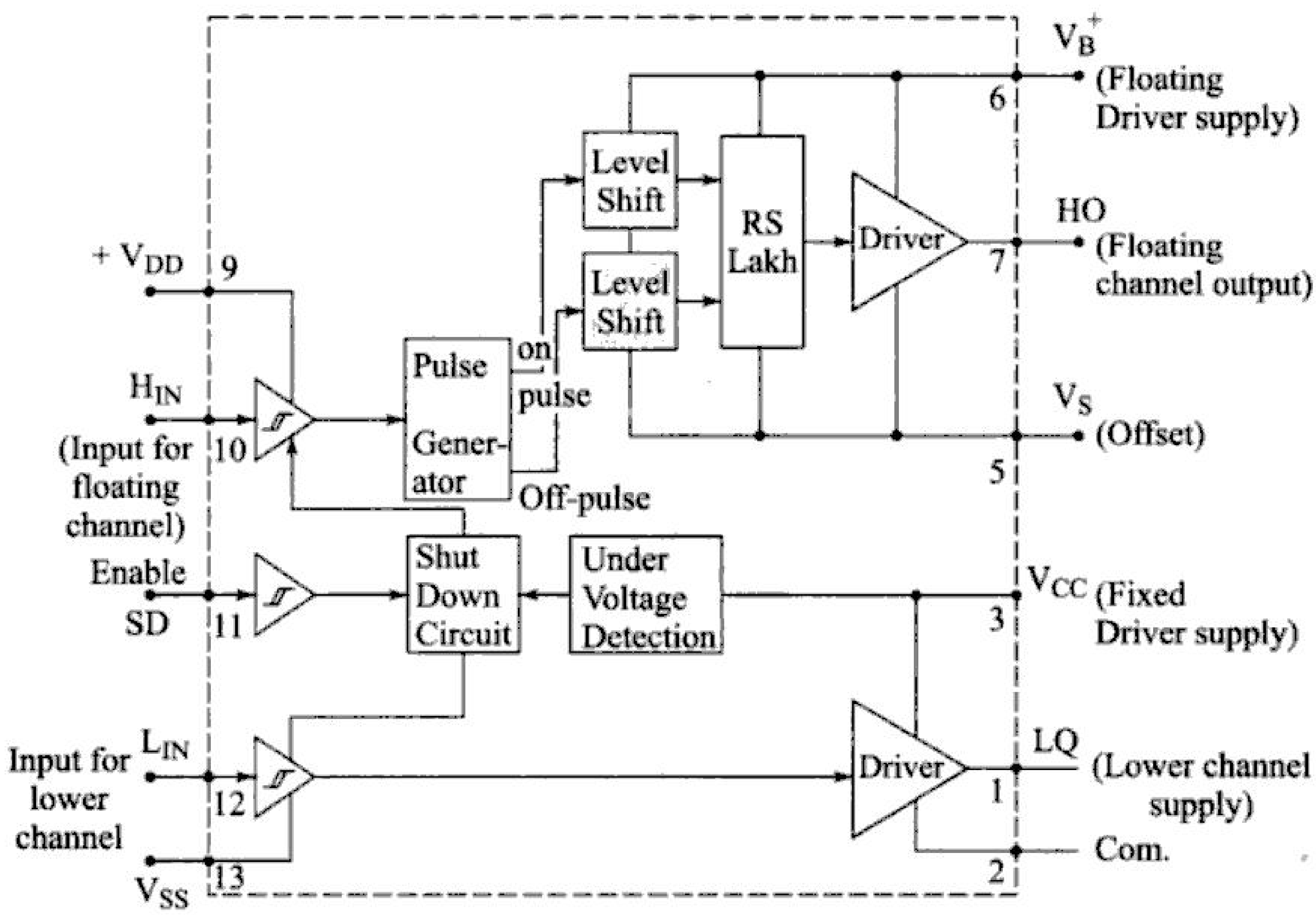

Fig. 5.66 *Functional block-diagram (Courtesy: International Rectifier)*

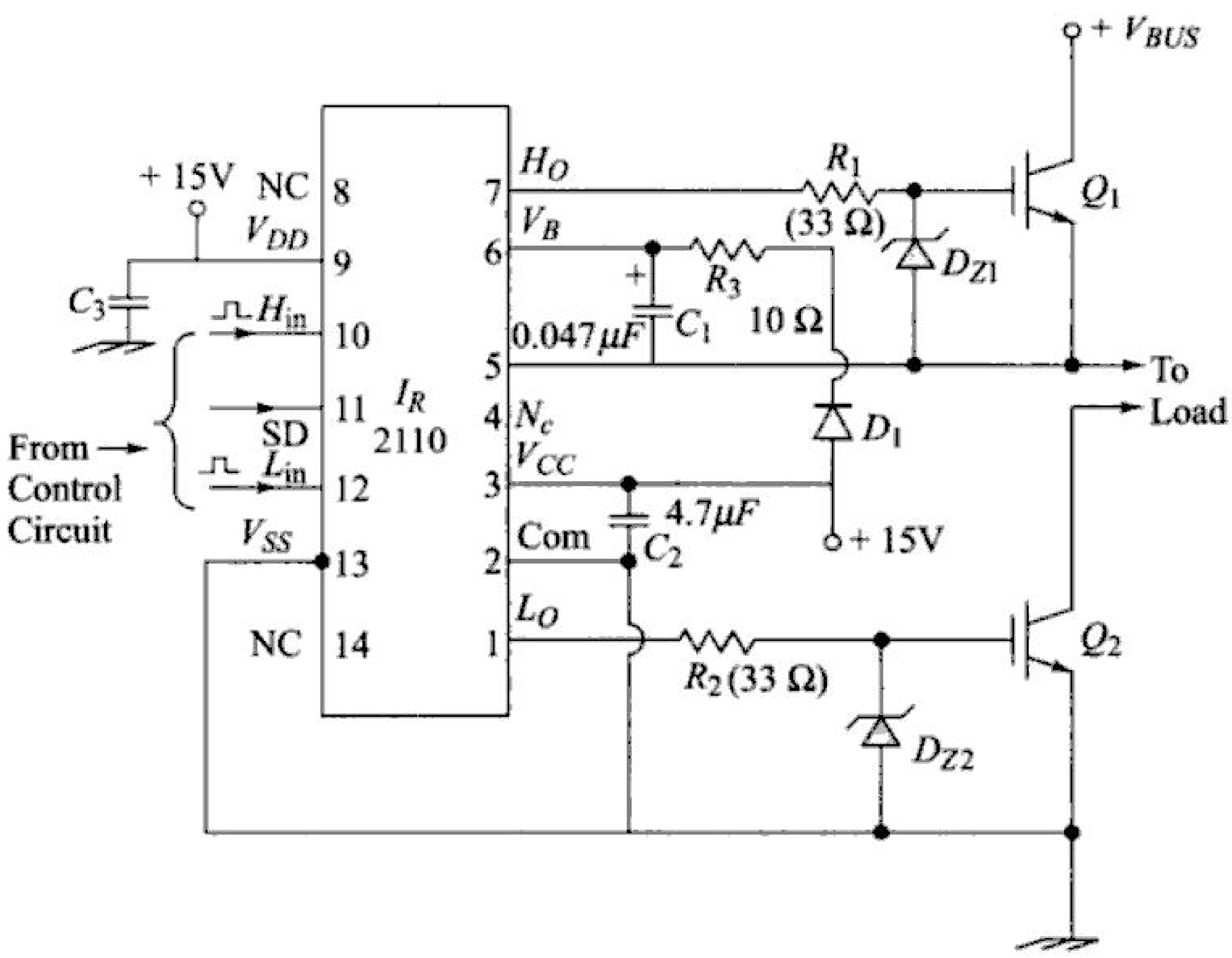

Fig. 5.67 *Typical connections*

Initially IGBT Q_2 is turned-on and Q_1 is off. Capacitor C_1 will charge through D_1, R_3, load, Q_2 to 15 V with the polarity shown in Fig. 5.67. As soon as Q_1 is turned-on, the potential at its source increases to V_{BUS}. This will boost the potential at the negative terminal of capacitor C_1 to V_{BUS}. The initial voltage on the capacitor is 15 V. Therefore, the voltage at pin 6 with respect to power ground becomes (V_{BUS} + 15 V), this voltage then gets connected to the gate of Q_1 through the upper driver. Thus, the gate emitter voltage of Q_1 is maintained at 15 V.

However, the capacitor C_1 discharges through the upper device. The discharge time of C_1 should be longer than the conduction period of Q_1. Therefore the values of R_3 and C_1 should be properly selected depending on the frequency of operation. If the capacitor C_1 discharges quickly even before the completion of the conduction interval of Q_1, then V_{GS} of Q_1 will drop down and Q_1 will turn-off.

Capacitors C_2 and C_3 are the supply bypass capacitors which are required to supply the transient current needed to switch the capacitive load. The capacitors C_1, C_2 and C_3 must be connected close to the actual device. A 0.047 μf ceramic disc capacitor in parallel with a 4.7 μf tantalum capacitor is recommended for the V_{CC} bypass. A 0.01 μf ceramic disc capacitor is usually sufficient to bypass the logic supply (V_{DD}). *SD* (pin 11) can be used to disable the outputs by connecting it to ground.

V_{DD} (pin 9) and V_{CC} (pin 3) can be connected together and operated from a single power supply.

Typical waveforms of IC 2110 are shown in Fig. 5.68 and the recommended dc operating conditions are given in Table 5.1.

Table 5.1 Recommended dc operating conditions

Symbol	*Parameter*	*Min.*	*Max.*	*Unit*
V_{BS}	Floating supply voltage	10	20	Volts
V_{HO}	High side channel o/p voltage	0	V_B	Volts
V_{CC}	Fixed supply voltage	10	20	Volts
V_{LO}	Low side channel output voltage	0	V_{CC}	Volt
V_{DD}	Logic supply voltage	3	V_{CC}	Volt
V_{IN}	Logic input voltage (H_{in}, L_{in}, S_D)	0	V_{DD}	Volt
V_{SS}	Logic supply offset voltage	–1.0	1.0	Volt

Applications: The high voltage bridge driver IC IR2110 can be used in the following applications:

(i) AC and DC motor drives.
(ii) High frequency switch mode power supplies.
(iii) Inverters
(iv) Choppers
(v) Battery charger
(vi) Induction heating and welding.

These driver ICs are designed for general and specific applications

(i) Current type: IR 2110, IR 2111, IR 2112

(ii) Special type:

- For square-wave and high voltage: IR 2111
- For resonant and phase shifted PWM: IR 2112, IR 2113
- For buck-boost converters: IR 2125
- For 3-phase, six step, PWM: IR 30, IR 2132
- For oscillating application converters: IR 2155.

5.15.13 Comparison of IGBT and MOSFET

MOSFETs	*IGBTs*
1. In the power MOSFET, the decrease in the electron mobility with increasing temperature results in a rapid increase in the on-state resistance of the channel and hence the on-state drop.	1. In IGBTs, this increase in voltage drop is very small.
2. The on-state voltage drop increases by a factor of 3 between room temperature and 200°C.	2. Here with the identical conditions, the increment in the on-state voltage drop is very small.
3. All highest temperature, maximum current rating goes down to 1/3 value.	3. At high ambient temperature; IGBT is extraordinarily well suited.
4. Current sharing in multiple paralleled MOSFETs is comparatively poor than IGBTs.	4. Current sharing in multiple paralleled IGBTs is far better than power MOSFET.
5. The turn-on transients are identical to IGBTs.	5. Turn-on transients are identical to MOSFETs.
6. Power MOSFET is suited for applications that require low blocking voltages and high operating frequencies.	6. IGBT is the preferred device for applications that require high blocking voltages and lower operating frequencies.

5.16 GATE TURN-OFF THYRISTORS (GTOs OR LATCHING TRANSISTORS)

Previous chapters describes the thyristor and their use in power electronic applications. Also, we have seen that thyristors can block high voltage (several thousand volts) in the off-state and conduct large currents (several thousand amperes) in the on-state with only a small on-state voltage drop (a few volts). The most useful of all is their capability of being switched ON when desired by

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5.25 Draw and explain the output characteristics of n-channel enhancement mode MOSFET.

5.26 Draw electrical equivalent circuit of a power MOSFET and explain why are they preferred in the inverter application.

5.27 Draw and explain the switching behaviour of power-MOSFET.

5.28 What is the significance of safe-operating area of a power MOSFET? Name other operating limitations of a power MOSFET.

5.29 Discuss briefly the parallel operation of MOSFETs.

5.30 Briefly discuss the gate-drive design considerations of the MOSFET.

5.31 Briefly discuss the following gate-drive circuits for power MOSFETs:
- (i) Driving the MOSFET from TTL
- (ii) Emitter-follower driving circuit
- (iii) CMOS gate-drive circuits
- (iv) Op-amp emitter-follower driver circuit
- (v) Isolated-gate drive circuit

5.32 Briefly explain the sources of power-losses in the switching MOSFET.

5.33 Compare power BJTs with power MOSFETs.

5.34 Justify the following statements:
- (i) Power MOSFET is operated at high enough gate-source voltage to minimize the conduction losses.
- (ii) Parallel operation of MOSFETs can be done more easily as compared to thyristors.
- (iii) Antiparallel diode is connected across MOSFET.
- (iv) Operating frequency of power MOSFET is higher than that of a power BJT.

5.35 With the help of neat structural diagram and suitable waveforms, explain the operation of insulated-gate BJT. (IGBT).

5.36 Explain the following points with respect to IGBT:
- (i) Forward blocking capability.
- (ii) Reverse blocking capability, and
- (iii) Forward conduction mode.

5.37 Describe briefly the latch-ups in an IGBT.

5.38 Discuss the static latch-up and dynamic latch-ups in an IGBT.

5.39 Discuss the switching characteristics of the IGBT with the help of neat circuit diagrams and waveforms.

5.40 Explain the safe operating areas of an IGBT.

5.41 Briefly describe the gate-drive circuits for IGBT.

5.42 Justify the following statements:
- (i) IGBT uses a vertically oriented structure
- (ii) IGBT combines the advantages of MOSFET and power BJT
- (iii) IGBT is preferred as a power switch over both the power BJT and MOSFET
- (iv) Punch-through IGBT structures are more popular and are widely used.

5.43 Compare SCR, Power BJT, MOSFET and IGBT on the basis of following parameters:

(i) operating frequency	(ii) trigger circuit
(iii) drop	(iv) snubbers
(v) V-I rating	(vi) Applications

5.44 Briefly explain the V-I characteristics of an IGBT.

5.45 Explain the basic difference between non-punch-through IGBTs and punch-through IGBTs.

5.46 Explain the operating principle of an IGBT on the basis of:
   (i) creation of an inversion-layer
   (ii) conductivity modulation of the drift layer

5.47 Draw and explain the equivalent circuit for modelling the operation of the IGBT.

5.48 Explain the parallel operation of IGBT. Also, highlight the problems faced while parallel-operation.

5.49 Briefly explain the gate-drive design considerations of IGBTs.

5.50 Draw and explain the IGBT driver circuit with overcurrent protection.

5.51 Draw and explain the functional block-diagram of IC IR 2110. Also, draw the typical waveforms.

5.52 How does a GTO differ from a conventional thyristor. Give its circuit symbol.

5.53 With the help of a neat structural diagram, explain the operation of GTO.

5.54 Explain briefly the switching behaviour of a GTO.

5.55 Describe the turn-off process in a GTO with the help of appropriate voltage and current waveforms.

5.56 Briefly discuss the overcurrent protection of GTOs.

5.57 Derive the expression for turn-off gain of GTO. Also, discuss on the magnitude of this parameter for reliable turn-off of GTO.

5.58 With the help of basic structural diagram explain the operation of static induction transistor. Also, list the applications of SIT.

5.59 Give the merits and demerits of a GTO as compared to a conventional SCR.

5.60 With the help of a neat structural diagram, explain the operation of static induction thyristors.

5.61 With the help of structure diagram and equivalent circuit, explain the behaviour of a MOS-controlled thyristor.

5.62 Justify: MCT is a GTO with MOS-controlled gate.

5.63 Explain the operating principle of *N*-MCT by neatly sketching the cross-sectional view and equivalent circuit diagram.

5.64 Explain the operating principle of *P*-MCT by neatly sketching the cross-sectional view and equivalent circuit diagram.

5.65 Briefly discuss the turn-on and turn-off behaviour of *N*-MCT

5.66 Briefly explain the turn-on and turn-off behaviour of *P*-MCT.

5.67 Comment on the I-V characteristics of MCT.

5.68 Draw and explain the switching characteristics of MCT.

5.69 Explain the following timing parameters related to MCT:
   (i) turn-on delay time and current rise time
   (ii) turn-off delay time and fall time

5.70 Justify: *P*-MCT can turn-off a current approximately three-times larger than an *N*-MCT.

5.71 Explain the effect of temperature on the operation of MCT.

5.72 Explain briefly the safe-operating area of MCT.

5.73 Briefly describe the operation of IGCT.

5.74 Explain the following terms with reference to IGCT:
(i) Buffer layer (ii) Transparent emitter
(iii) Reverse conduction (iv) Controlled diode recovery

5.75 Explain with the help of neat diagrams the basic principle of operation of MTO.

5.76 Describe the basic principle of operation of ETO.

5.77 Explain briefly the nonuniform and uniform turn-on process of ETO with the help of neat waveforms.

5.78 Draw and explain the operation of ETO gate-drive circuit.

5.79 With the help of neat waveforms, explain the snubberless turn-off process of ETO.

5.80 Compare MTO and IGCT briefly.

5.81 Compare MTO and ETO on the basis of:
(i) speed (ii) gain
(iii) efficiency (iv) control method
(v) maximum ratings

PROBLEMS

5.1 The circuit shown in Fig. P 5.1 is used to control the power dissipated in the 10Ω load resistor. Assume that the bilateral switching diode has a breakdown voltage of ± 2.8 V and that the holding voltage of the diode and Triac are negligible.
The applied sinusoidal voltage is 300 V RMS, at 60 Hz.
(i) Compute the conduction angle.
(ii) Draw the waveform of the voltage applied to the load.
(iii) Compute the total power dissipated by the load resistor.

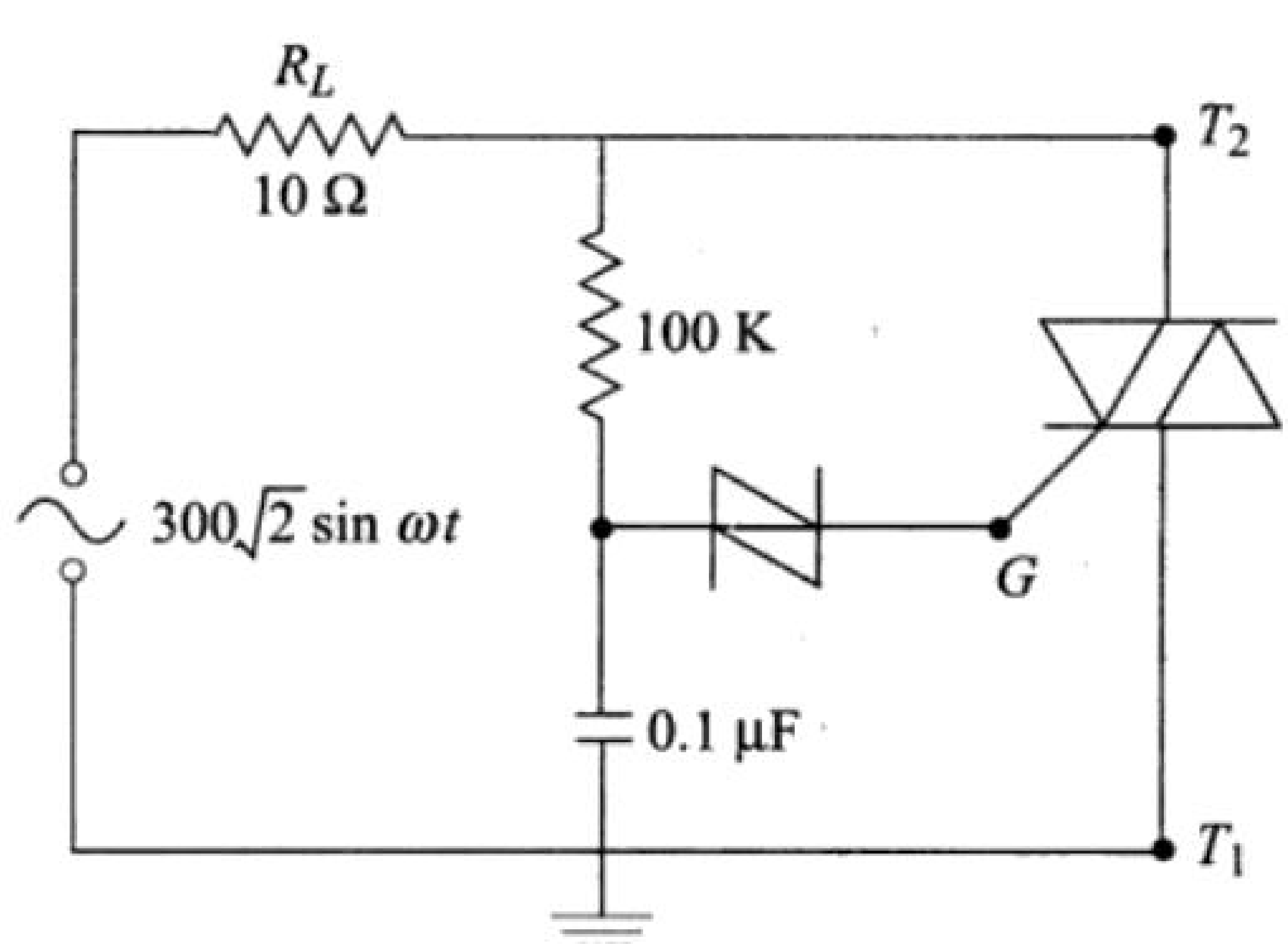

Fig. P 5.1

[*Ans* (i) Conduction angle = 103.5°; (iii) Total power dissipated = 5.81 kW]

5.2 Figure P 5.2 shows an SCR used in a over-heater detector circuit. The thermistor used in the circuit is a temperature sensitive resistor; its resistance increases with temperature. The SUS shown in the circuit has V_s = 8 V.

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The operation of the circuit on inductive loads changes slightly. Now at instant t_{01}, when the thyristor is triggered, the load-current will increase in a finite-time through the inductive load. The supply voltage from this instant appears across the load. Due to inductive load, the increase in current is gradual. Energy is stored in inductor during time t_{01} to t_1. At t_1, the supply voltage reverses, but the thyristor is kept conducting. This is due to the fact that current through the inductance cannot be reduced to zero.

During negative-voltage half-cycle, current continues to flow till the energy stored in the inductance is dissipated in the load-resistor and a part of the energy is fed-back to the source. Hence, due to energy stored in inductor, current continuous to flow upto instant t_{11}. At instant, t_{11}, the load-current is zero and due to negative supply voltage, thyristor turns-off.

At instant t_{02}, when again pulse is applied, the above cycle repeats. Hence the effect of the inductive load is increased in the conduction period of the SCR.

The half-wave circuit is not normally used since it produces a large output voltage ripple and is incapable of providing continuous load-current.

The average value of the load-voltage can be derived as:

$$E_{dc} = \frac{1}{2\pi} \int_{\alpha}^{\pi+\alpha} E_m . \sin \omega t \, d(\omega t)$$

Here, it has been assumed that in negative half-cycles, the SCR conducts for a period of α.

$$\therefore \quad E_{dc} = \frac{E_m}{2\pi} [- \cos \omega t]_{\alpha}^{\pi+\alpha} \quad \text{Or,} \quad E_{dc} = \frac{E_m}{\pi} \cos \alpha \qquad (6.6)$$

From Eqs (6.1) and (6.6), it is clear that the average load-voltage is reduced in case of inductive load. This is due to the conduction of SCR in negative cycle.

6.3.3 Effect of Freewheeling Diode

Many circuits, particularly those which are half or uncontrolled, include a diode across the load as shown in Fig. 6.9. This diode is variously described as a commutating diode, flywheel diode or by-pass diode. This diode is commonly described as a commutating diode as its function is to commutate or transfer load current away from the rectifier whenever the load-voltage goes into a reverse-state.

This diode serves two main functions:

(i) It prevents reversal of load voltage except for small diode voltage-drop.
(ii) It transfers the load current away from the main rectifier, thereby allowing all of its thyristors to regain their blocking states.

Figure 6.10 shows a half-wave controlled rectifier with a freewheeling diode D_f connected across R–L load. The load-voltage and current waveforms are also shown in Fig. 6.11.

With diode D_f, thyristor will not be able to conduct beyond 180°.

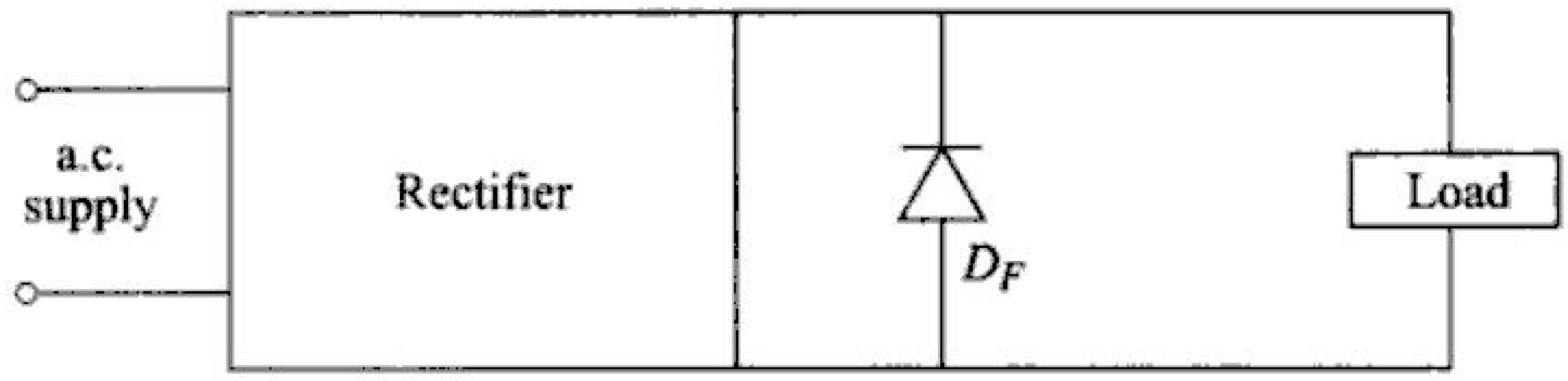

Fig. 6.9 *Position of commutating diode D_F*

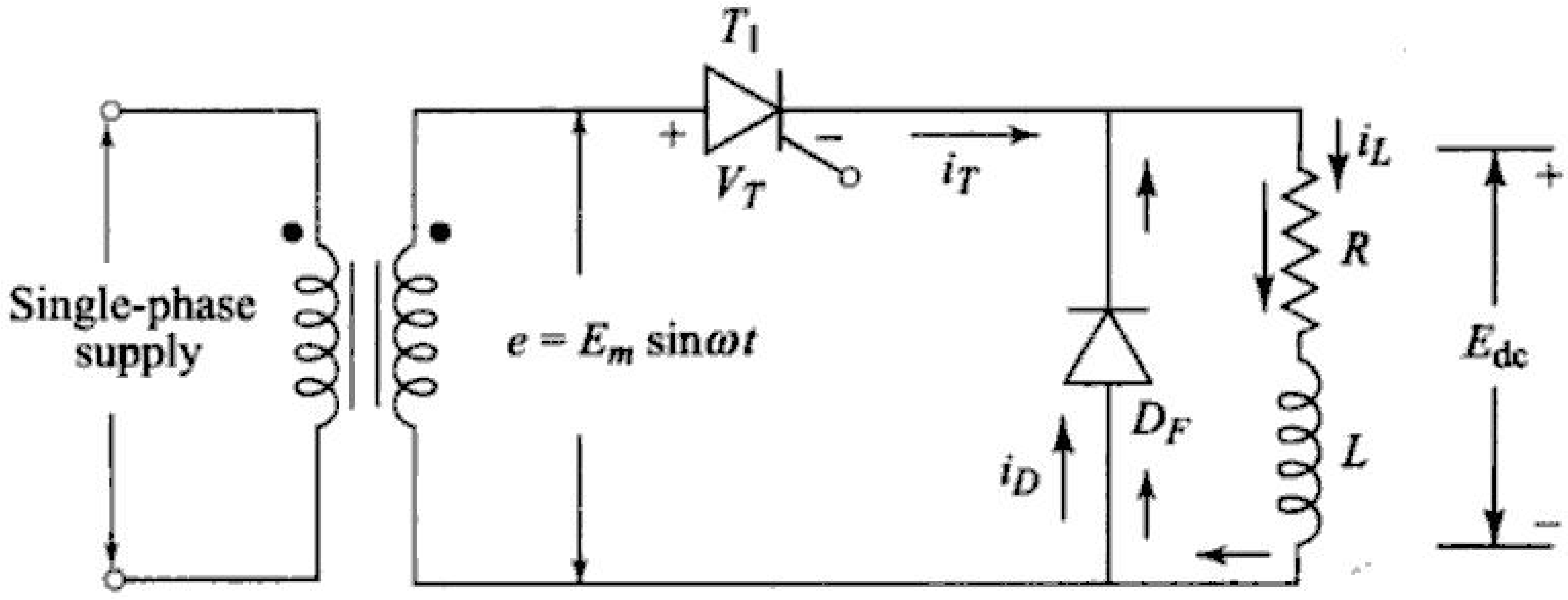

Fig. 6.10 *Half-wave rectifier with a freewheeling diode*

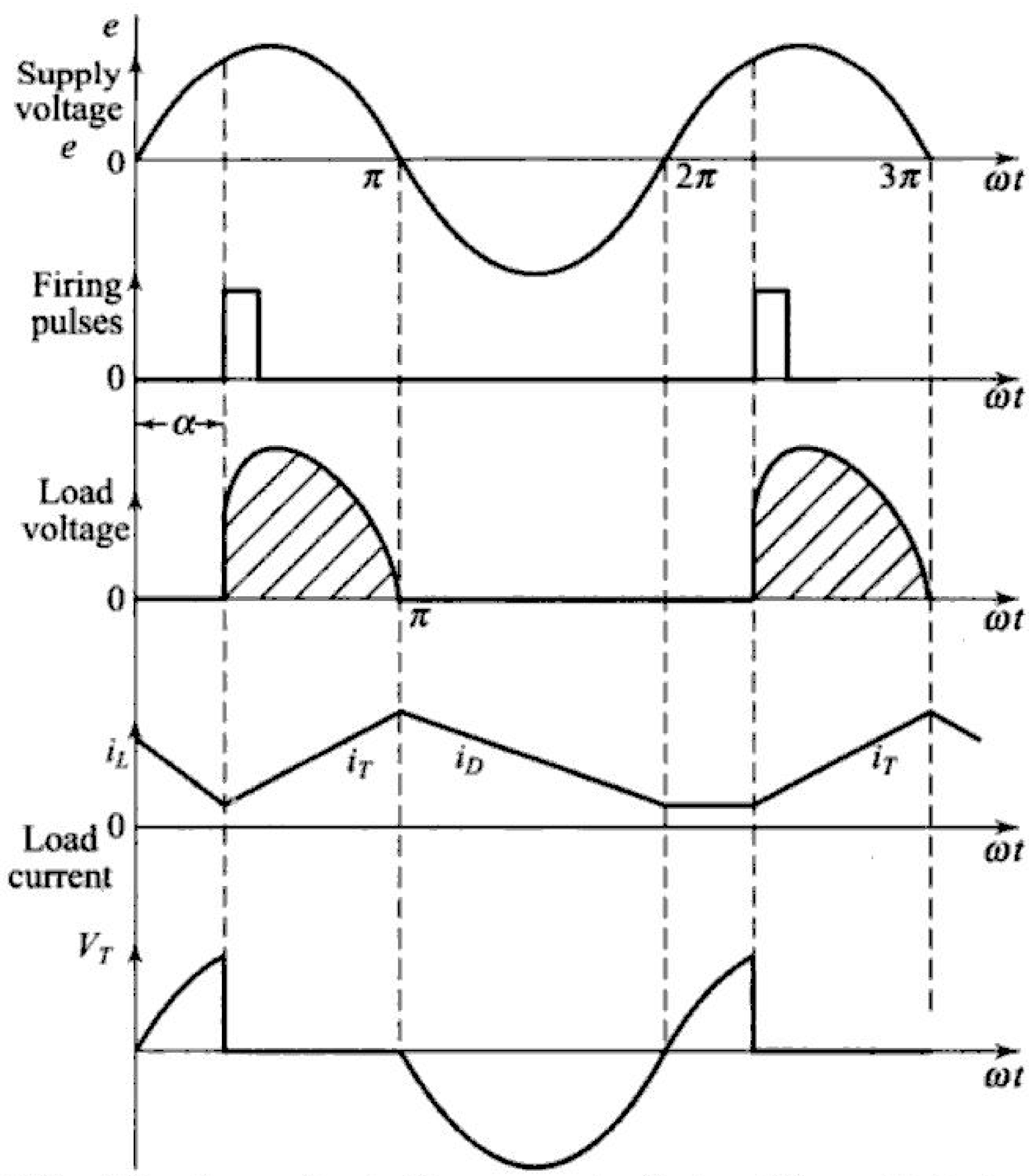

Fig. 6.11 *Waveforms for half-wave controlled-rectifier with inductive load and freewheeling diode*

We know that during the positive half-cycle, voltage is induced in the inductance. Now, this induced voltage in inductance will change its polarity as the di/dt changes its sign and diode D_f will start conducting as soon as the induced voltage is of sufficient magnitude, thereby enabling the inductance to discharge its stored energy into the resistance.

Hence, after 180°, the load current will freewheel through the diode and a reverse-voltage will appear across the thyristor. The power flow from the input takes place only when the thyristor is conducting. If there is no freewheeling diode, during the negative portion of the supply voltage, thyristor returns the energy stored in the load inductance to the supply line. With diode D_f, the free-wheeling action takes place and no power will be returned to the source. Hence, the ratio of the reactive power flow from the input to the total power consumed in the load is less for the phase-control circuit with a freewheeling diode. In other words, the freewheeling diode improves the input power-factor.

Mathematically:

$$\frac{EI \sin \phi}{EI} = \text{less} \quad \therefore \sin \phi = \text{less} \tag{6.7}$$

Since, ϕ = less $\therefore$ Power-factor $\cos \phi$ = more (6.8)

Hence it is clear that the freewheeling diode helps in improvement of power-factor of the system.

SOLVED EXAMPLES

Example 6.1 If the half-wave controlled rectifier has a purely resistive load of R and the delay angle is $\alpha = \pi/3$. Determine:

(a) Rectification efficiency (b) Form factor (c) Ripple factor
(d) Transformer utilization factor (e) Peak inverse voltage for SCR T_1

Solution:

(a) Rectification efficiency $\eta = \dfrac{p_{dc}}{p_{ac}}$ where, p_{dc} = dc load power = E_{dc}^2/R and

p_{ac} = rms load power = $\dfrac{E_{rms}^2}{k}$. We have the relation, from Eq. (6.1),

$$E_{dc} = \frac{E_m}{2\pi}(1 + \cos \alpha), \text{ Since, } \alpha = \pi/3 \quad \therefore E_{dc} = 0.239\, E_m$$

Also, from equation (6.4), we have

$$E_{rms} = E_m \left[\frac{\pi - \alpha}{4\pi} + \frac{\sin 2\alpha}{8\pi}\right]^{1/2}$$

For firing angle $\alpha = \pi/3$, $E_{rms} = 0.485\, E_m$

$$\because \text{ Rectification efficiency } \eta = \frac{(0.239\, E_m)^2}{(0.485\, E_m)^2} \quad \therefore \quad \eta = 24.28\%$$

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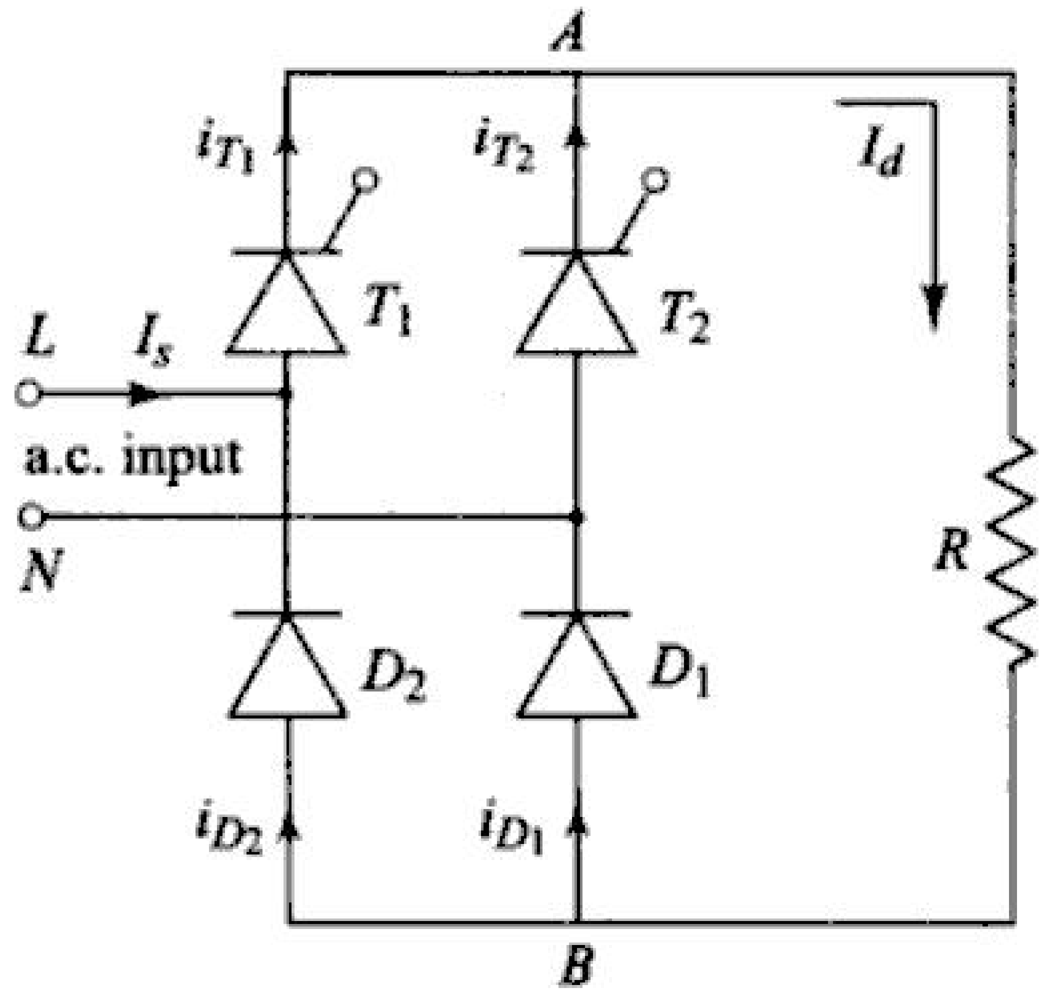
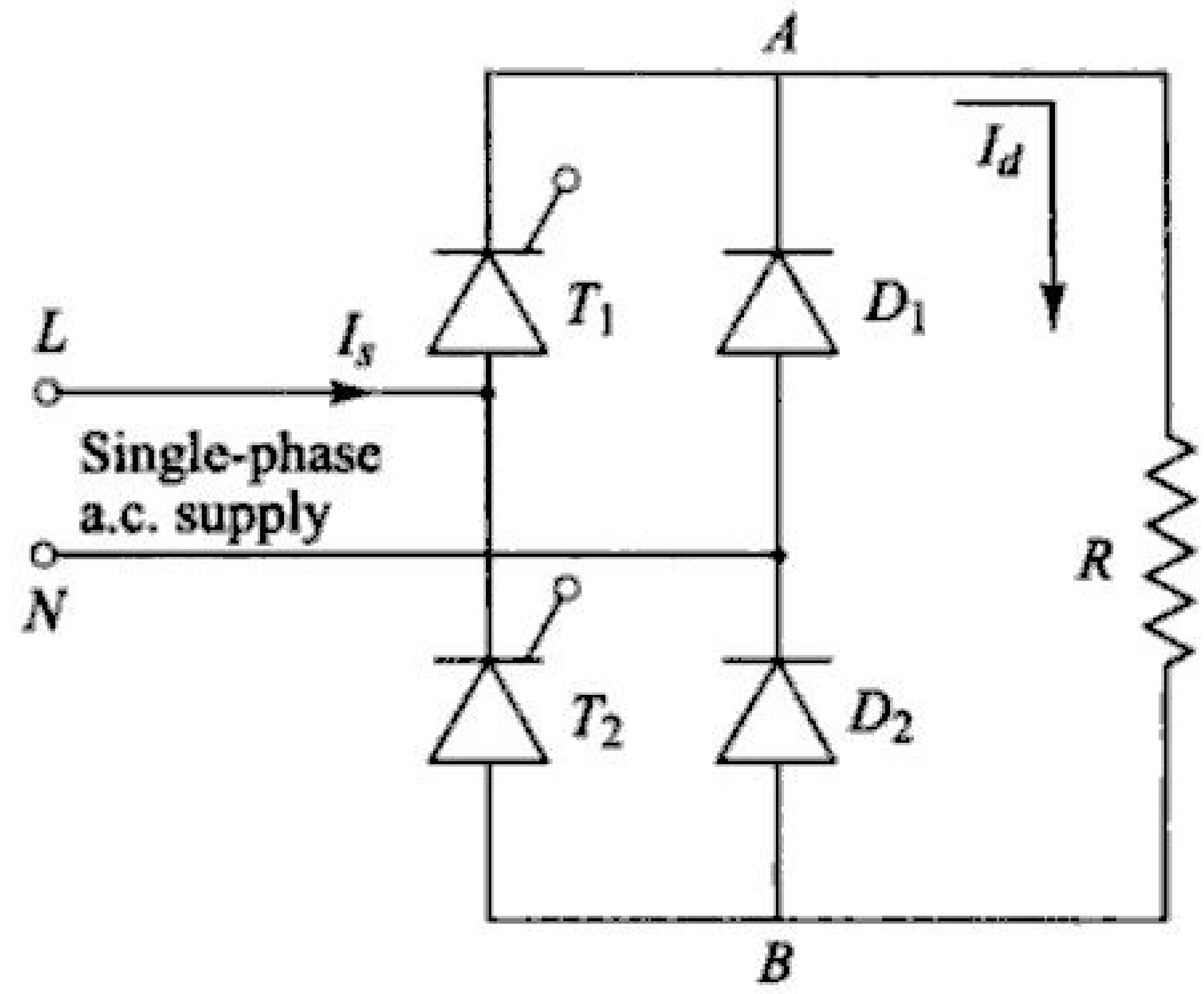


(a) Symmetrical-configuration



(b) Asymmetrical-configuration

Fig. 6.24 *Half controlled-bridge circuits*

In a symmetrical configuration, the cathodes of two SCRs are at the same potential so their gates can be connected and a single gate-pulse can be used for triggering either SCR. The SCR which is forward-biased at the instant of firing will turn-on. In asymmetrical configuration, separate-triggering circuits are to be used. The different-waveforms of symmetrical converter-circuit is shown in Fig. 6.25.

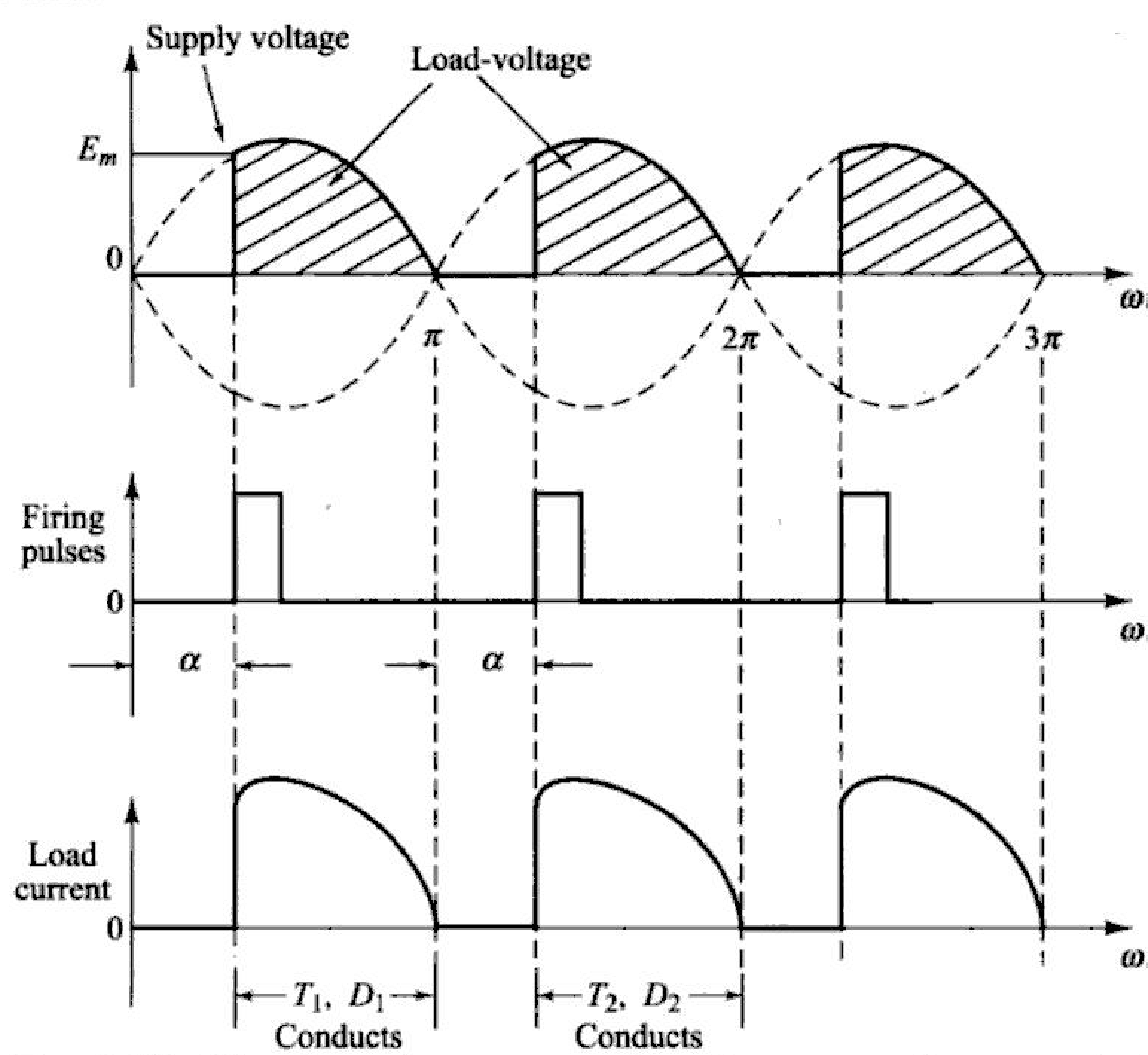


Fig. 6.25 *Waveforms for symmetrical configuration with resistive load*

Now, consider the symmetrical configuration of half-controlled bridge-circuit. During the positive half-cycle of the a.c. supply, thyristor T_1 and diode D_1 are forward-biased and are in the forward-blocking mode. When the SCR T_1 is triggered, at a firing-angle α, the current flow through the path L—T_1—R—D_1—N. As shown in Fig. 6.25, the load-current will flow until it is commutated by reversal of supply voltage at $\omega t = \pi$.

During the negative half-cycle of the a.c. supply, thyristor T_2 and diode D_2 are forward-biased. When SCR T_2 is triggered at an angle $(\pi + \alpha)$, the current would flow through the path N— T_2 —A—R—B—D_2 —L. This current is continuous till angle 2π, when SCR T_2 is turned-off.

The voltage and current-relations are derived as follows:

(i) ***Average d.c. load-voltage:***

$$E_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi} E_m . \sin \omega t \, d(\omega t)$$

$$= \frac{1}{\pi} E_m [-\cos \omega t]_{\alpha}^{\pi} = \frac{E_m}{\pi}[1 + \cos \alpha] \tag{6.17}$$

(ii) ***Average load-current:***

$$I_d = \frac{E_m}{\pi R}[1 + \cos \alpha]$$

(iii) ***RMS load-voltage:*** The RMS load voltage for a given firing angle α is given by

$$E_{rms} = \left[\frac{E_m^2}{\pi}\int_{\alpha}^{\pi} \sin^2 \omega t \, d(\omega t)\right]^{1/2} = E_m\left[\frac{1}{\pi}\int_{\alpha}^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right). d(\omega t)\right]^{1/2}$$

$$= E_m\left[\frac{1}{2\pi}\left(\omega t - \frac{\sin 2\omega t}{2}\right)_{\alpha}^{\pi}\right]^{1/2} = E_m\left[\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right]^{1/2} \tag{6.18}$$

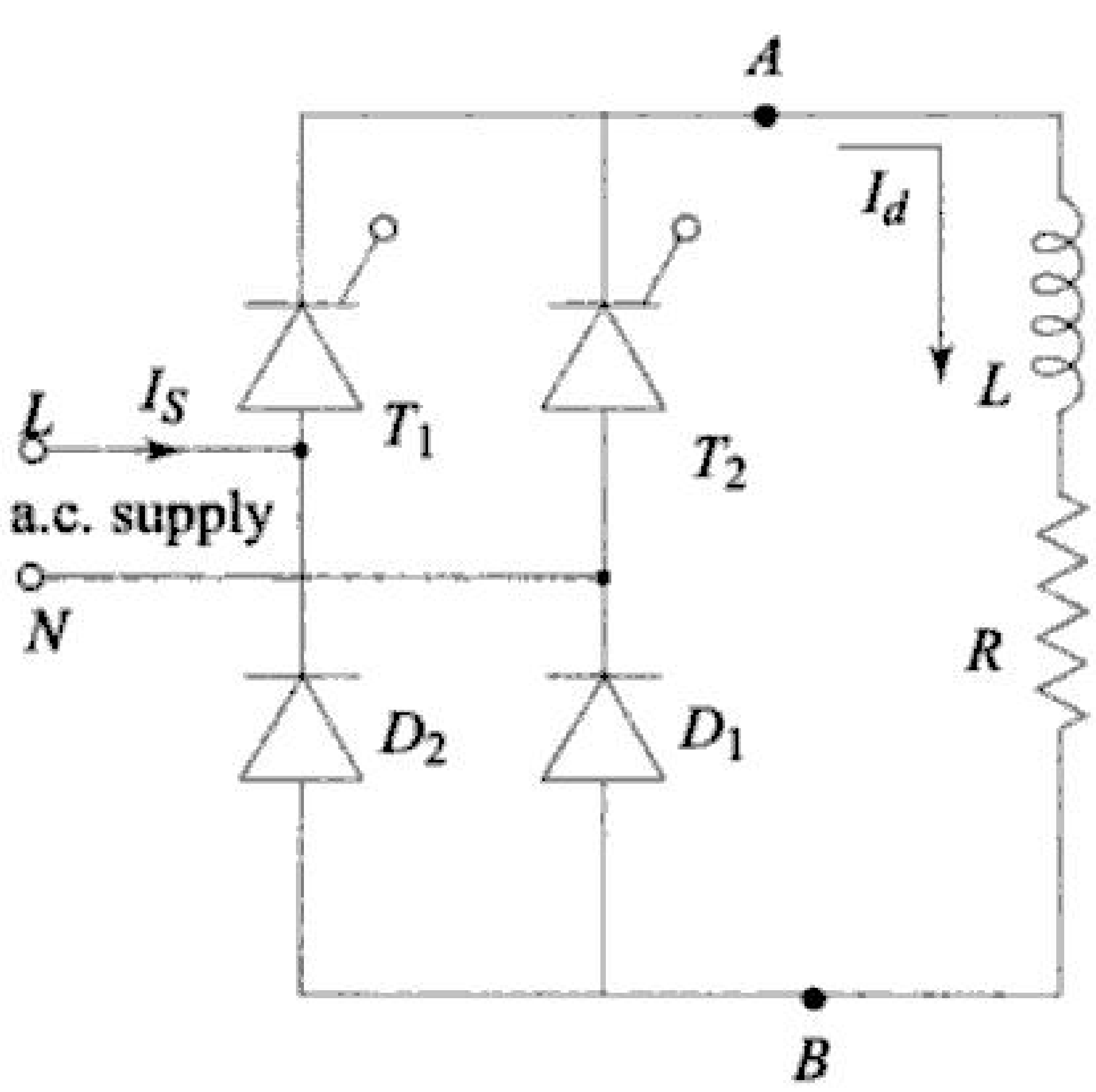
6.5.2 Half Controlled Bridge Rectifier with *R-L* Load

Figure 6.26 shows two alternative arrangements of 2-pulse half-controlled bridge converters with inductive load. The various voltage and current waveforms for both symmetric and asymmetric configurations are shown in Fig. 6.27. Consider the symmetrical circuit configuration. As shown in Fig. 6.27(a), thyristor T_1 is turned-on at a firing angle α in each positive half-cycle. From this instant α, supply voltage appears across output terminals AB, through thyristor T_1 and diode D_1. Current flows through the path L—T_1—A—L—R—B—D_1—N. Here, the filter inductance L is assumed to be sufficiently large as to produce continuous load current. This current I_d is taken to be constant. Hence during positive half-cycle, thyristor T_1 and diode D_1 conducts.

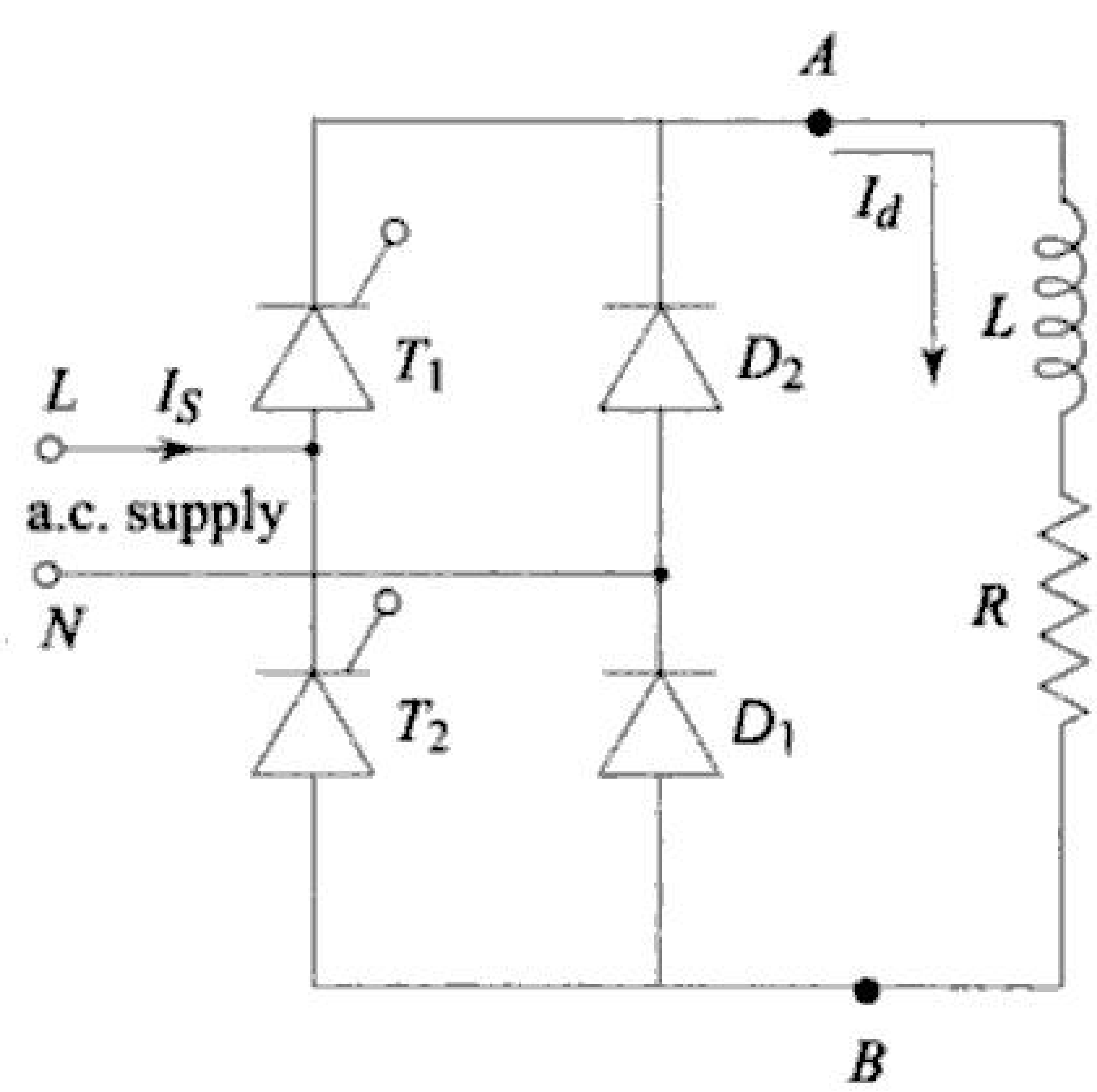
Now, when the supply voltage reverses at $\omega t = \pi$, the diode D_2 is forward-biased since diode D_1 is already conducting. The diode D_2 then turns ON, and the load current passes through D_2 and T_1. The supply voltage reverse-biases D_1 and turns it off. Thus, the load-current freewheels through the path R—B—D_2—T_1—A—L during the interval from π to $(\pi + \alpha)$ in each supply-cycle.

During the negative half-cycle, at the instant $(\pi + \alpha)$, a triggering-pulse is applied to the forward-biased thyristor T_2. Thyristor T_2 is turned ON. As thyristor T_2 is turned ON, the supply voltage reverse-biases T_1 and then turns it OFF by the line commutation. Therefore, the load-current flows through T_2 and D_2, the above-cycle repeats and the waveforms obtained are as shown in Fig. 6.27(a), which are similar to that of fully-controlled converter with a freewheeling diode. Here, we have seen that the conduction period of thyristors and diodes are equal, therefore this circuit is called as the symmetrical configuration.

Now consider the circuit of Fig. 6.26(b). During the positive half-cycle of the a.c.-supply, thyristor T_1 and diode D_1 are forward-biased. As shown in Fig. 6.27(b), thyristor T_1 is turned ON at firing angle α. Current flows through the path L—T_1—A—L—R—B—D_1—N. Hence, T_1 and D_1 conduct from α to π. Similarly, T_2 and D_2 conduct from $(\pi + \alpha)$ to 2π in each negative half-cycle of the a.c. supply. The freewheeling action is provided by diodes D_1 and D_2 from 0 to α and from π to $(\pi + \alpha)$ in each supply cycle. In this converter configuration, the conduction periods of thyristors and diodes are unequal. Hence this circuit configuration is known as the asymmetrical configuration.



(a) Symmetrical configuration



(b) Asymmetrical configuration

Fig. 6.26

In the above discussion, we have seen that the thyristor conducts for a longer interval in the symmetrical circuit configuration. Therefore, the thyristors used in this circuit must have a higher average current-rating compared to those in the asymmetrical-circuit configuration.

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(ii) This voltage is zero when $\alpha = 90°$.
(iii) This voltage is negative maximum when $\alpha = 180°$.

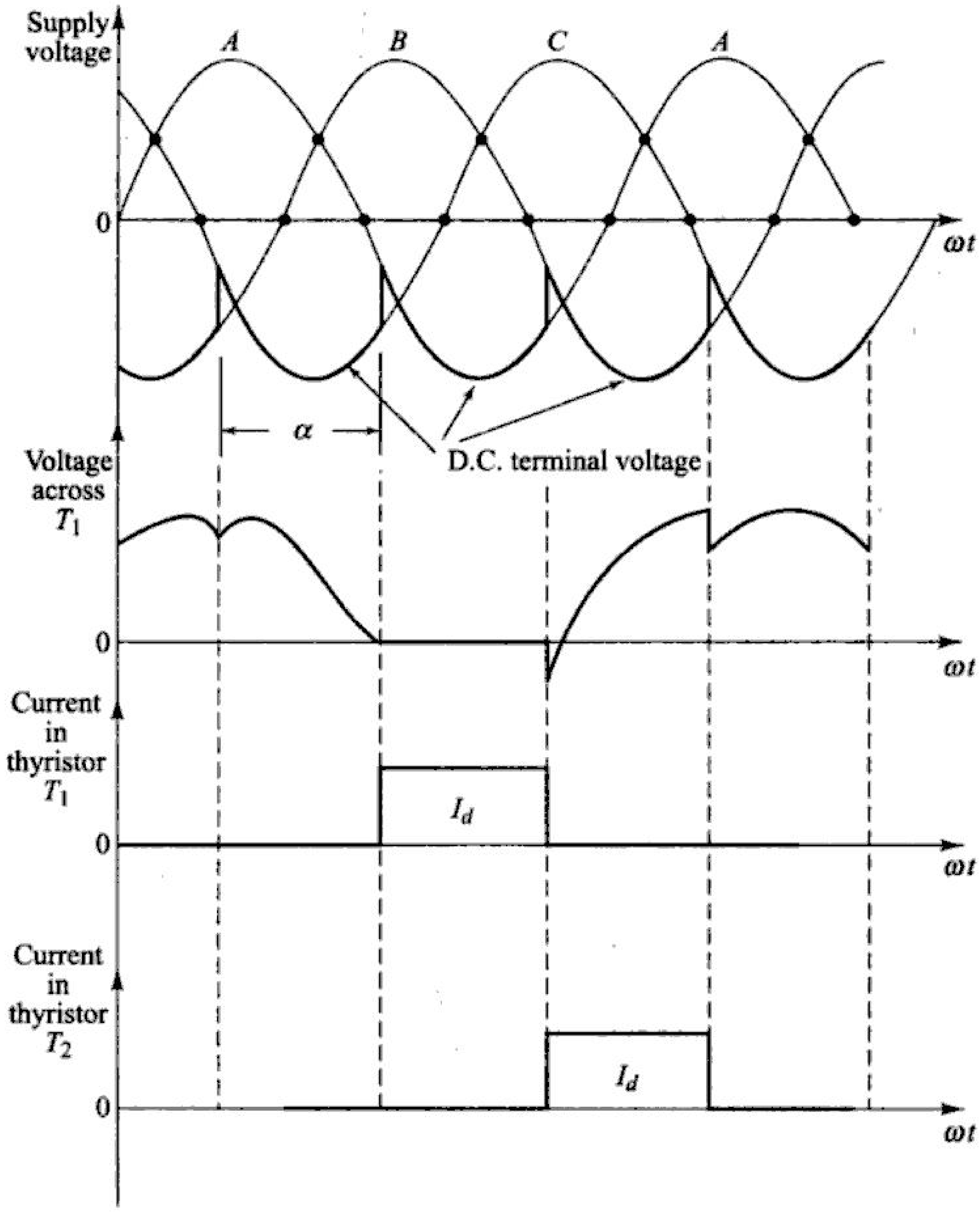

Fig. 6.33 *(e) Voltage and current waveforms for $\alpha = 180°$*

The product of voltage and current is the instantaneous value of power. For the phase angle between 0 and 90°, the average value of power is positive, indicating a flow of energy from the a.c. system to the d.c. circuit. With $\alpha = 90°$, the positive and negative value of power are in balance so that effective power becomes zero. For $\alpha > 90°$, the average power is negative, so that energy is transmitted from the d.c. circuit to the a.c. system.

In the above analysis, we have assumed that the current waveform in each transformer secondary, which is the same as the associated thyristor current waveform consists of a unidirectional or "half-wave" rectangular "block" having a duration of 120°. But this waveform contains a direct component having an amplitude of $I_d/3$. Therefore, if a simple star connected transformer secondary is used to

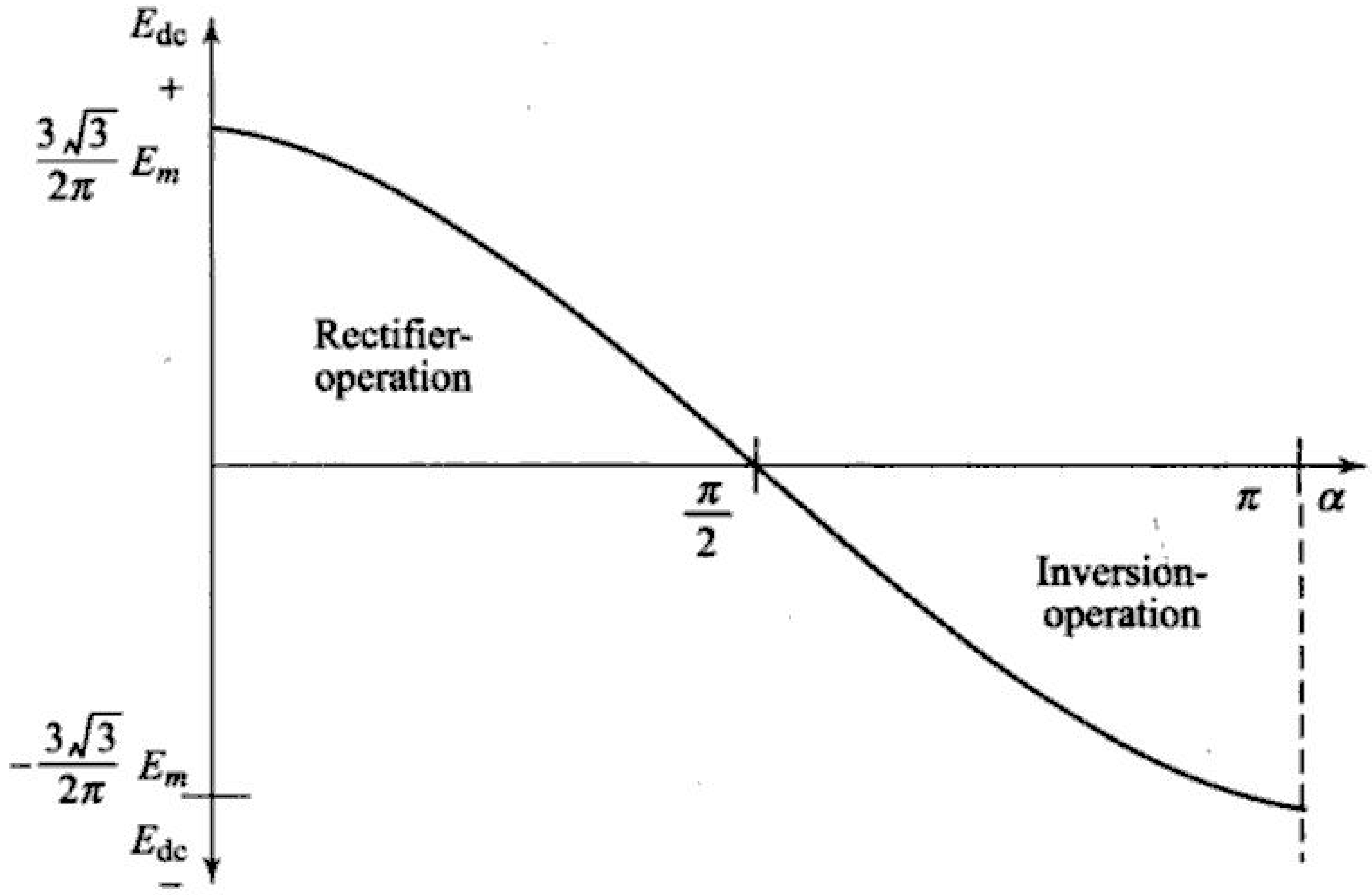

Fig. 6.34 *Graph of E_{dc} vs. α*

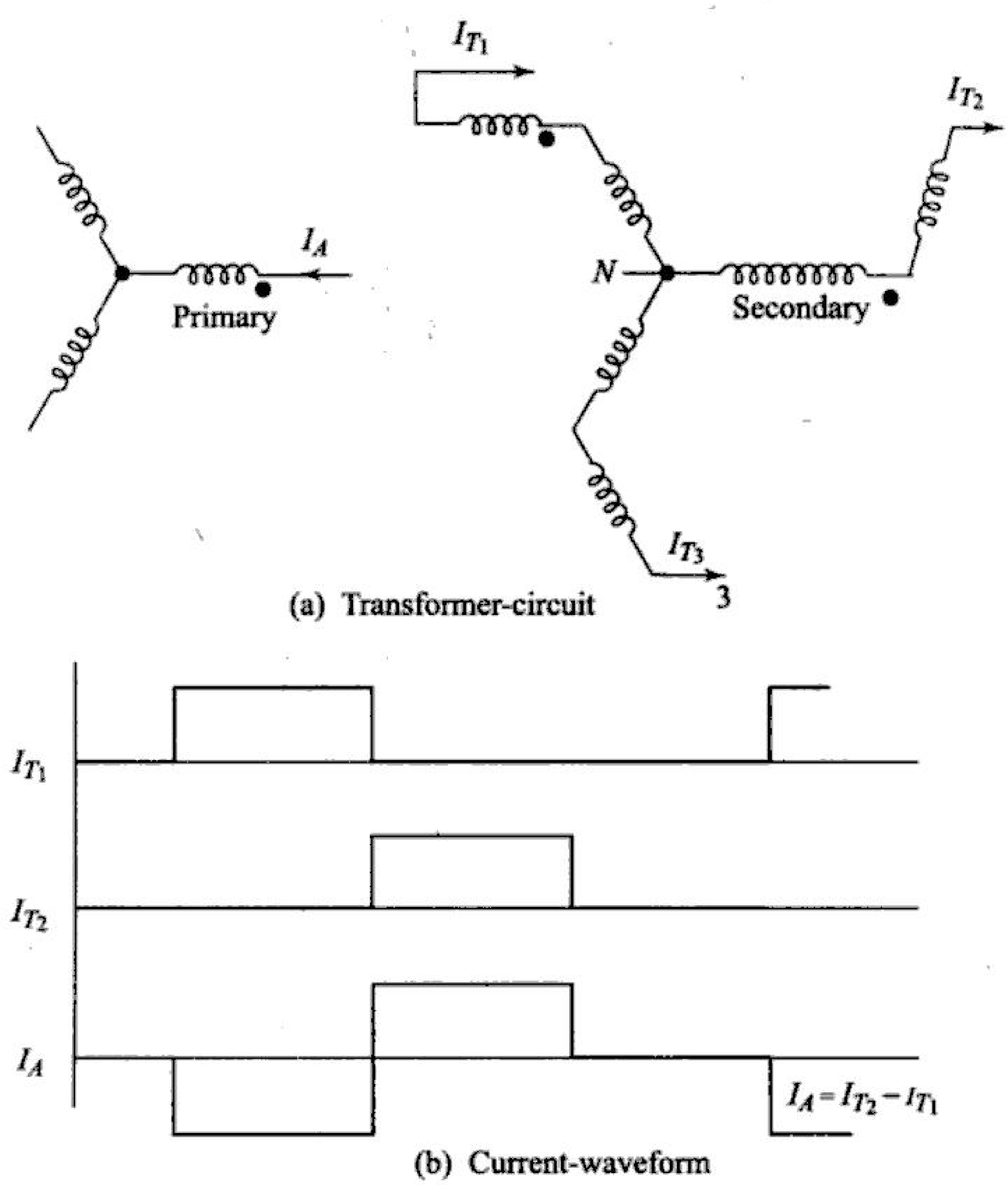

Fig. 6.35 *Zig-zag connection*

carry this current, then a d.c. magnetisation of the transformer core results. To avoid this problem, the interconnected star called as the zig-zag connection, shown in Fig. 6.35(a), is used as the secondary of the supply-transformer. The current which is reflected into the primary is now a.c. as shown in Fig. 6.35(b), being as much positive as negative, hence avoiding any d.c. component in the core mmf.

6.9.3 Effect of Freewheeling Diode

The circuit of three-pulse mid-point converter with freewheeling diode is shown in Fig. 6.36. The related waveforms, which assumes a perfectly smooth load-current, are shown in Fig. 6.37. For firing angles less than 30°, the d.c. terminal voltage of the converter is always positive, and the freewheeling diode does not come into operation. As the firing angle is retarded beyond this point, so the load current starts to freewheel through the diode for certain periods, thus cutting off the input line current, and preventing the d.c. terminal load voltage from swinging into the negative direction.

Hence, the effect of the freewheeling diode is to cause a reduction of ripple voltage of the d.c. terminals, and, at the same time, to divert the load current away from the input lines. The total range of firing angle control required for this circuit is 150°.

Solved Examples

Example 6.12 A three-phase half-wave controlled rectifier has a supply of 200 V/phase. Determine the average load voltage for firing angle of 0°, 30°, 60°, assuming a thyristor volt drop of 1.5 V and continuous load current.

Solution: From Eq. (6.45), we have

$$E_{dc} = \frac{3\sqrt{3}}{2\pi} E_m . \cos\alpha - \text{drop across SCR} = \frac{3\sqrt{3}}{2\pi} 200\ \sqrt{2}\ \cos\alpha - 1.5$$

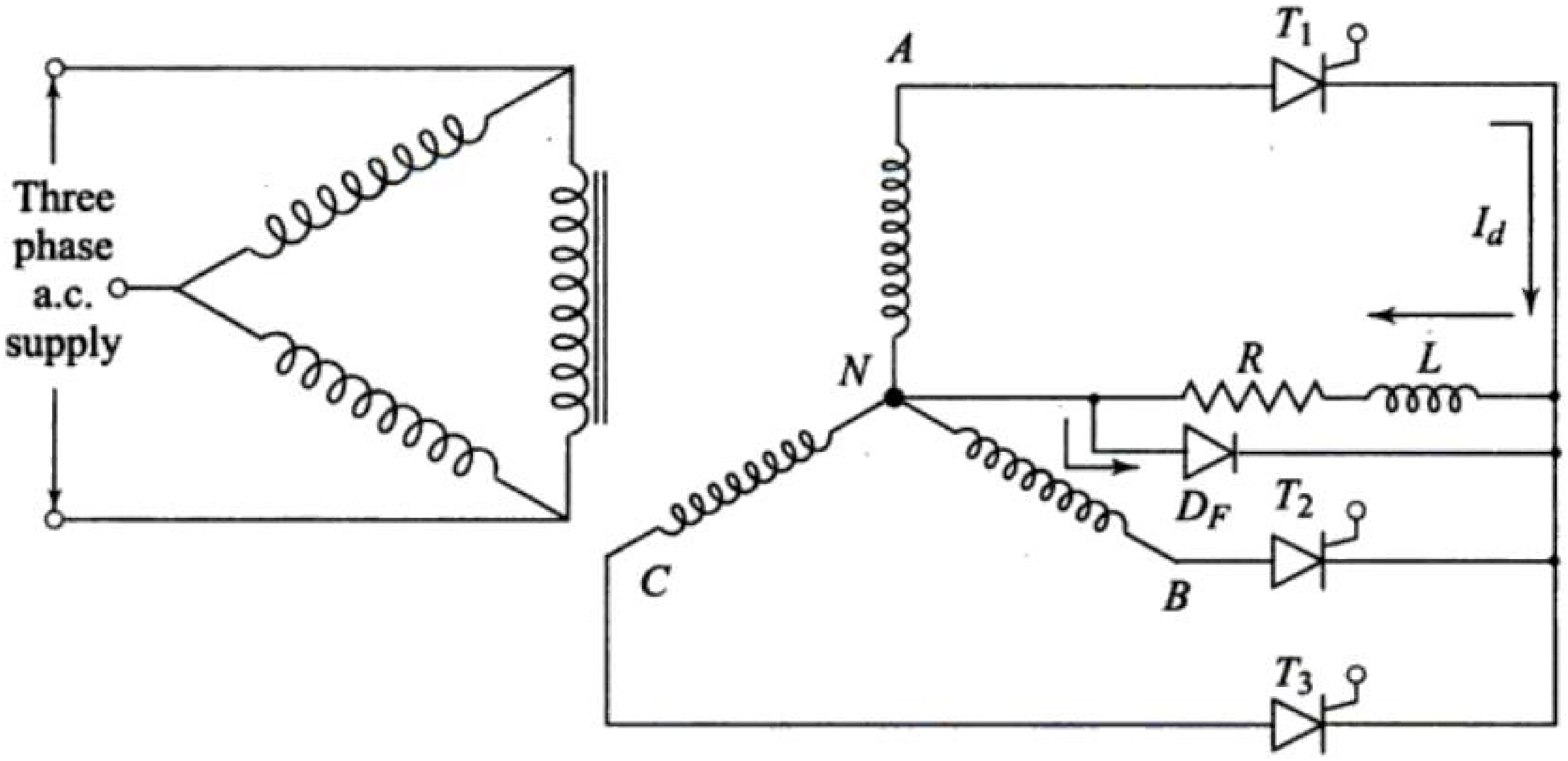

Fig. 6.36 *Three-pulse mid-point converter with a freewheeling diode*

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(ii) For $\alpha \leq 60°$, the supply current waveforms are of 120° in each half cycle and for $\alpha > 60°$ (not shown in figure) it is less than 120°, i.e. $(180° - \alpha)$ in each half-cycle.

(iii) For $\alpha \leq 60°$, the SCR waveform is 120° wide and for $\alpha > 60°$, it is $(180° - \alpha)°$ wide.

(iv) PIV rating of SCR is $\sqrt{3}\ E_m$.

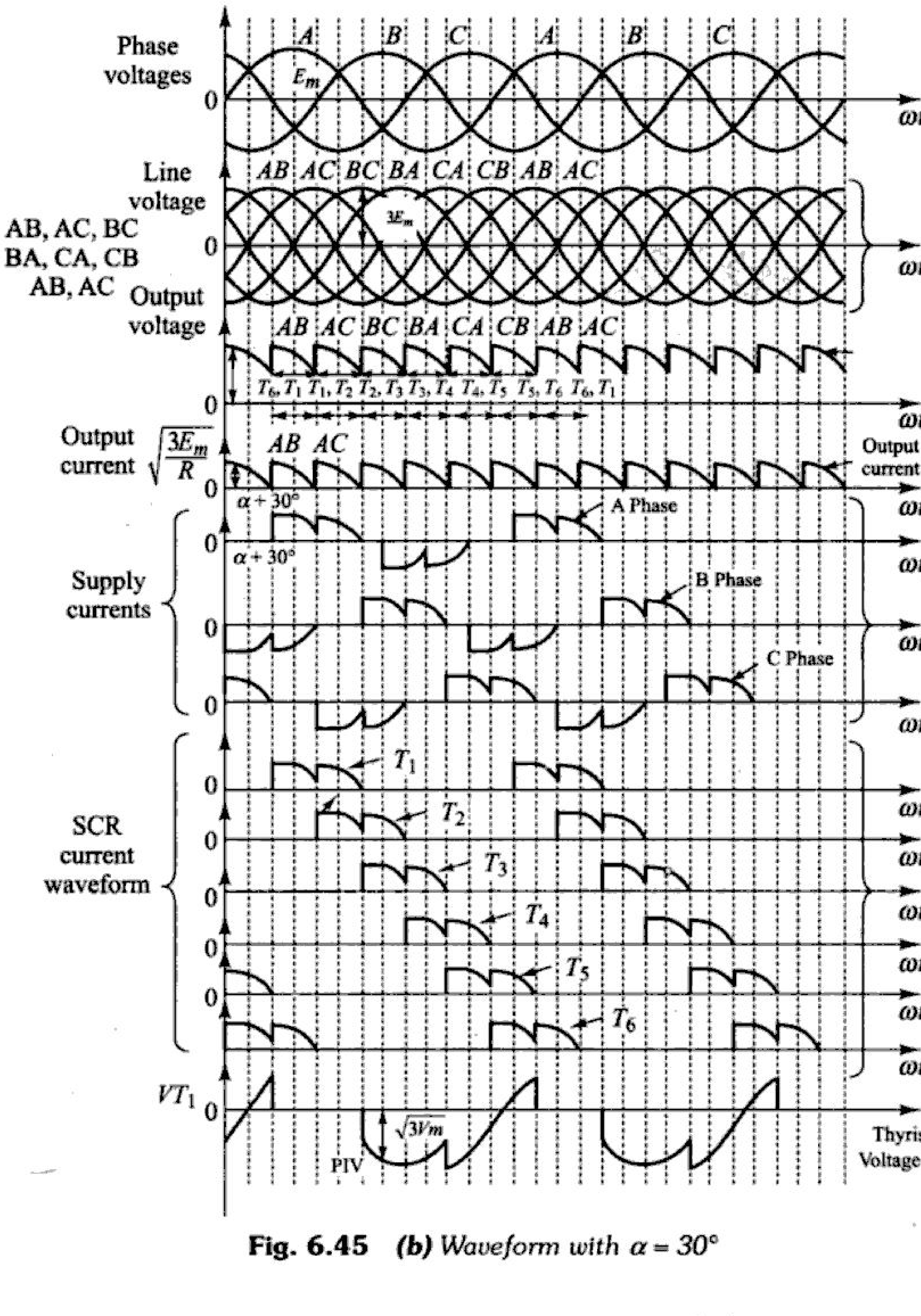

Fig. 6.45 ***(b)*** *Waveform with $\alpha = 30°$*

6.11.2 With Inductive Load (R-L)

The power diagram of the three-phase fully-controlled converter with R-L load is shown in Fig. 6.45. The output voltage waveforms with firing angles are shown in Fig. 6.46 (a). The load inductance is assumed to be very large so as to produce a constant load current.

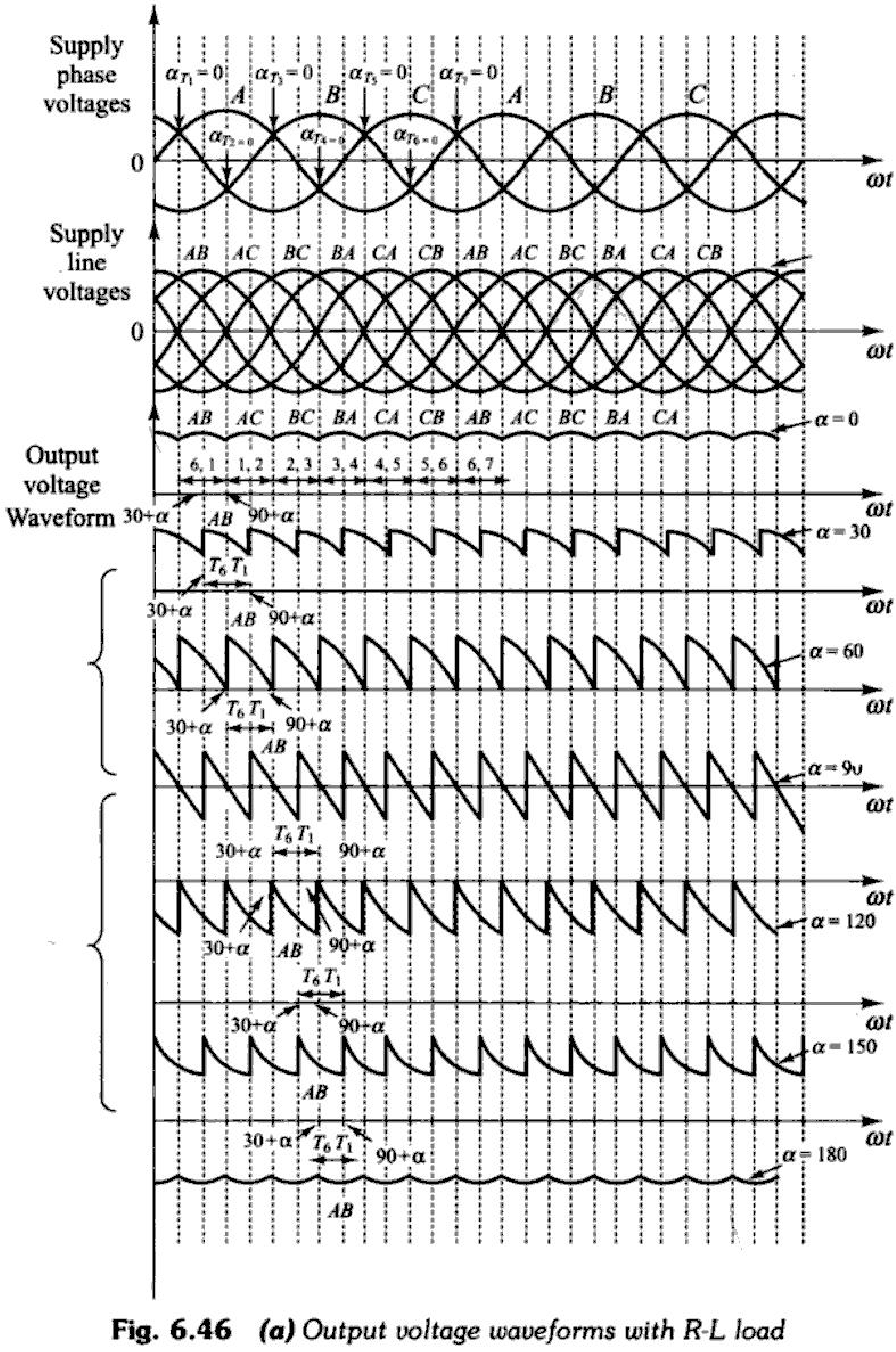

Fig. 6.46 *(a) Output voltage waveforms with R-L load*

Following points can be noted from the waveforms of Fig. 6.46.

(i) Waveforms are similar with R-load for $\alpha = 0°$, $30°$, and $60°$.

(ii) For $\alpha > 60°$, the waveforms are different. The voltage goes negative due to the inductive nature of the load. The previous thyristor pair continuous to conduct till the next SCR is triggered. For examples T_6 and T_1 continuous to conduct upto $(90 + \alpha)$ till thyristor T_2 is triggered and when T_2 is triggered it commutates the SCR T_6 and then T_1 and T_2 starts conducting.

(iii) For $\alpha = 90°$, the area under the positive and the negative cycle are equal and the average voltage is zero.

(iv) For $\alpha < 90°$, average output voltage is positive and for $\alpha > 90°$, the average output voltage is negative.

(v) The maximum value of α is 180°.

(vi) The output is always a six pulse, i.e. ripple frequency is 300 Hz irrespective of the value of α.

Expression for Average Output Voltage and RMS Output Voltage:

(i) Average Output Voltage

From Fig. 6.46, we can write:

$$\text{Average output voltage, } E_{dc} = 6 \times \frac{1}{2\pi} \int_{30+\alpha}^{90+\alpha} E_{Ry(\omega t)}\, d\omega t$$

$$= \frac{3}{\pi} \int_{30+\alpha}^{90+\alpha} \sqrt{3}\, E_m \sin(\omega t + 30)\, d\omega t = \frac{3}{\pi} \int_{60+\alpha}^{120+\alpha} \sqrt{3}\, E_m \sin(\omega t)\, d\omega t$$

$$= \frac{3\sqrt{3}\, E_m}{\pi} [\cos(\omega t)]_{120+\alpha}^{60+\alpha} = \frac{3\sqrt{3}}{\pi} E_m [\cos(60+\alpha) - \cos(120+\alpha)]$$

$$E_{dc} = \frac{3\sqrt{3}\, E_m}{\pi} \cos\alpha \text{ for } 0 \le \alpha \le 180° \tag{6.52}$$

where E_m is the peak-value of the live-to neutral voltage.

As the firing angle changes from 0 to 90°, the voltage also changes from maximum to zero and the converter is said to be in *rectification mode*. For the angles in the range 90° to 180°, the voltage varies from 0 to negative maximum and the converter is in the *inversion mode*. It can transfer power from d.c. side to a.c. if there is a negative d.c. source available at the d.c. terminals. The mean value of the d.c. voltage is superimposed by ripple content.

(ii) R.M.S. Output Voltage

$$E_{rms} = \left[\frac{1}{2\pi} \int_0^{2\pi} E_{dc}^2(\omega t)\, d\omega t\right]^{1/2} = \left[6 \times \frac{1}{2\pi} \int_{30+\alpha}^{90+\alpha} E_{AB}^2(\omega t)\, d\omega t\right]^{1/2}$$

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Since $\sin(120 + 2\alpha) - \sin(240 + 2\alpha) = \sqrt{3}\cos 2\alpha$ and $120° = 2\pi/3$, we get

$$E_{\text{rms}} = \left\{\frac{9E_m^2}{4\pi}\left[\frac{2\pi}{3} + \frac{\sqrt{3}}{2}(1 + \cos 2\alpha)\right]\right\}^{1/2} = \frac{3}{2}E_m\left[\frac{2}{3} + \frac{\sqrt{3}}{2\pi}(1 + \cos 2\alpha\right]^{1/2} \tag{6.55}$$

Case II $\alpha > 60°$, RMS output voltage is given by:

$$E_{\text{rms}} = \left[\frac{3}{2\pi}\int_{30+\alpha}^{210} \cdot E_{\text{AC}}^2(\omega t)\,\mathrm{d}\omega t\right]^{1/2} = \left[\frac{3}{2\pi}\int_{30+\alpha}^{210}\left(\sqrt{3}\,E_m \sin(\omega t - 30\right)^2 \mathrm{d}\,\omega t\right]^{1/2}$$

$$= \left[\frac{9E_m^2}{2\pi}\int_{30+\alpha}^{210}\sin^2(\omega t - 30)\,\mathrm{d}\omega t\right]^{1/2} = \left[\frac{9E_m^2}{2\pi}\int_{\alpha}^{180}\sin^2\omega t\,\mathrm{d}\omega t\right]^{1/2}$$

$$= \left[\frac{9E_m^2}{4\pi}\int_{\alpha}^{180}(1 - \cos 2\,\omega t)\,\mathrm{d}\omega t\right]^{1/2}$$

$$= \frac{3}{2}E_m\left\{\frac{1}{\pi}\left[(180 - \alpha) + \frac{1}{2}(\sin(2\,\omega t))\right]_{180}^{\alpha}\right\}^{1/2}$$

$$= \frac{3}{2}E_m\left\{\frac{1}{\pi}\left[(180 - \alpha) + \frac{1}{2}(\sin 2\alpha - \sin(360°)\right]\right\}^{1/2}, \quad \pi = 180°$$

$$\therefore \quad E_{\text{rms}} = \frac{3E_m}{2}\left[\frac{\pi - \alpha + 1/2\sin 2\,\alpha}{\pi}\right]^{1/2} \tag{6.56}$$

Devices Ratings: SCRs and diode conducts only for 120° for $\alpha \le 60°$ and for $(180° - \alpha)$ for $\alpha \ge 60°$.

(a) Case I $\alpha \le 60°$

(i) SCR and diode rms current ratings:

$$I_{\text{T(rms)}} = I_{\text{D(rms)}} = \frac{I_{\text{dc (rms)}}}{\sqrt{3}} = \frac{\text{rms value of output current}}{\sqrt{3}}$$

(ii) Average current ratings:

$$I_{\text{D(avg)}} = I_{\text{T(avg)}} = \frac{I_{\text{dc (avg)}}}{3} = \frac{\text{Average value of output current}}{3}$$

(b) Case II $\alpha > 60°$, $I_{\text{T(rms)}} = I_{\text{D(rms)}} = \dfrac{I_{\text{dc (rms)}}}{\sqrt{3}}$

$$I_{T(avg)} = I_{d(avg)} = \frac{I_{dc}}{3},\ I_{T(peak)} = I_{D(peak)} = \frac{E_m}{R_L} \quad (6.57)$$

$$\text{PIV} > \sqrt{2}\ E_m, \text{ and } I_{dc(rms)} = \frac{E_{rms}}{R_L} = \frac{\text{RMS value of ouput voltage}}{R}$$

6.12.2 Operation with Inductive Load

Waveforms for semiconverter with large inductive load are shown in Fig. 6.49 (b). The following points can be observed from the Fig. 6.49 (b):

(i) The voltage waveform is same as that with resistive (R) load. Hence, the average and rms values of the output voltage waveform are same and are given by Eqs. (6.54), (6.55) and (6.56).

(ii) **Continuous conduction mode:** The output current waveform is continuous for $\alpha < 60°$, and is ripple free as shown for $\alpha = 30°$. Thus, the form-factor (FF) of current waveform is unity and the ripple factor is zero. The peak value of current I_{dc}.

(iii) **Discontinuous conduction mode:** For firing angles $\alpha > 60°$, the discontinuous mode occurs, as shown for $\alpha = 90°$. It can be observed from the waveforms that the output voltage becomes zero during a part of the output voltage period because of the freewheeling action.

(iv) Supply current waveform is a quasi-square wave for any $\alpha \le 60°$. For any $\alpha > 60°$, the pulse width per half-cycle decreases to $(180 - \alpha)$, *i.e.* less than 120°. The peak value of the current waveform is I_{dc}.

(v) SCR and diode current waveform for any α, $0 \le \alpha \le 180°$ is a rectangular wave of duration 120°, i.e. of duty-cycle 1/3. The peak value of the waveform is I_{dc}.

(vi) PIV rating of SCRs and diode is $\sqrt{3}\ E_m$.

(vii) The maximum value of α is 180°

(viii) For $\alpha > 60°$, freewheeling action takes place when the output voltage is zero.

(ix) Operation of the circuit can be understand with the help of following points:

(a) The source current is equal to load current I_{dc} when either the SCR or the diode is conducting otherwise the source current is zero.

(b) In general, if SCR conducts means phase current is positive and if diode conducts, the phase current is negative. Phase current is zero when neither device is conducting.

(c) Devices conducting current is equal to load current I_{dc}.

(x) **Half-waving effect:** For large firing angle delays, commutation failure may take place due to the limited time available in the symmetrical 3-ϕ semiconverter circuit configuration, if the current is assumed to be continuous. This may result "in-half-waving effect". That is, the converter operates as an uncontrolled half wave converter. This effect is shown in Fig. 6.49 (c), with the thyristor. T_1 in conduction and the firing pulses to

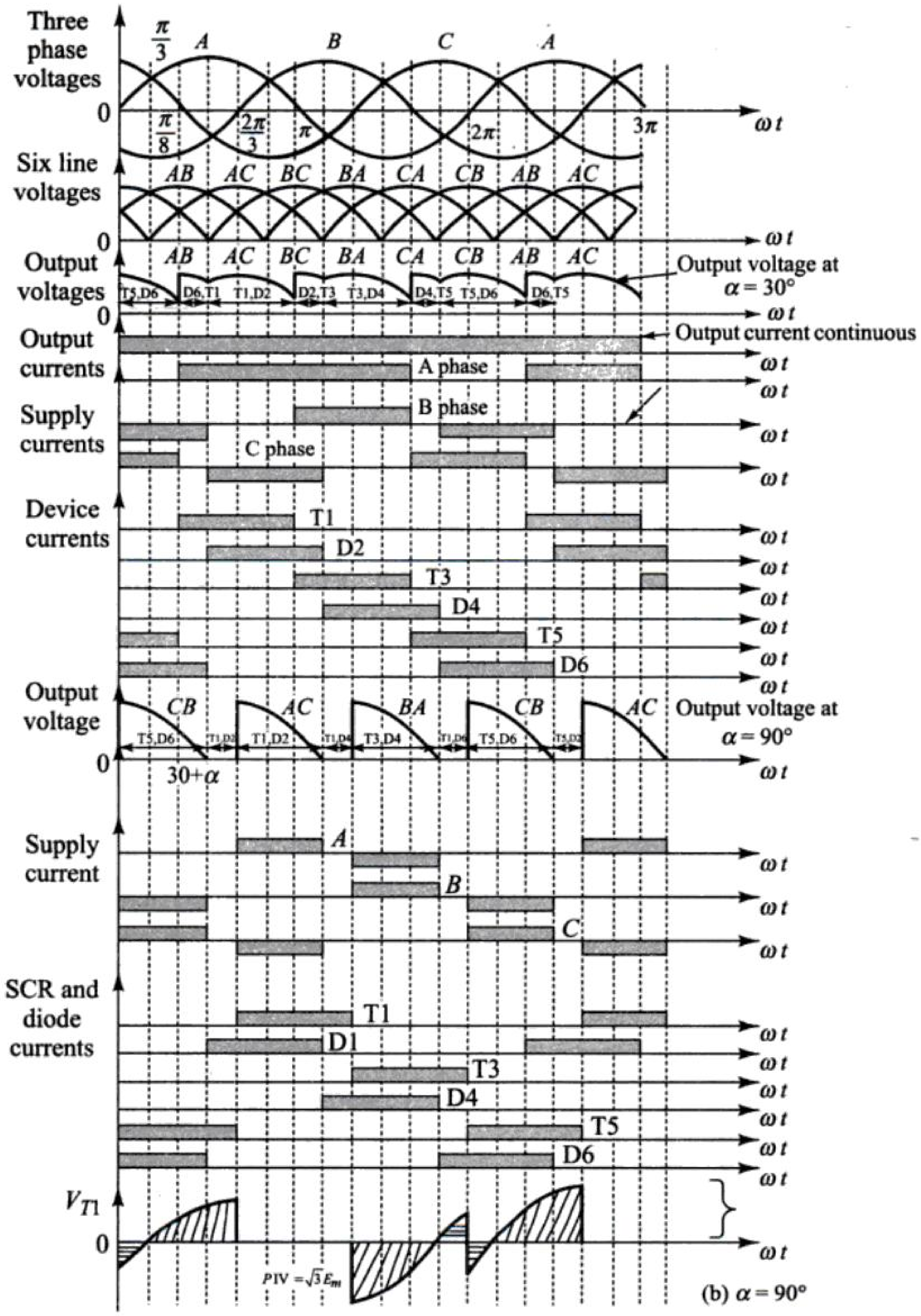

Fig. 6.49 ***(b)*** *Waveforms for α = 30° and α = 90°*

SCRs T_3 and T_5 are inhibited. For the condition shown in Fig. 6.49 (c), the output voltage becomes uncontrolled being E_{AB} or E_{AC} for 120° each.

Prior to the half-waving effect, the waveforms are shown for α = 120° in Fig. 6.49 (c). The ripple in the output current becomes quite appreciable. The thyristor current is the same as the load current, since the thyristor conducts all the times. This effect can be eliminated by connecting a freewheeling diode

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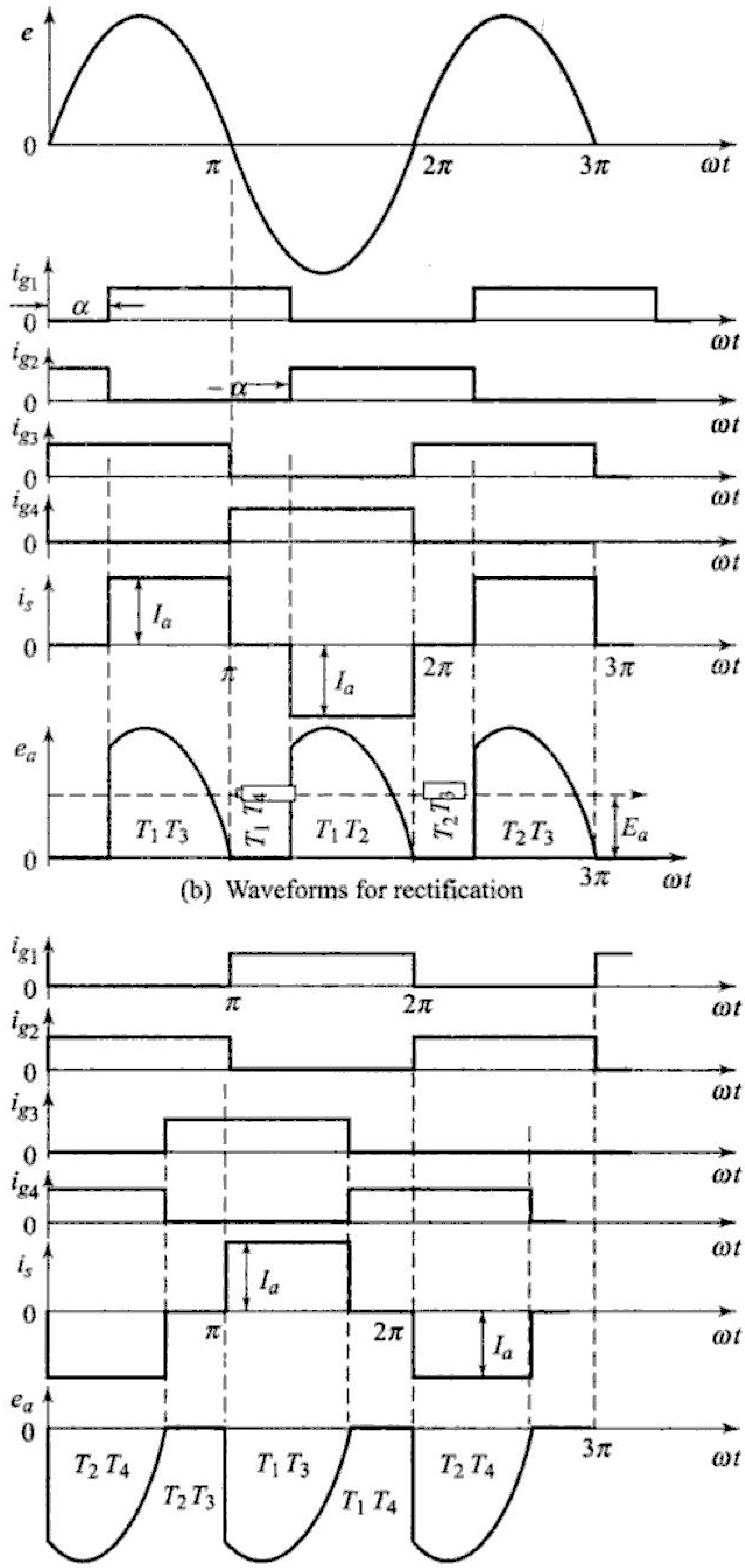


(b) Waveforms for rectification

(c) Waveforms for inversion

Fig. 6.56 ***(b)** and **(c)** Semiconverter operation of a full converter*

In the inversion mode (Fig. 6.56(c)), thyristors T_1 and T_2 are gated during the whole of the negative and positive half-cycles, respectively, of the supply voltage so that they behave as diodes during their respective half-cycles. The firing angle for SCRs T_3 and T_4 is varied to change the output voltage.

When two SCRs of the same leg (such as T_1 and T_4 or T_2 and T_3) conduct, the motor current freewheels through them producing zero output voltage. The nature of the motor terminal voltage e_a and the supply current i_s is the same as that in a semiconverter system. Therefore, performance is improved at the cost of complexity in the control logic circuit.

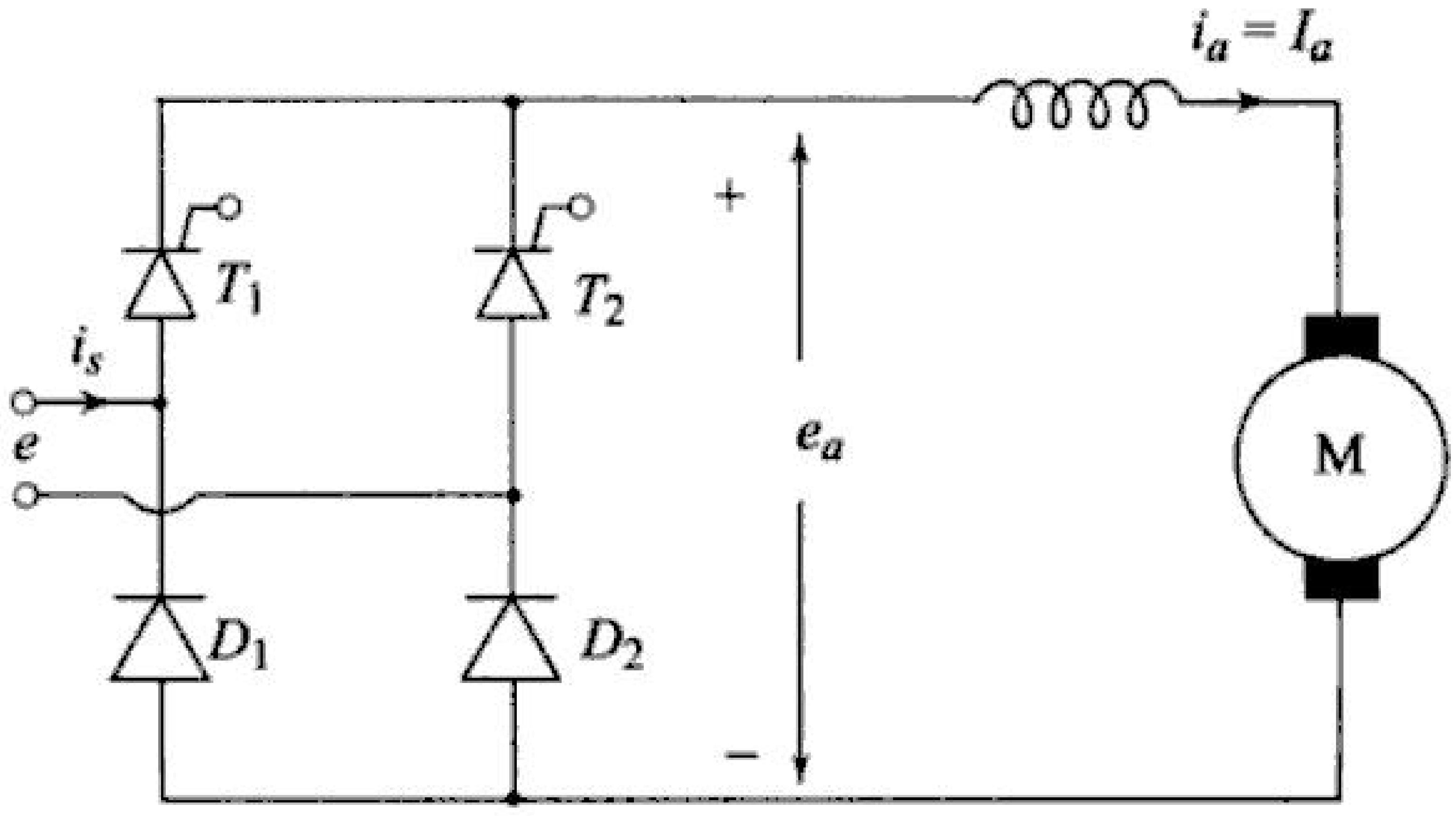
Another interpretation of the foregoing control scheme is as follows: In the rectification mode, the firing of the negative group of thyristors (T_3 and T_4) is kept at zero. Therefore, when the firing angle of the positive group of thyristors T_1 and T_2 is zero, the output voltage is maximum; when it is 180°, the output voltage is zero. In the inverting mode, the triggering of the positive group of thyristor is kept at 180° and when the firing angle for the negative group is also 180°, the output voltage has its maximum negative value. In practice, the firing angle must be limited to less than 180° in all cases to allow a margin for commutation. As the firing angle for T_3 and T_4 is reduced from 180°, the output voltage becomes less negative. This interpretation helps in understanding the application of this control scheme in three-phase full converters, where it is called sequential control. The firing angle for the positive group of SCRs is kept constant at zero and that for the negative group of thyristors is varied for the rectification mode. For the inversion mode, the firing angle for the positive group is varied, and that for the negative group is kept at 180°. This control scheme, although it improves power factor in both single-phase and three-phase converters, is not recommended for three-phase converters because of three major disadvantages:

(a) Even harmonic currents are present in the supply line current.
(b) Third harmonic ripple is present in the output.
(c) There is a danger of commutation failure.

6.17.3 Asymmetrical Firing

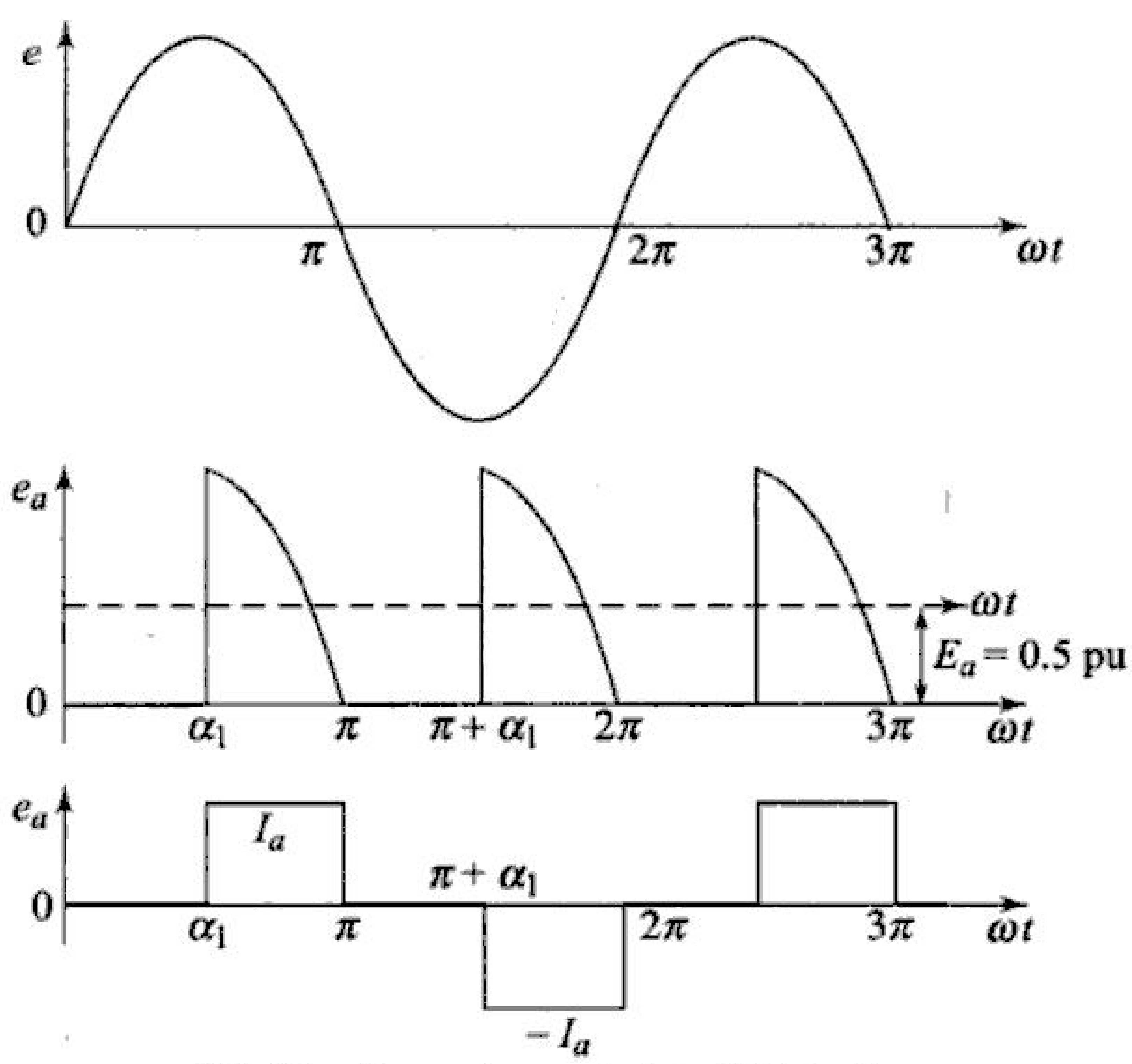
The improvement in power factor can be achieved by a technique known as asymmetrical firing, shown in Fig. 6.57(c). In this scheme thyristors are triggered at different angles, whereas in the symmetrical firing scheme (Fig. 6.57(b) both thyristors are triggered at the same firing angle. For example, if 0.5 p.u. average output voltage is required, SCRs are triggered at $\alpha = 90°$ in the symmetrical firing scheme. To obtain the same average output voltage in the asymmetrical firing scheme, if SCR T_1 is triggered at $\alpha_1 = 60°$, then SCR T_2 is triggered at $\alpha_2 = 120°$. Since one SCR is triggered at a lower value of the firing angle, the power factor is slightly improved in asymmetrical firing. However, asymmetrical firing produces several disadvantages. It generates d.c. and even harmonic currents in the supply line current.

The d.c. component can, however, be avoided if the firing angles are alternated in successive cycles. If sufficient inductance is not present in the motor armature

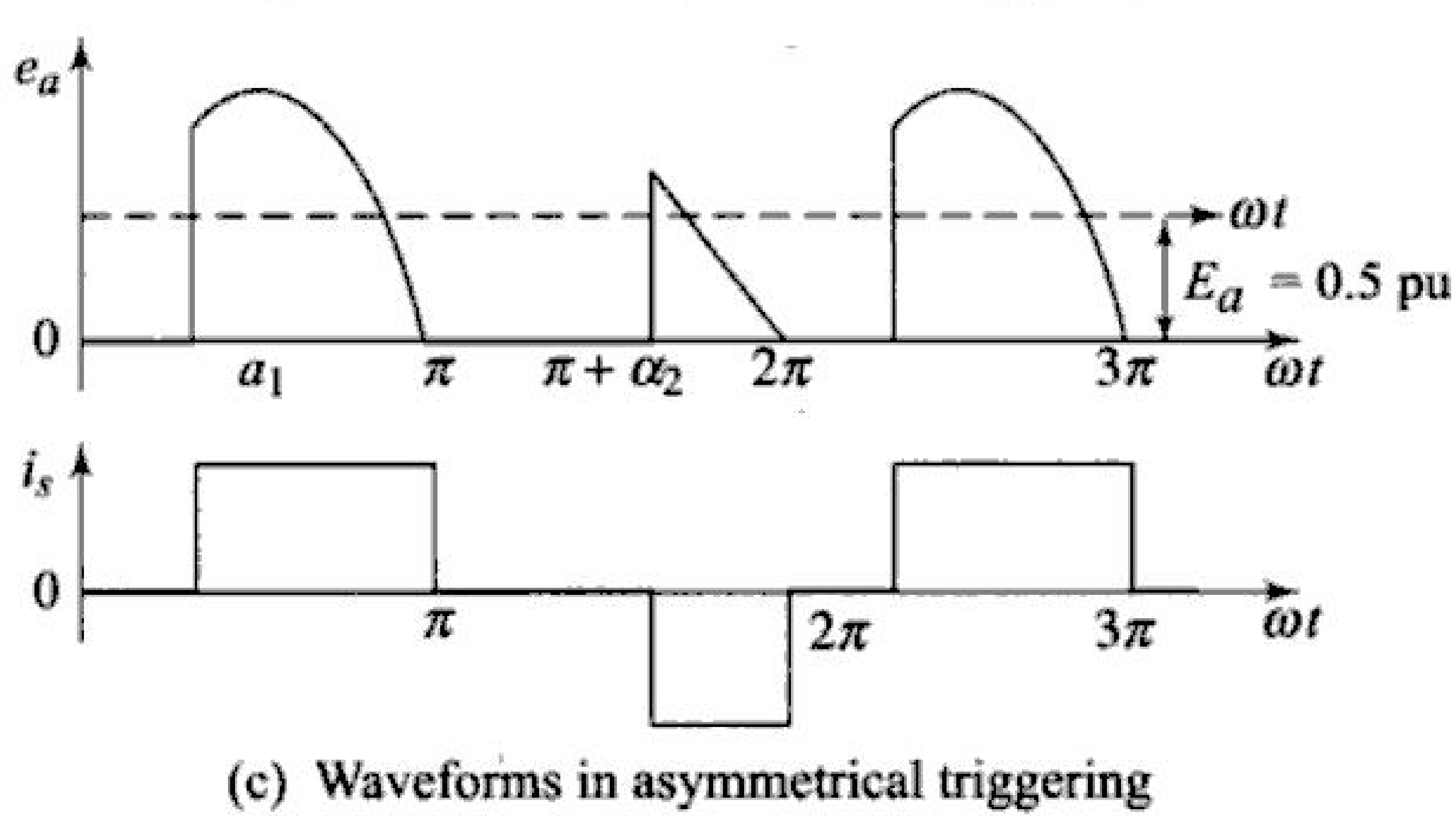


(a) Semiconverter circuit

Fig. 6.57 ***(a)***



(b) Waveforms in symmetrical triggering



(c) Waveforms in asymmetrical triggering

Fig. 6.57 ***(b)*** *and* ***(c)*** *Symmetrical and asymmetrical triggering* circuit, asymmetrical firing makes the motor current very peaky and discontinuous. The disadvantages outweigh the advantages of minor improvement in power factor and therefore, asymmetrical firing is only of theoretical interest.

6.17.4 Extinction Angle Control (EAC)

Figure 6.58 shows the single-phase semiconverter, where thyristors T_1 and T_2 are replaced by switches S_1 and S_2. The switching actions of S_1 and S_2 can be either performed by SCRs or by GTOs. A dotted square of Fig. 6.58 represents an SCR(GTO) and its commutation circuitry. For the sake of simplicity, commutation circuits are not shown. Figure 6.59 shows the waveforms for the extinction angle control scheme.

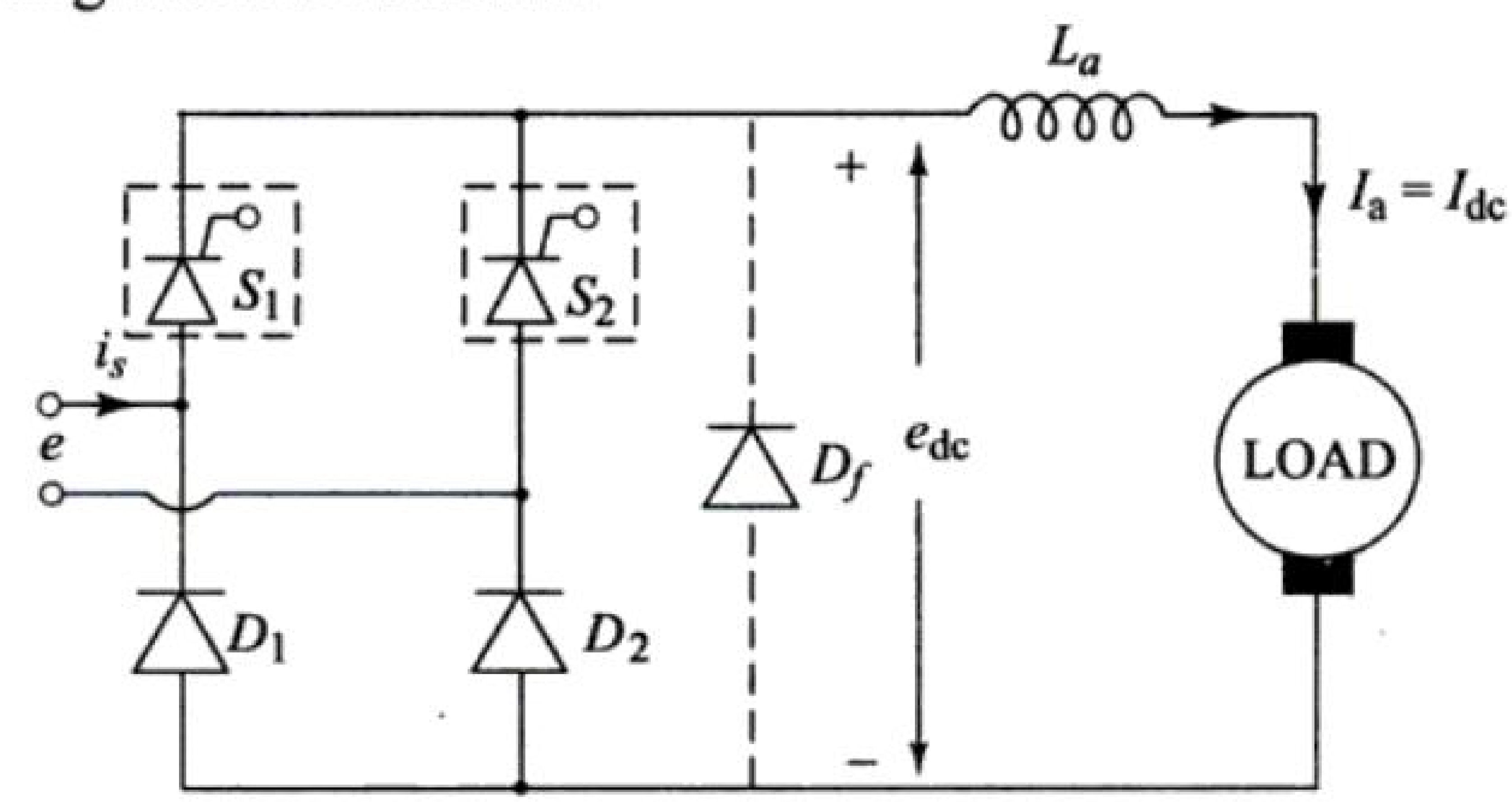


Fig. 6.58 *Power circuit employing forced commutation*

In this scheme, as shown in Fig. 6.59, switch S_1 is turned ON at $\omega t = 0$ and turned OFF by forced commutation at $\omega t = \beta$. Switch S_2 is turned ON at $\omega t = \pi$ and is turned OFF at $\omega t = (\pi + \beta)$. The output voltage is controlled by varying the extinction angle, β. The fundamental component i_1 of the supply current i_s,

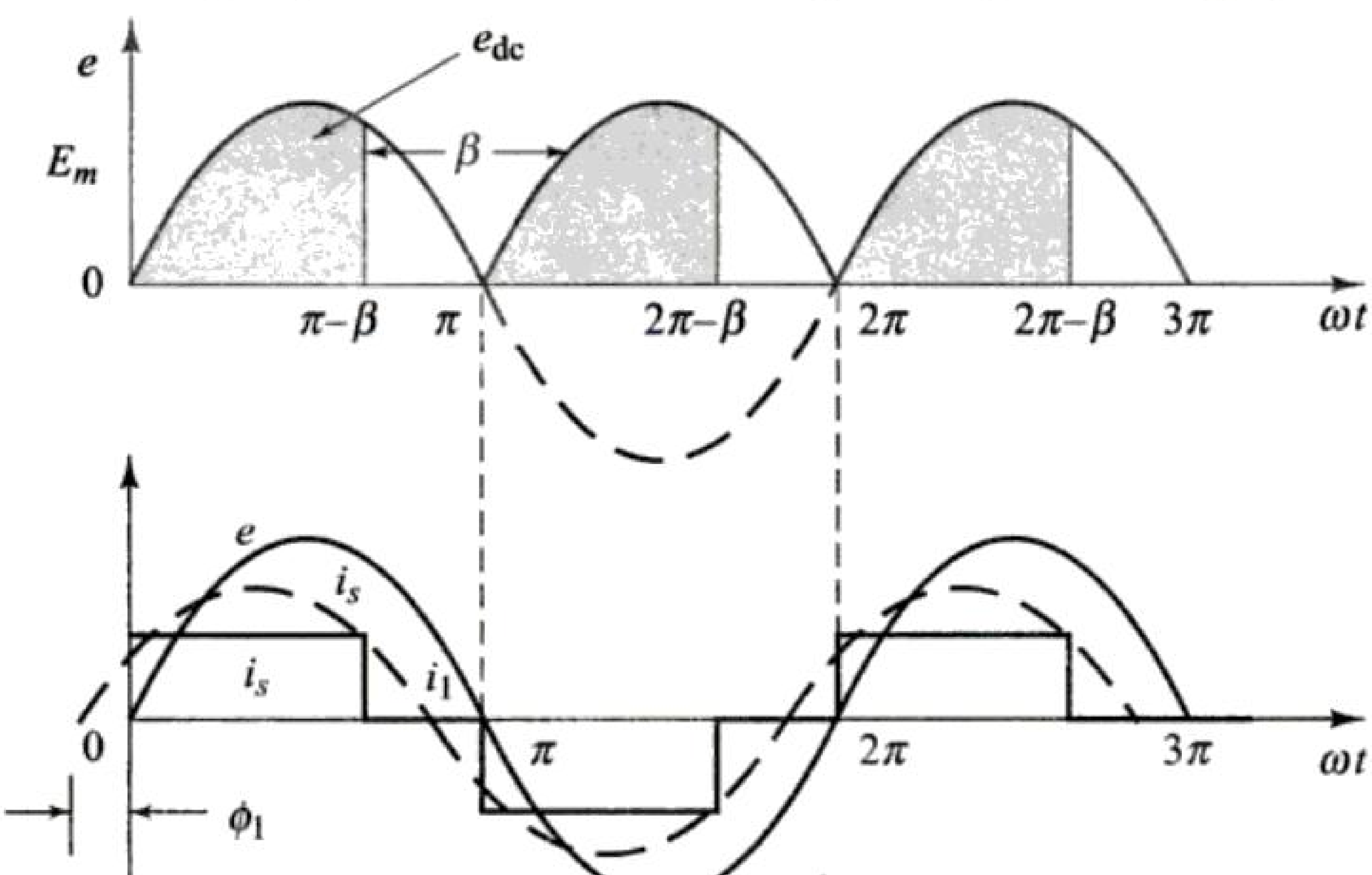


Fig. 6.59 *Extinction angle control scheme waveforms*

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6.39 Derive the expressions for average output voltage, RMS supply current, RMS *n*th harmonic current, displacement angle, supply power factor, displacement factor, and harmonic factor in case of symmetrical angle control scheme.

6.40 Explain in detail the sinusoidal pulse-width modulation control scheme for power factor improvement.

6.41 Derive the expressions for average output voltage, RMS supply current, RMS *n*th harmonic current, displacement angle, supply power factor, displacement factor, harmonic factor, in sinusoidal pulse-width modulation control scheme for improvement of power factor.

PROBLEMS

6.1 A single-phase half-wave rectifier is used to supply power to a load of impedance 10 Ω from 230 V, 50 Hz a.c. supply at the firing angle of 30°. Calculate
(a) Average load voltage.
(b) Effective value.
(c) Load current.

[*Ans* (a) 96.35 V, (b) 159.8 V, (c) 9.636 A]

6.2 A voltage source $e = 100 \sin 377t$, supplies a resistive load of 100 Ω through a thyristor, which performs half-wave controlled rectification. Calculate, the average power in the load, if the firing angle is fired at 45° with respect to the supply voltage waveform.

[*Ans*. 22.7 W]

6.3 A highly inductive load, such that load current can be assumed constant, is to be supplied from a 230 V, 50 Hz, single-phase supply by a fully-controlled and a half-controlled bridges. Compare the average load. Voltage provided by each bridge at firing angles of 30° and 90°. Neglect device voltage drops.

[*Ans*. (i) Fully controlled bridge–
E_{dc}, 30° = 179.33 V, E_{dc}, 90° = 0
(ii) Half-controlled bridge–
E_{dc} 30° = 193.199 V, E_{dc} 90° = 103.54 V]

6.4 A single-phase 230 V, 1 kW heater is connected across a single-phase, 230 V, 50 Hz supply through an SCR. For firing angle of 45° and 90°, calculate the power absorbed by the heater-element.

[*Ans*. (i) α = 45°, power = 454.57 W
(ii) α = 90°, power = 250 W]

6.5 Calculate the average output voltage of a three-phase half-controlled bridge operating with a triggering angle of $\pi/2$ and connected to three-phase a.c. supply of 400 V and 50 Hz. The load current i_d is assumed to be continuous.

[*Ans*. E_{dc} = 270 V]

6.6 A single-phase fully-controlled bridge is connected to an a.c. supply of 230 V and 50 Hz is used for the speed control of d.c. motor with separate field excitation. The full-load average armature current is 10 A and the converter operates at a firing angle $\alpha = \pi/4$. Neglecting the inductance and resistance of both armature and source, calculate the minimum value of series inductance, L_d, required in the armature circuit to provide for continuous current conduction.

[*Ans*. L_d = 46.5 mH]

6.7 A fully-controlled three-phase bridge converter is working in the inversion mode with a firing advance angle of 25°. If the a.c. supply is 220 V with a reactance of 0.1 Ω/phase, determine the maximum current that can be commutated, allowing a recovery angle of 5°. Neglect device voltage drops.

[*Ans.* I_d = 140 A]

6.8 A six-pulse thyristor converter, connected to 230 V, 50 Hz, 3–ϕ a.c. supply. If the reactance on a.c. side is 0.1502 and the commutation angle is 15°, calculate the d.c. load current.

[*Ans.* I_d = 90.47 A]

6.9 Calculate d.c. output voltage from a six-pulse double-star circuit connected to an a.c. supply of 415 V, three-phase, 50 Hz at a firing angle of 30°.

[*Ans.* E_{dc} = 161.38V]

6.10 A three-phase, half-wave converter is supplying a load with a continuous constant current of 40 A over a firing angle from 0 to 75°. What will be the power dissipated by the load at these limiting values of firing angle? The supply voltage is 415 V (line).

[*Ans.* for α = 0°, Power = 11.2 kW
α = 75°, Power = 2.9 kW]

6.11 A single-phase, half-controlled bridge is constructed as shown in Fig. P. 6.11. Sketch the load voltage waveform for an R–L load at a firing angle of 30°.

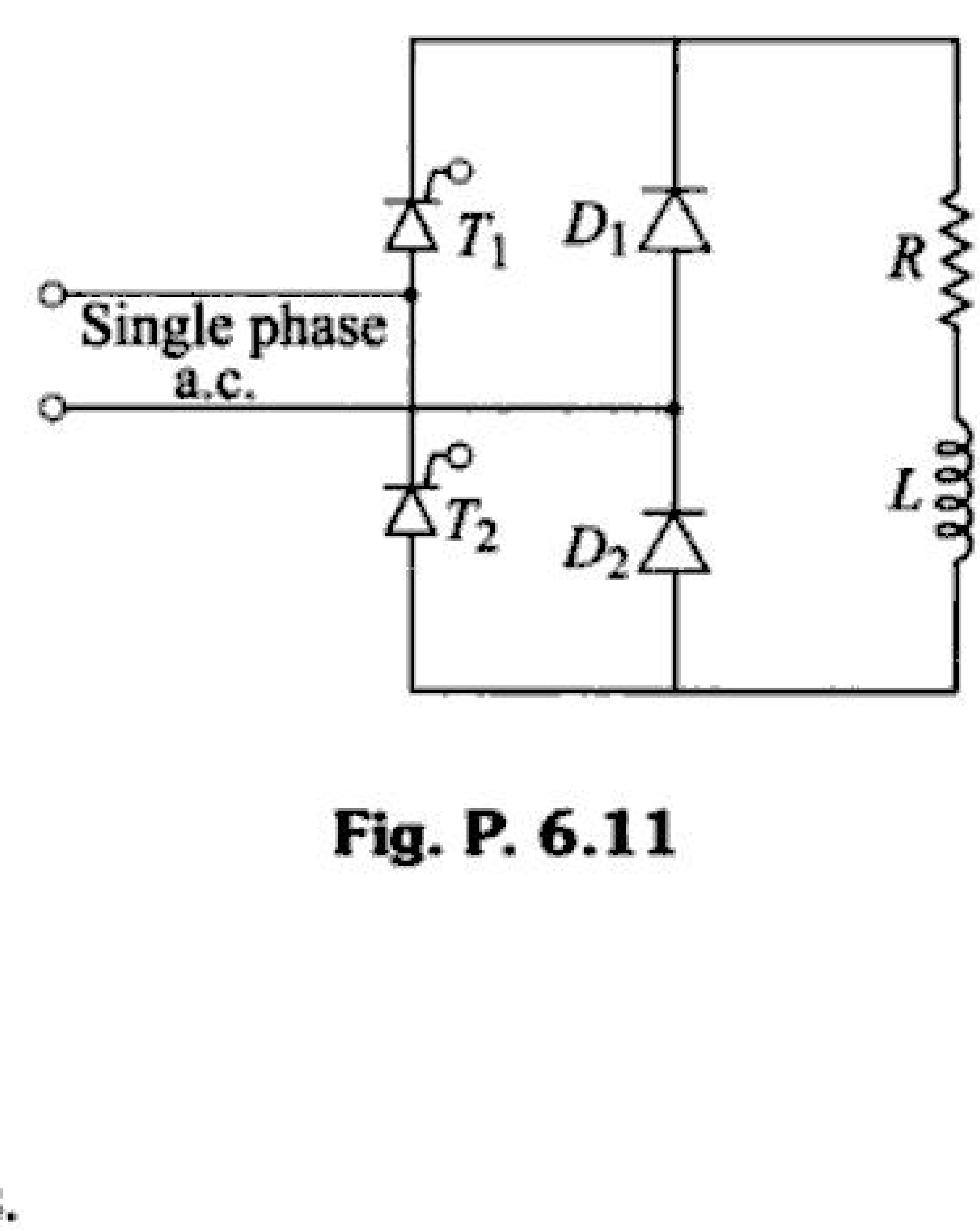

Fig. P. 6.11

6.12 A three-phase, fully-controlled bridge converter is supplying a d.c. load of 400 V, 60 A from a three-phase, 50 Hz, 660 V (line) supply. If the thyristors have a voltage drop of 1.2 V when conducting then, neglecting overlap, compute

(i) the firing angle of thyristor.
(ii) RMS current in thyristors.
(iii) the mean power loss in thyristors.
(iv) If the a.c. supply has an inductance per phase of 3.6 mH, what will be the new value of firing angle required to meet the load requirements?

[*Ans.* (i) α = 63.10°, (ii) I_{rms} = 34.64 A, (iii) Power = 24 W, (iv) α = 58.23°]

6.13 (a) A three-phase, fully-controlled bridge converter is connected to a three-phase, 50 Hz, 415 V (line) supply and is operating in the inverting mode at a firing advance angle of 30°. If the a.c. supply has a resistance and inductance per-phase of 0.09 Ω and 1 mH, respectively. Find

(i) d.c. source voltage.
(ii) overlap angle.
(iii) recovery angle, when the d.c. current is constant at 52 A.

Thyristors have a forward voltage drop when conducting of 1.8 V.

(b) In case (a), what will be the maximum d.c. current that can be accommodated at a firing advance angle of 22.5°, allowing for a recovery angle of 5° ?

[*Ans.* (a) (i) 506.6 V; (ii) μ = 8.17°; (iii) γ = 21.43°, (b) I_d = 67.53A]

6.14 A three-phase fully-controlled converter is employed to change a battery with an emf of 95 V and an interval resistance of 0.1 Ω. The supply RMS voltage is 110 V line-to-line and sufficient inductance is induced in the output-circuit to maintain the current virtually constant at 20 A.

Determine

(i) the firing angle α, (ii) power factor of supply.

[*Ans.* (i) α = 49.22°, (ii) p.f. = 0.62]

6.15 A three-phase fully-controlled bridge converter operates in both rectification and inversion mode. The leakage inductance of each phase of input transformer winding is 0.002 H. The three-phase input voltage is balanced and sinusoidal, and has an RMS magnitude of 230 V per phase and frequency 50 Hz. The load current of d.c. side is 15 A.

(a) Calculate the drop in the d.c. output voltage caused by the internal reactance drop.

(b) When the bridge is working in rectification mode and the d.c. output voltage is 200 V, then compute

(i) firing angle α

(ii) overlap angle for the phase currents.

(c) When the bridge is to be functioning as an inverter with a load current 15 A and d.c. output voltage and 200 V then calculate the recovery angle or margin angle.

[*Ans.* (a) 9 V, (b) (i) = 67°, (ii) = 2.48°, (c) 67°]

6.16 (a) A single-phase semiconverter delivers power to *RLE* load with R = 5 Ω, L = 10 mH and E = 80 V. The a.c. supply voltage is 230 V, 50 Hz. For the continuous conduction, find the average value of output-current for a firing angle of 50°. (b) If one of the two main SCRs is damaged and open-circuited, find the new value of average output current on the assumption of continuous conduction. Draw the output voltage waveforms and indicate the conducting periods of devices.

[*Ans.* (a) 18.013 A; (b) 1 A]

6.17 A three-phase fully-controlled thyristor bridge converter supplies a d.c. voltage source of 400 V having an interval resistance of 1.8 Ω. Assume highly inductive load with a content load current of 20 A. The supply RMS load voltage per phase is 230 V and source inductance in each phase is 0.005 H. Compute the following by ignoring the source resistance:

(i) Firing angle α for an output voltage of 436 V

(ii) Overlap angle.

[*Ans.* (i) 30°; (ii) 11°]

6.18 A single phase fully controlled bridge rectifier is given 230 V, 50 Hz supply. The firing angle is 45° and the load is highly inductive. Determine:

(i) Average output voltage (iii) Power factor

(ii) Voltage ripple factor (iv) Form factor

Ans. [(i) 146.42 V, (ii) 1.21, (iii) 0.637 (lagging), (iv) 1.57]

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The comparator outputs e_{d_1} and e_{d_2} are used as the inputs for the AND gates A_1 and A_2, respectively. The second input for both AND gates is the pulses generated by the pulse-generator. E_C is the control voltage. The output e_{d_1} and e_{d_2} allow the firings pulses to be applied to the converters. Both converters receive the firing pulses when the load current is below the threshold value and hence, circulating current flows through the dual converter. Otherwise, only one converter, receives the firing pulses, and the dual converter operates in the noncirculating current mode. Figure 7.15 illustrates the associated waveforms. The circulating current in this control scheme flows only when the load current is small. Thus, the size of the reactor is small. When only one converter conducts, the core of the reactor can saturate at high load currents and the reactor does not have to perform the circulating current limiting function.

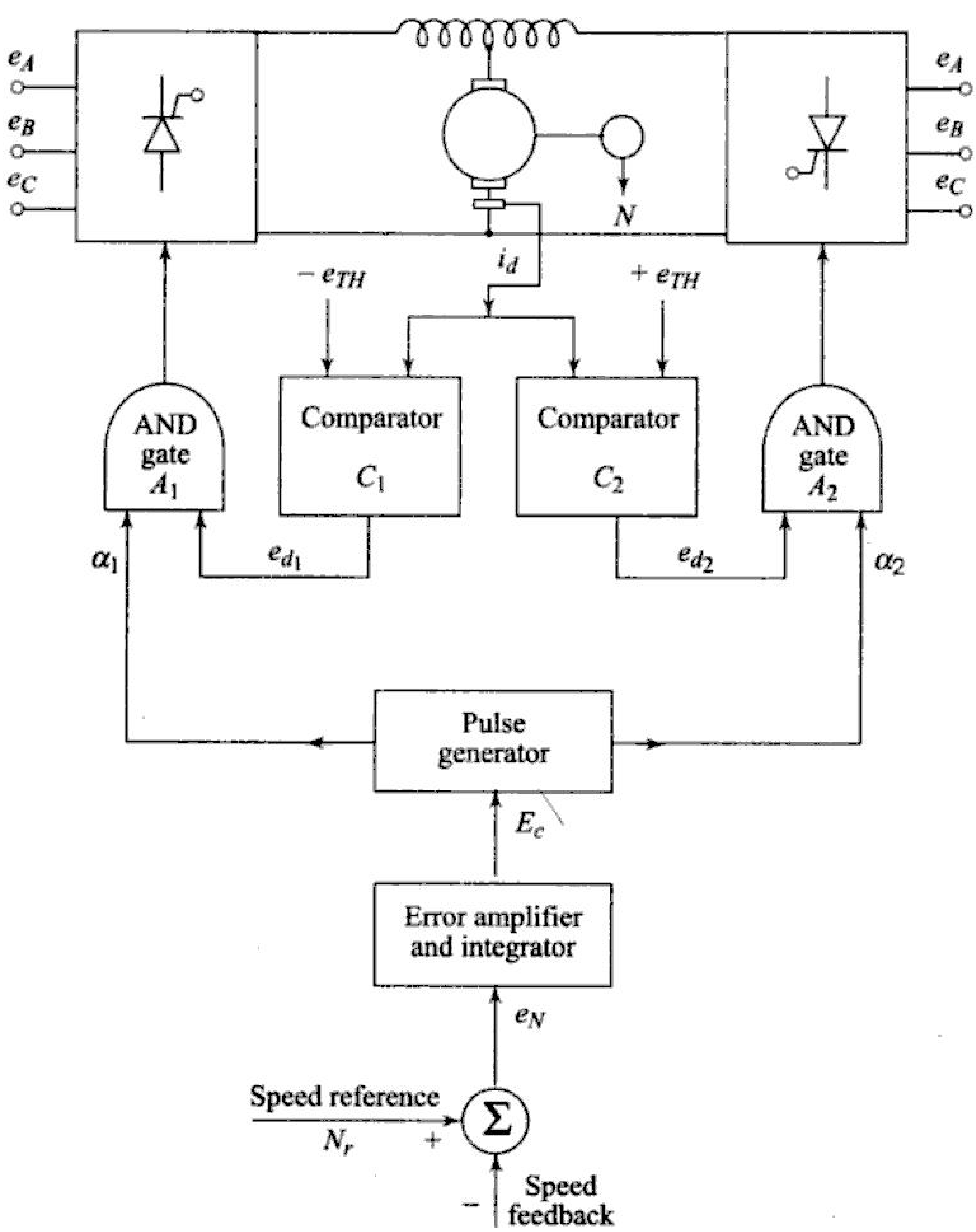

Fig. 7.14 *Basic block diagram*

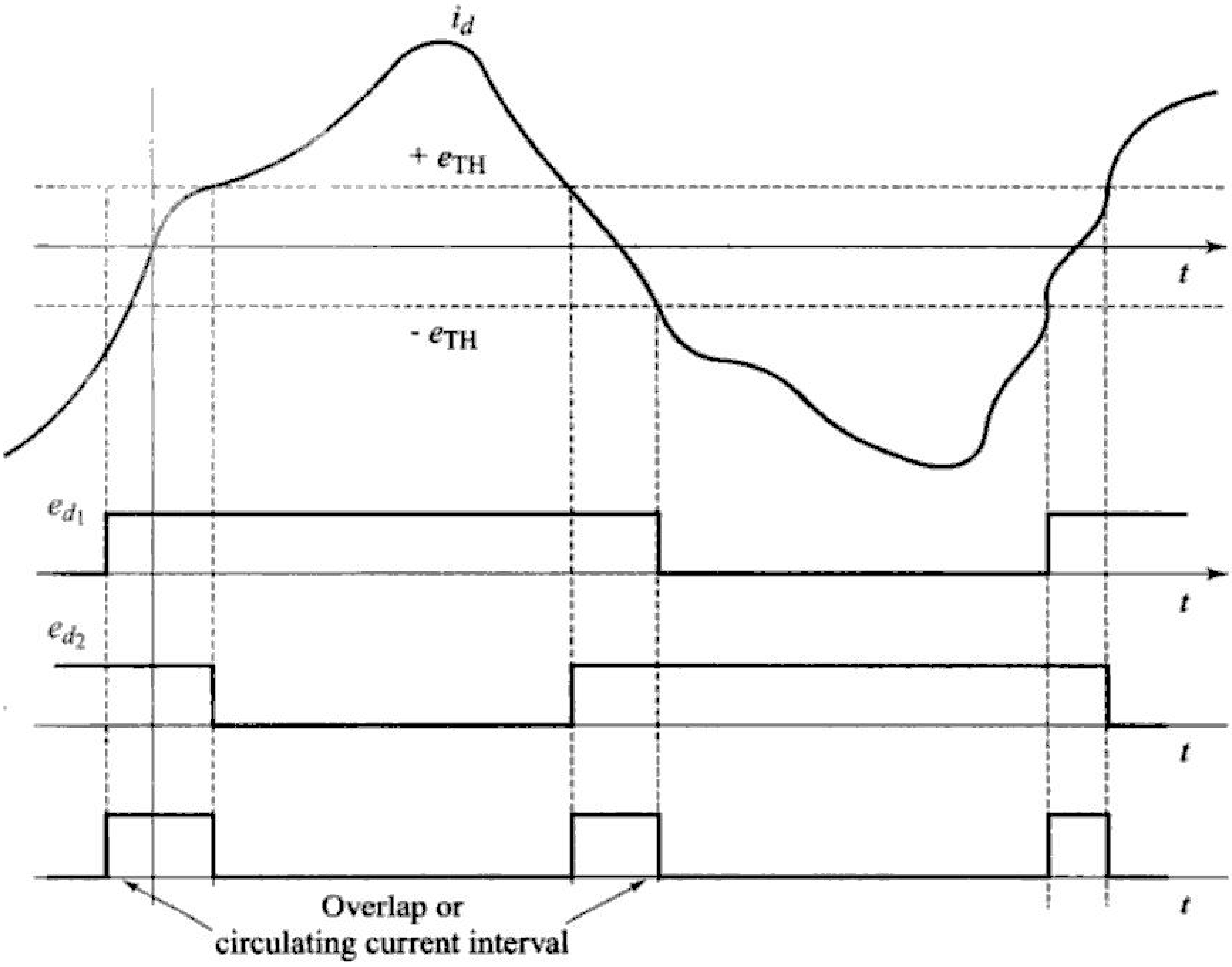

Fig. 7.15 *Associated waveforms*

7.7 COMPARISON BETWEEN NON-CIRCULATING CURRENT MODE AND CIRCULATING CURRENT MODE

The comparison between non-circulating current mode and circulating-current mode of dual-converters is given below:

Non-circulating current mode	*Circulating current mode*
1. In this mode of operation, only one converter operates at a time and the second converter remains in a blocking state.	In this mode of operation, one converter operates as a rectifier and the other converter operates as an inverter.
2. Converters may operate in discontinuous current mode.	Converters operates in continuous current mode.
3. Reactors may be needed to make load-current continuous.	Reactors are needed to limit circulating current. These reactors are costly.
4. Since no circulating current flows through the converters, efficiency is higher.	Circulating current flows through the converters and hence increases the losses.
5. Due to discontinuous current, non-linear transfer characteristics are obtained.	Due to continuous current, linear transfer characteristics are obtained.

(*Contd.*)

	Non-circulating current mode	Circulating current mode
6.	Due to discontinuous current, response is sluggish.	Due to continuous-current in the converters, response is fast.
7.	Due to spurious firing, faults between converters results in dead short-circuit conditions.	Due to spurious firing, fault currents between converters are restricted by the reactor.
8.	In this mode of operation, the cross-over technique is complex.	In this mode of operation, the crossover technique is simple.
9.	Loss of control for 10 to 20 ms is observed in this mode of operation.	Since converters do not have to pass through blocking unlocking and safety intervals of 10 to 20 ms, hence control is never lost in this mode of operation.
10.	The control scheme needs command module to sense the change in polarity.	As both the converters are operating at the same time, the control scheme does not require command module.
11.	The complete scheme is cheaper compared to circulating current mode.	The complete scheme is expensive.
12.	In this mode of operation, the converter loading is the same as the output load.	In this mode of operation the converter loading is higher than the output load.

7.8 MICROPROCESSOR BASED-FIRING SCHEME FOR A DUAL CONVERTER

Figure 7.16 illustrates a scheme of firing control of a dual converter using a microprocessor. This scheme consists of the following:

(a) Thyristor power converter In this case, a dual converter used for four-quadrant operation of the d.c. motor. There are two converter groups, one positive group and the other negative group. When two thyristors of a particular group conduct simultaneously, then the load current flows.

(b) Power signal operation From the three-phase voltages, digitised signals are obtained. An isolation is provided by means of the filament single-phase transformers. The output of the transformers is amplified. The amplified signals are saturated to obtain the digitized signals. These signals are used to obtain the base interrupt.

(c) Frequency doubler stage In this stage, a base interrupt signal is obtained and this signal frequency is double to that of the supply. This is obtained by combining the two sets of pulse signals obtained at the rising and falling edges of the above digitized signals. The interrupt signals is available at each 60° interval so that six firing pulses are available for firing the converter. At the falling edge of the interrupt, signal starts a new firing cycle.

(d) Firing angle control A microprocessor is used for the firing angle control of the dual converter. To perform the functions of firing range selection, firing pulse generation, cross over protection, etc. the microprocessor can be

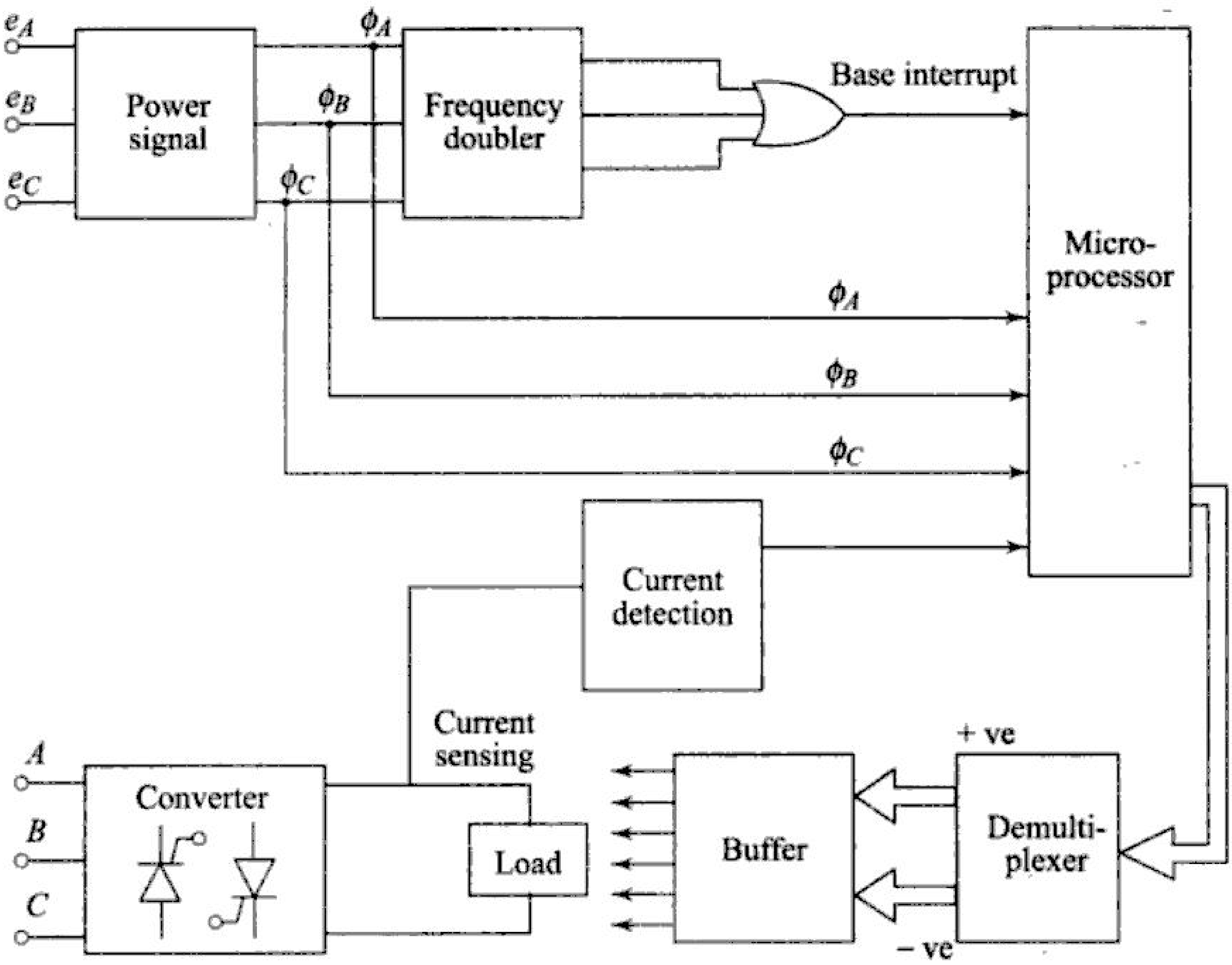

Fig. 7.16 *Block diagram for firing scheme of a dual converter using microprocessor*

programmed using a suitable software. The thyristor of the converter in conduction should receive the firing pulses for either modes of continuous and discontinuous operation. Two thyristors should receive the pulses at anytime. The firing signal contains several pulses. The firing pulses so obtained turn the thyristor ON reliably. A proper software facilitates the implementation of the firing pulses with minimum hardware. A second requirement is firing angle control. This can be achieved by storing the angle command in two registers of the processor. To indicate the firing pulses for the positive group of thyristors or negative group of thyristors, information should also be available. This information can be made available again from the digitized power signals and also power source voltages. A logic can be developed to define the firing angle range and also the firing pulses to a given converter. Using proper look-up tables, the firing angle selection can be suitably implemented. The following steps are involved:

(i) Read in the digitized signals.
(ii) The range indicater and a look-up table provide the firing-code.
(iii) After checking the protections, the gates of the thyristors are triggered.
(iv) At the end of firing process, the microprocessor will take care of interrupted program. The microprocessor can be programmed to do the other jobs of servo-system.

(e) Current detection selection Another feature requiring detection is the current detection. It becomes more meaningful to detect the direction of load-current rather than the detection of thyristor currents. Positive group of thyristors conduct if the current is in the positive direction. However, they may be conducting if the current direction is not positive. This is due to the turn-off characteristics of the SCRs. Therefore, it is necessary to device special methods to make sure that no SCR is conducting when the current direction signals are zero. This is necessary to avoid the firing of the thyristors in the other converter.

One of the protection features to be implemented using a microprocessor is failure of any phase. This can be implemented using digitized power signals, cross-over conditions, etc. The multi-level protection is possible and this increases the reliability.

Figure 7.17 illustrates the block-diagram for microprocessor based speed control of a d.c. motor using a dual converter.

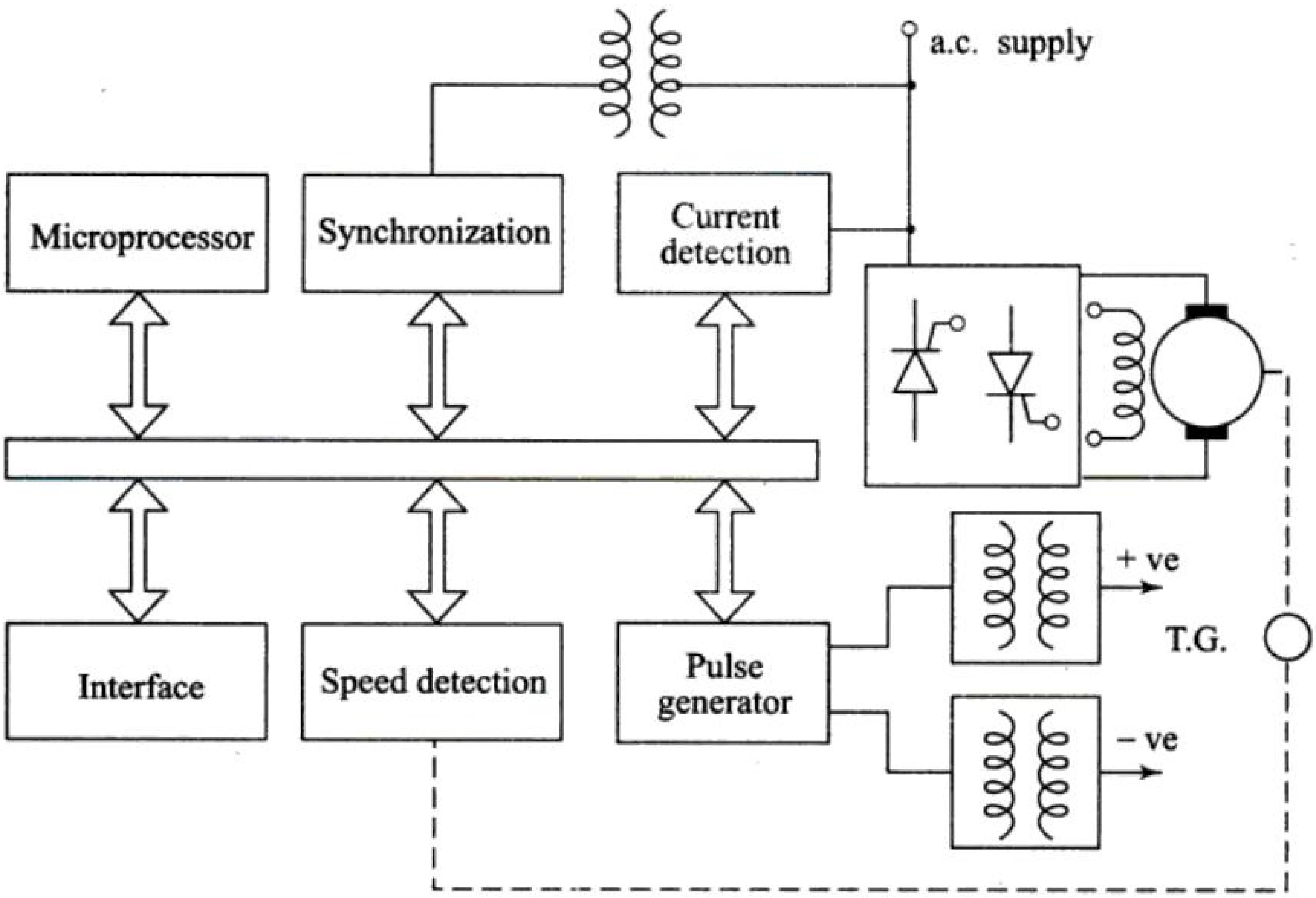

Fig. 7.17 *Basic block diagram*

SOLVED EXAMPLES

Example 7.1 Compute the peak value of the circulating current for the 3-ϕ circulatory current type dual converter consisting of two three-phase fully controlled bridges for the given data.

Per phase supply RMS voltage = 230 V, ω = 315 rad/s, L = 12 mH

$$\alpha_1 = 60°, \alpha_2 = 120°.$$

Solution: The peak value of the circulating current from Eq. (7.18) is given by

$$i_{cp} = \frac{3\sqrt{2}E_{rms}}{\omega L}(1 - \cos \pi/6), = \frac{3\sqrt{2} \times 230}{315 \times 12 \times 10^{-3}}(1 - \cos \pi/6) = 34.58 \text{ A}.$$

Example 7.2 Design a dual converter to achieve a four-quadrant operation of the separately excited d.c. motor. Motor and converter specifications are given by

(i) Motor specifications

$E_a = 220$ V, $I_a = 30$ A, $N = 1500$ rpm.

(ii) Converter specifications

Supplied from 3-ϕ, 400 V, 50 Hz supply

Assume drop in the circuit is 15%.

Solution: Consider that dual converter consist of six-pulse converters to achieve a four-quadrant operation.

(i) Step 1 Rectifier operation:

Total drop in the system = $220 \times 0.15 = 33$ V.

$\therefore$ Total d.c. voltage, $E_{dc\alpha} = E_{dc}$ + drop, $= 220 + 33 = 253$ V.

For six-pulse bridge converter, we have the relation

$$E_{dc\ \alpha} = 1.35\ E_{ac} \cos \alpha_1.$$

where E_{ac} = RMS value of a.c. voltage.

$\therefore$ $253 = 1.35 \times 400 \times \cos \alpha_1 \quad \therefore \cos \alpha_1 = 0.469 \quad \therefore \alpha_1 = 62°.$

A.C. line current $I_{ac} = 0.817.\, I_{dc} = 0.817 \times 30 = 24.51$ A.

A.C. terminal power, $P_{ac} = \sqrt{3} \times E_{ac} \times I_{ac} = \sqrt{3} \times 400 \times 24.51 = 16.98$ kW.

$$P_{ac} = 1.05\, P_{dc}, \quad \therefore P_{dc} = \frac{P_{ac}}{1.05} = \frac{16.98 \times 10^3}{1.05} = 16.17 \text{ kW}.$$

(ii) Step 2

Current limiting inductance L_C is given by, $L_C = \dfrac{2 \times 1.35 \times E_{ac}}{6\omega I_{\text{ripple}}} \left[\dfrac{1}{7} + \dfrac{1}{5}\right]$

where $I_{\text{ripple}} = \dfrac{I_d}{5}$ for six-pulse converter $= \dfrac{30}{5} = 6$ A.

$$\therefore \quad L_c = \frac{2 \times 1.35 \times 400}{6 \times 2\pi \times 50 \times 6} = 33 \text{ mH}$$

(iii) Step 3

Firing angle $\alpha_2° = 180° - \alpha_1 = 180° - 62 = 118°$

(iv) Selection of SCR

(a) Voltage rating, PIV = $2\sqrt{2}\, E_{ac} = 2\sqrt{2} \times 400 = 1131.37$ PIV = 1200 V.

(b) Current rating

$$I_T = 2\sqrt{2} \times I_{ac} = 2\sqrt{2} \times 24.51 = 69.32 \text{ A} \cong 70 \text{ A}.$$

REVIEW QUESTIONS

7.1 Explain with a neat circuit diagram the basic principle of a dual converter.

7.2 Compare the ideal dual converter mode with non-ideal dual converter mode.

7.3 Describe in detail the operation of dual converter without circulating current.

7.4 With the help of basic block diagram, explain how converter selection is achieved by control signal polarity.

7.5 With the help of suitable control scheme, explain how converter selection in achieved by load current polarity.

7.6 Explain by giving basic block diagram, the converter selection by both control voltage and load current approach.

7.7 Discuss the advantages and disadvantage of the converter selection method of both control voltage and load current.

7.8 Explain in detail the operation of dual converter with circulating current. List the advantages and disadvantages of the same scheme.

7.9 Draw the basic block diagram of a dual converter operating in circulating current mode and describe the operation with associated waveforms.

7.10 Derive the expression for peak value of the circulating current.

7.11 By giving the basic block diagram, explain the operation of a dual mode dual converter in detail.

7.12 Give the comparison between non-circulating current mode and circulating current mode.

7.13 Draw and explain in detail the microprocessor based firing scheme for a dual converter.

PROBLEMS

7.1 Calculate the peak value of the circulating current for the 3-ϕ circulatory current type dual converter consisting of two three-phase fully controlled bridges for the given data.
Per phase supply RMS voltage = 230 V, f = 15 Hz, L = 15 mH, α_1 = 60°, α_2 = 120° [*Ans* ic_p = 27.74 A.]

7.2 Two three-phase full-converters are connected in antiparallel to form a three phase dual converter of the circulating current type. The input to the dual-converter is 3-ϕ, 400 V, 50 Hz. If the peak value of the circulating current is to be limited to 20 A, find the value of inductance needed for the reactor for firing angle of 60°. [*Ans* L_C = 20.89 mH.]

7.3 Design a dual converter to achieve at four-quadrant operation for I_d = 10 A at 200 V. The converter is supplied from 400 V, 3-ϕ and 50 Hz supply.
I_{ripple} = 2 A.
[*Ans* (i) α_1 = 68°, α_2 = 112° (ii) $L_c = I_{ac}$ = 8.17, P_{ac} = 5.66 kW, P_{dc} = 5.39 kW.
(iii) L_c = 98 mH (iv) PIV = 1200 V, I_T = 22 Amp]

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Chapter 8

Choppers

LEARNING OBJECTIVES:

- To describe the need and function of a chopper.
- To consider the operation of a d.c. chopper.
- To explain the different chopper control techniques.
- To examine the operation of step-up and step-down choppers.
- To classify the d.c. choppers in terms of their operating envelopes.
- To consider the operation of buck, boost, buck-boost and cuk-switching regulators.
- To explain the working principle and circuit analysis of Type A chopper.
- To explain the working principles of Type B, Type C, Type D and Type E chopper circuits.
- To consider the operation of various chopper commutation circuits.
- To examine the operation of Jones and Morgan chopper circuits.
- To explain the working principles of an a.c. chopper and a multiphase chopper.
- To consider the operation of buck, boost, buck-boost and cuk-switching regulators.

8.1 INTRODUCTION

To produce quality goods in any industry, the processes necessarily require the use of variable speed drives. Variable speed d.c. and a.c. drives are being increasingly used in all industries. These drives and processes take power from d.c. voltage sources. In many cases, conversion of the d.c. source voltage to different levels is required. For example, subway cars, trolley buses, or battery operated vehicles require power from a fixed voltage d.c. source. However, their speed control requires conversion of fixed voltage d.c. source to a variable-voltage d.c. source for the armature of the d.c. motor.

Generally, following techniques are available for obtaining the variable d.c. voltage from a fixed d.c. voltage:

(1) Line Commutated Converters (Conversion of AC supply to variable DC supply using controlled rectifiers; covered in Chapter 6).

(2) AC Link Chopper (inverter-rectifier) In this method the d.c. is first converted to a.c, by an inverter (d.c. to a.c. converter). The obtained a.c. is then stepped up or down by a transformer and then rectified back to d.c. by a rectifier. As the conversion is in two stages, d.c. to a.c. and a.c. to d.c., this technique is therefore, costly, bulky and less efficient. However, the transformer provides isolation between load and source. Figure 8.1 illustrates the conversion processes.

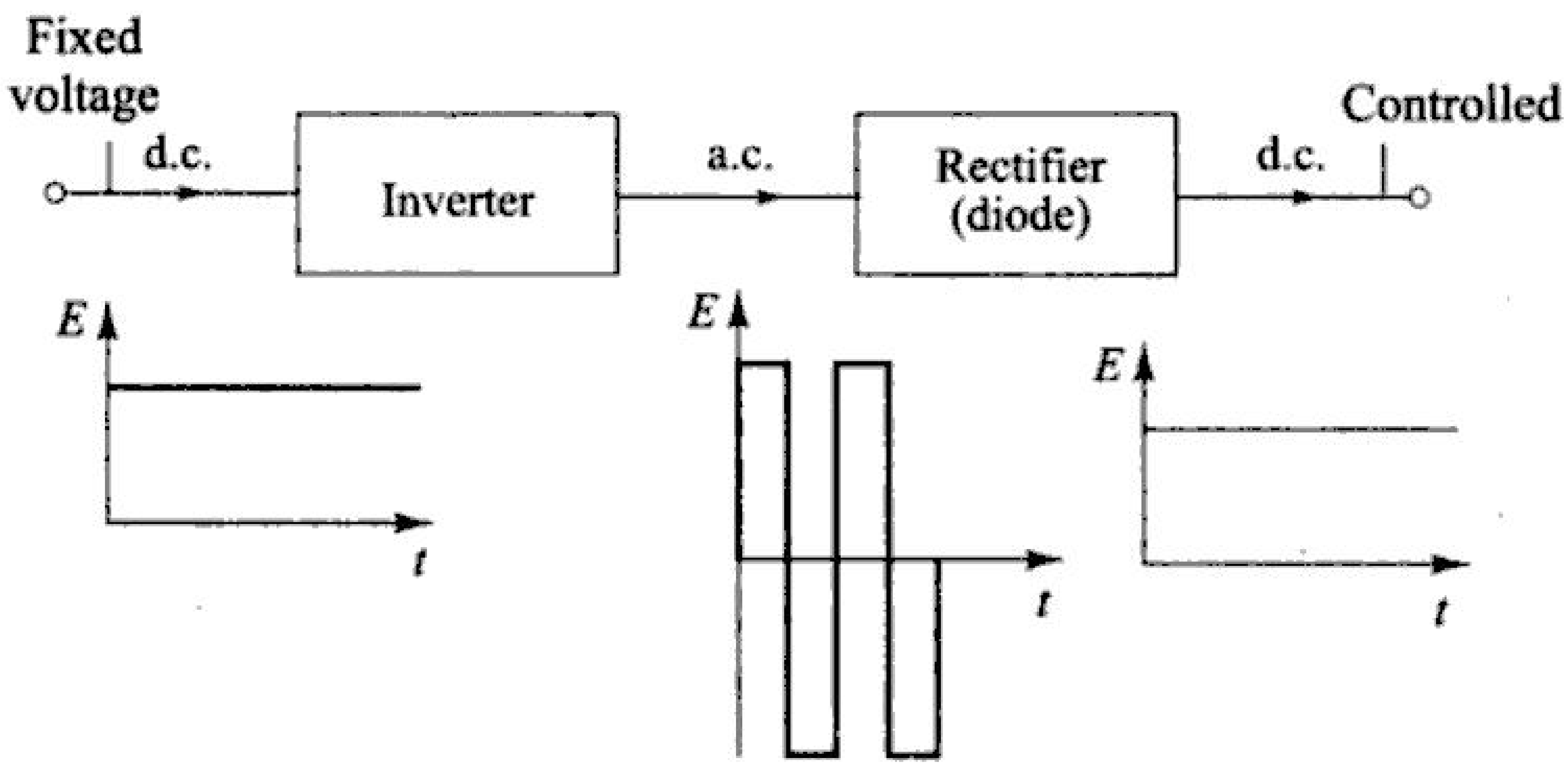

Fig. 8.1 *a.c.-link-chopper*

(3) DC Chopper (d.c. to d.c. power converters) A d.c. chopper is a static device (switch) used to obtain variable d.c. voltage from a source of constant d.c. voltage, Fig. 8.2. Therefore, chopper may be thought of as d.c. equivalent of an a.c. transformer since they behave in an identical manner. Besides, the saving in power, the d.c. chopper offers greater efficiency, faster response, lower maintenance, small size, smooth control, and, for many applications, lower cost, than motor-generator sets or gas tubes approaches.

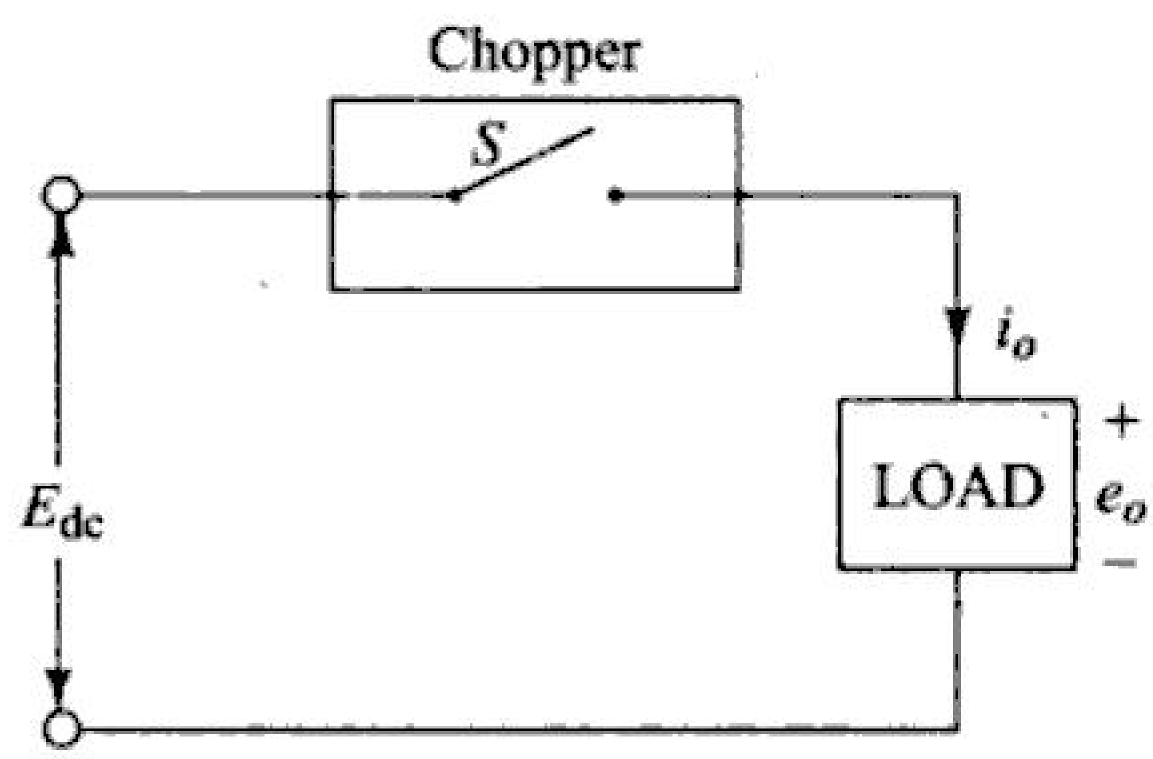

Fig. 8.2 *Basic chopper configuration*

Solid-state choppers due to various advantages are widely used in trolley cars, battery-operated vehicles, traction-motor control, control of a large number of d.c. motors from a common d.c. bus with a considerable improvement of power factor, control of induction motors, marine hoists, forklift trucks and mine haulers. The objective of this chapter is to discuss the basic principles of chopper operation and more common types of chopper configuration circuits.

8.2 BASIC CHOPPER CLASSIFICATION

DC choppers can be classified as:

(A) According to the Input/Output Voltage Levels

(i) ***Step-down chopper:*** The output voltage is less than the input voltage.

(ii) ***Step-up chopper:*** The output voltage is greater than the input voltage.

(B) According to the Directions of Output Voltage and Current

(i) Class A (type A) chopper
(ii) Class B (type B) chopper
(iii) Class C (type C) chopper
(iv) Class D (type D) chopper
(v) Class E (type E) chopper

The voltage and current directions for above classes are shown in Fig. 8.3.

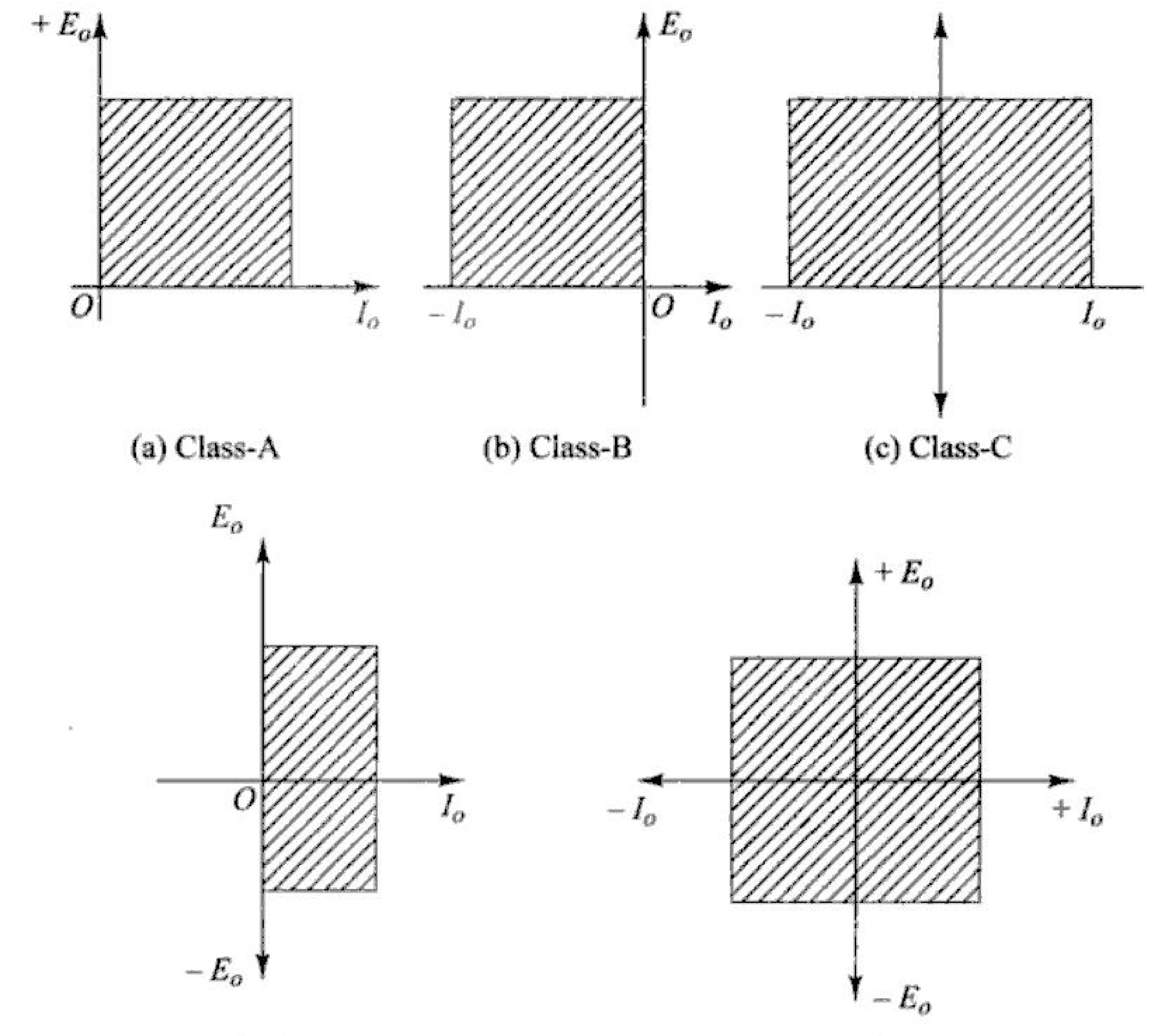

Fig. 8.3 *Chopper configurations*

(C) According to Circuit Operation

(i) *First-quadrant chopper:* The output voltage and both must be positive. (Type A).

(ii) *Two-quadrant chopper:* The output voltage is positive and current can be positive or negative (class-C) or the output current is positive and the voltage can be positive or negative (class-D).
(iii) *Four-quadrant chopper:* The output voltage and current both can be positive or negative (class-E).

(D) According to Commutation Method

(i) Voltage-commutated choppers
(ii) Current-commutated choppers
(iii) Load-commutated choppers
(iv) Impulse-commutated choppers

8.3 BASIC CHOPPER OPERATION

8.3.1 Principle of Step-Down Chopper (Buck-Converter)

In general, d.c. chopper consists of power semiconductor devices (SCR, BJT, power MOSFET, IGBT, GTO, MCT, etc., which works as a switch), input d.c. power supply, elements (R, L, C, etc.) and output load. (Fig. 8.4). The average output voltage across the load is controlled by varying on-period and off-period (or duty cycle) of the switch.

A commutation circuitry is required for SCR based chopper circuit. Therefore, in general, gate-commutation devices based choppers have replaced the SCR-based choppers. However, for high voltage and high-current applications, SCR based choppers are used. The variations in on- and off periods of the switch provides an output voltage with an adjustable average value. The power-diode (D_P) operates in freewheeling mode to provide a path to load-current when switch (S) is OFF. The smoothing inductor filters out the ripples in the load current. Switch S is kept conducting for period T_{on} and is blocked for period T_{off}. The chopped load voltage waveform is shown in Fig. 8.5.

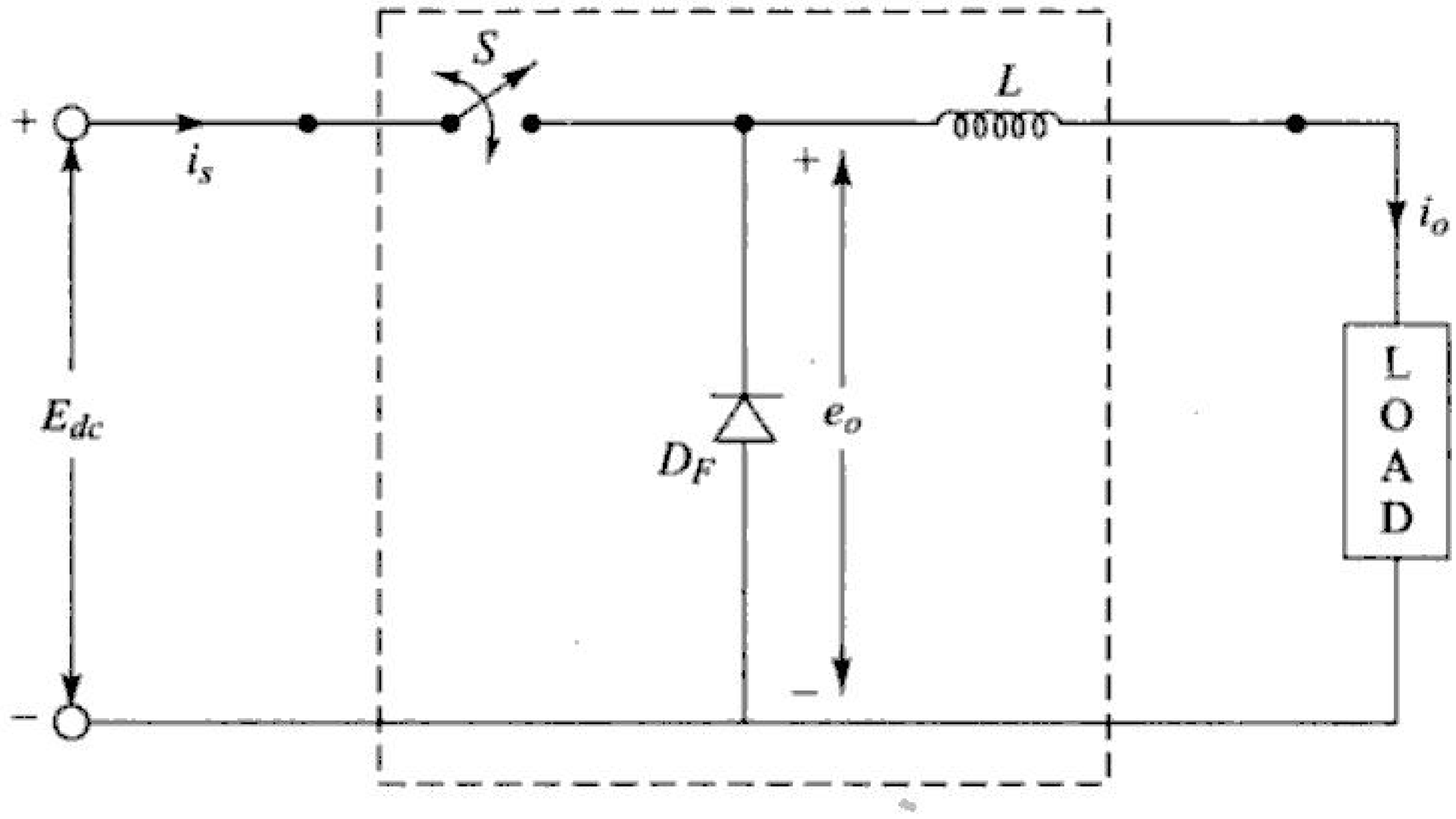

Fig. 8.4 *Basic chopper circuit*

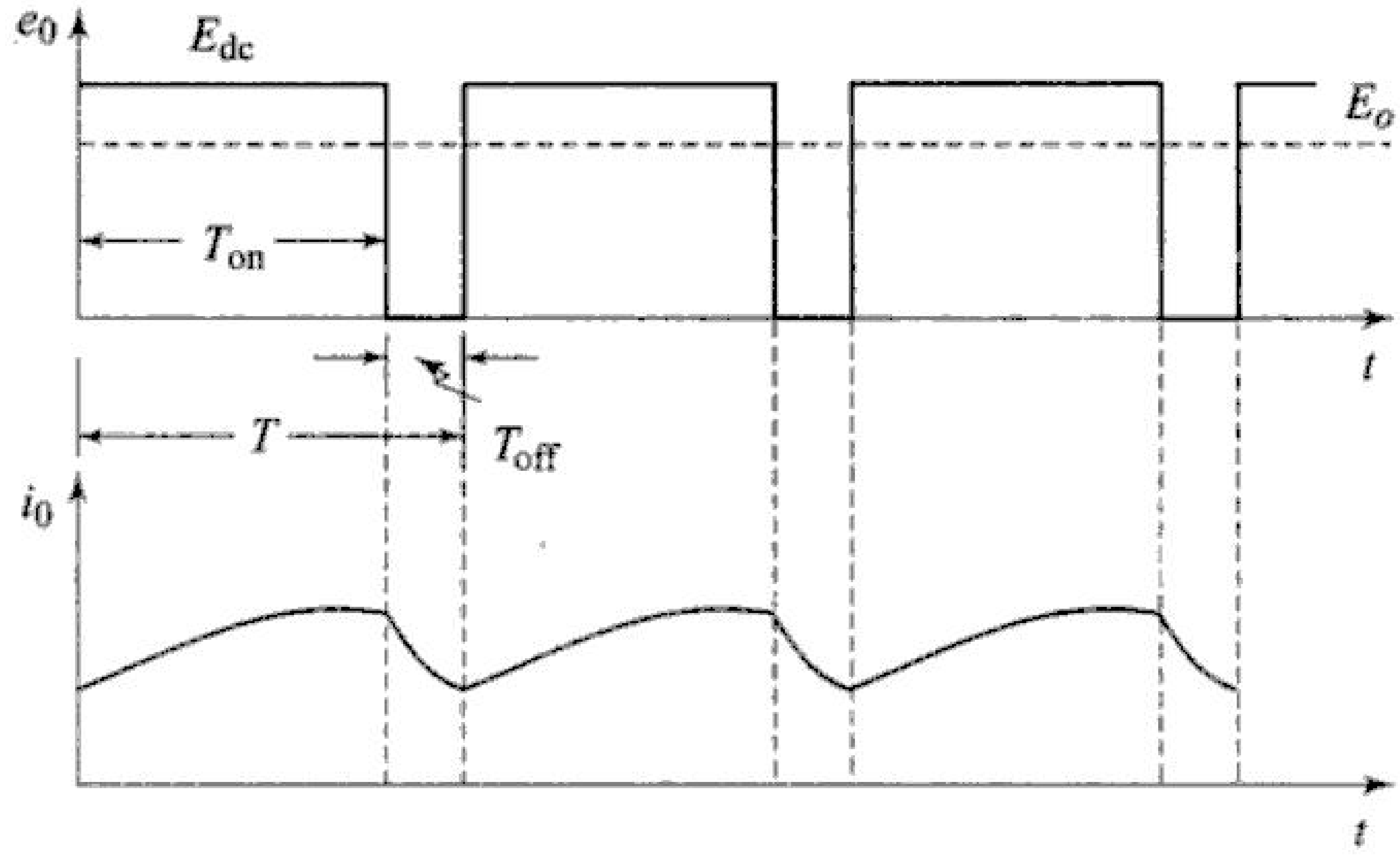

Fig. 8.5 *Output voltage and current waveforms*

During the period T_{on}, when the chopper is on, the supply terminals are connected to the load, terminals. During the interval T_{off}, when the chopper is off, load current flows through the freewheeling diode D_F. As a result, load terminals are short circuited by D_F and load voltage is therefore, zero during T_{off}. In this manner, a chopped d.c. voltage is produced at the load terminals.

From Fig. 8.5, the average load-voltage E_0 is given by

$$E_0 = E_{dc} \frac{T_{on}}{T_{on+off}} \tag{8.1}$$

where T_{on} = on-time of the chopper, T_{off} = off-time of the chopper

$T = T_{on} + T_{off}$ = chopping period

If $\alpha = \frac{T_{on}}{T}$ be the duty cycle, then above equation becomes,

$$E_0 = E_{dc} \cdot \frac{T_{on}}{T} \tag{8.2}$$

$$E_0 = E_{dc} \cdot \alpha \tag{8.3}$$

Thus, the load voltage can be controlled by varying the duty cycle of the chopper.

Also, $$E_0 = \frac{T_{on}}{T} E_{dc} = T_{on} \cdot f \cdot E_{dc} \tag{8.4}$$

where f = chopping frequency

From Eq. (8.3), it is obvious that the output voltage varies linearly with the duty-cycle. It is therefore possible to control the output voltage in the range zero to E_{dc}.

If the switch S is a transistor, the base-current will control the ON and OFF period of the transistor switch. If the switch is GTO thyristor, a positive gate pulse will turn-it ON and a negative gate pulse will turn it OFF. If the switch is an SCR, a commutation circuit is required to turn it OFF.

The average value of the load current is given by

$$I_0 = \frac{E_o}{R} = \frac{\alpha \cdot E_{dc}}{R} \tag{8.5}$$

The effective (RMS) value of the output voltage is given by

$$E_{o\,(RMS)} = \sqrt{\frac{E_{dc}^{\ 2} \cdot T_{on}}{T}} = E_{dc} \cdot \sqrt{\frac{T_{on}}{T}}$$

$$= E_{dc}\sqrt{\alpha} \tag{8.6}$$

SOLVED EXAMPLES

Example 8.1 A d.c. chopper circuit connected to a 100 V d.c. source supplies an inductive load having 40 mH in series with a resistance of 5 Ω. A freewheeling diode is placed across the load. The load current varies between the limits of 10 A and 12 A. Determine the time ratio of the chopper.

Solution: The average value of the load current $= \dfrac{I_1 + I_2}{2} = \dfrac{10+12}{2} = 11$ A.

The maximum value of the load current $= \dfrac{100}{5} = 20$ A

Now, the average value of the voltage, $E_{0av} = 100 \times \dfrac{11}{20} = 55$ V

Also, $\quad E_{dc} \cdot \dfrac{T_{on}}{T_{on} + T_{off}} = E_{0av}$ or $\dfrac{T_{on}}{T_{on} + T_{off}} = \dfrac{E_{0av}}{E_{dc}}$

$$\frac{T_{on}}{T_{on} + T_{off}} = \frac{55}{100} = 0.55 \quad \therefore T_{on} = 0.55\,(T_{on} + T_{off})$$

$$\therefore \quad \frac{T_{on}}{T_{off}} = \frac{0.55}{0.45} = 1.222.$$

Example 8.2 For the chopper circuit shown in Fig. Ex. 8.2, express the following variables as functions of E_{dc}, R, and duty cycle α.

(i) Average output voltage and current.
(ii) Output current at the instant of commutation.
(iii) Average and RMS freewheeling diode currents.
(iv) RMS value of the output voltage.
(v) RMS and average load currents.

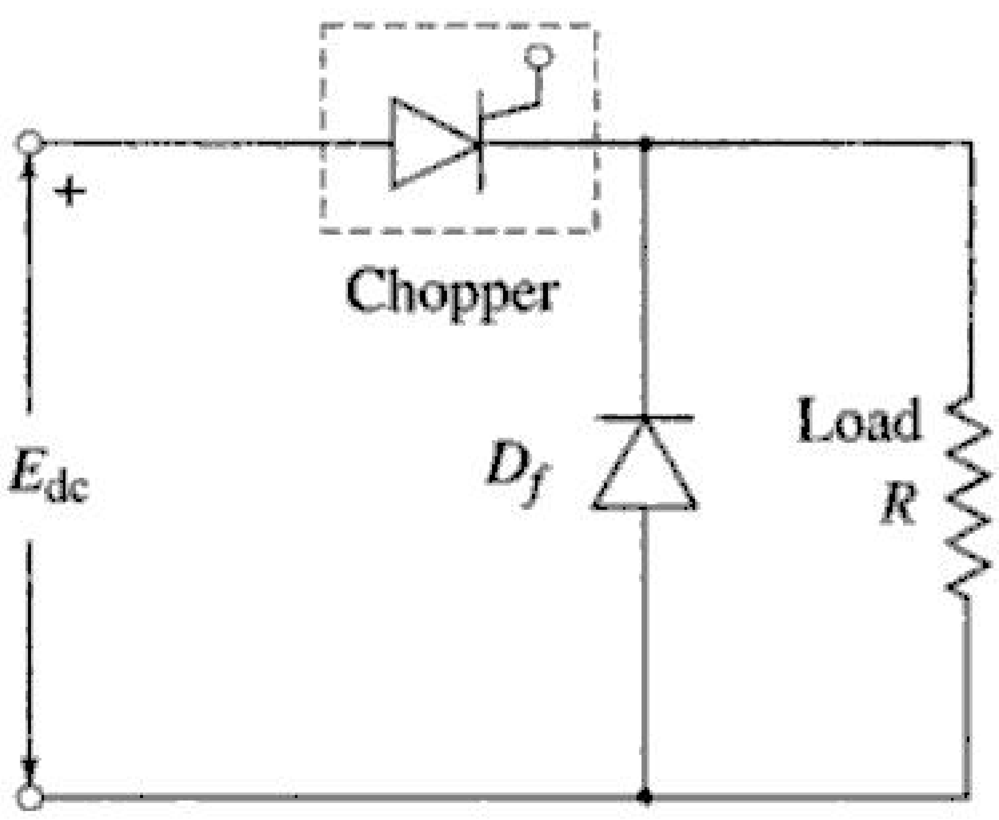

Fig. Ex. 8.2

Solution: With resistive load, load current waveforms are similar to load voltage waveforms.

$\therefore$ (i) Average output voltage $E_0 = E_{dc}\dfrac{T_{on}}{T} = E_{dc} \cdot \alpha.$

Average output current, $I_{0av} = \dfrac{E_0}{R} = \dfrac{E_{dc}}{R}\alpha.$

(ii) Output current at the instant of commutation $= \dfrac{E_{dc}}{R}$.

(iii) Freewheeling diode does not come into picture for a resistive load. Hence, average and RMS values of freewheeling diode currents are zero.

(iv) RMS value of output voltage

$$= \left[\frac{T_{on}}{T}E_{dc}^2\right]^{1/2} = \sqrt{\alpha}\cdot E_{dc}$$

(v) Now, average thyristor current

$$= \frac{E_{dc}}{R}\cdot\frac{T_{on}}{T} = \alpha\frac{E_{dc}}{R}$$

$$\text{RMS thyristor current} = \left(\alpha\cdot\left(\frac{E_{dc}}{R}\right)^2\right)^{1/2} = \sqrt{\alpha}\cdot\frac{E_{dc}}{R}$$

Example 8.3 A step-down dc chopper has a resistive load of R = 15 ohm and input voltage E_{dc} = 200 V. When the chopper remains ON, its voltage drop is 2.5 V. The chopper frequency is 1 kHz. If the duty cycle is 50%, determine:

(a) Average output voltage
(b) RMS output voltage
(c) Chopper efficiency
(d) Effective input resistance of chopper

Solution:

Given: Input voltage E_{dc} = 200 V, duty cycle α = 0.5

$R = 15\ \Omega$, F = 1 kHz, Chopper drop E_d = 2.5 V

(a) Average output voltage $E_0 = \alpha\cdot(E_{dc} - E_d)$

$= 0.5\ (200 - 2.5) = 98.75$ V

(b) RMS output voltage

$$E_{0(rms)} = \sqrt{\alpha}\ (E_{dc} - E_d) = \sqrt{0.5}\ (200 - 2.5) = 139.653\text{ V}$$

(c) Chopper efficiency

Output power, $P_0 = E_{0rms}\cdot I_{0rms}$

Now, $\quad I_{0rms} = \dfrac{E_{0rms}}{R} = \dfrac{\sqrt{\alpha}\cdot E_{dc}}{R}$

$\therefore \quad P_0 = \sqrt{\alpha}\cdot E_{dc}\cdot\dfrac{\sqrt{\alpha}\cdot E_{dc}}{R} = \dfrac{\alpha E_{dc}^2}{R}$

If E_d is the chopper drop, then

$$P_0 = \frac{\alpha(E_{dc} - E_d)^2}{R} = \frac{0.5(200 - 2.5)^2}{15} = 1300.21\ \omega$$

Now, the input power to the chopper is given by

$$P_i = \frac{1}{T}\int_0^T E_{dc}\ i_s\ dt = \frac{1}{T}\int_0^{T_{on}} E_{dc}\frac{(E_{dc} - E_d)}{R}\ dt = \frac{1}{T}\int_0^{\alpha \cdot T} \frac{E_{dc}(E_{dc} - E_d)}{R}\ dt$$

$$= \frac{E_{dc}(E_{dc} - E_d)}{T.R.}(t)_o^{\alpha_T} = \frac{\alpha E_{dc}(E_{dc} - E_d)}{R.} = \frac{0.5(200)(200 - 2.5)}{15} = 1316.67\text{ W}$$

$\therefore$ Chopper efficiency, $\eta = \frac{P_o}{P_i} = \frac{1300.21}{1316.67} = 0.9874 = 98.74\%$

8.3.2 Principle of Step-up Choppers

The chopper configuration of Fig. 8.4 is capable of giving a maximum voltage that is slightly smaller than the input d.c. voltage (i.e. $E_0 < E_{dc}$). Therefore, the chopper configuration of Fig. 8.4 is called as step-down choppers. However, the chopper can also be used to produce higher voltages at the load than the input voltage (i.e., $E_0 \geq E_{dc}$). This is called as step-up chopper and is illustrated in Fig. 8.6.

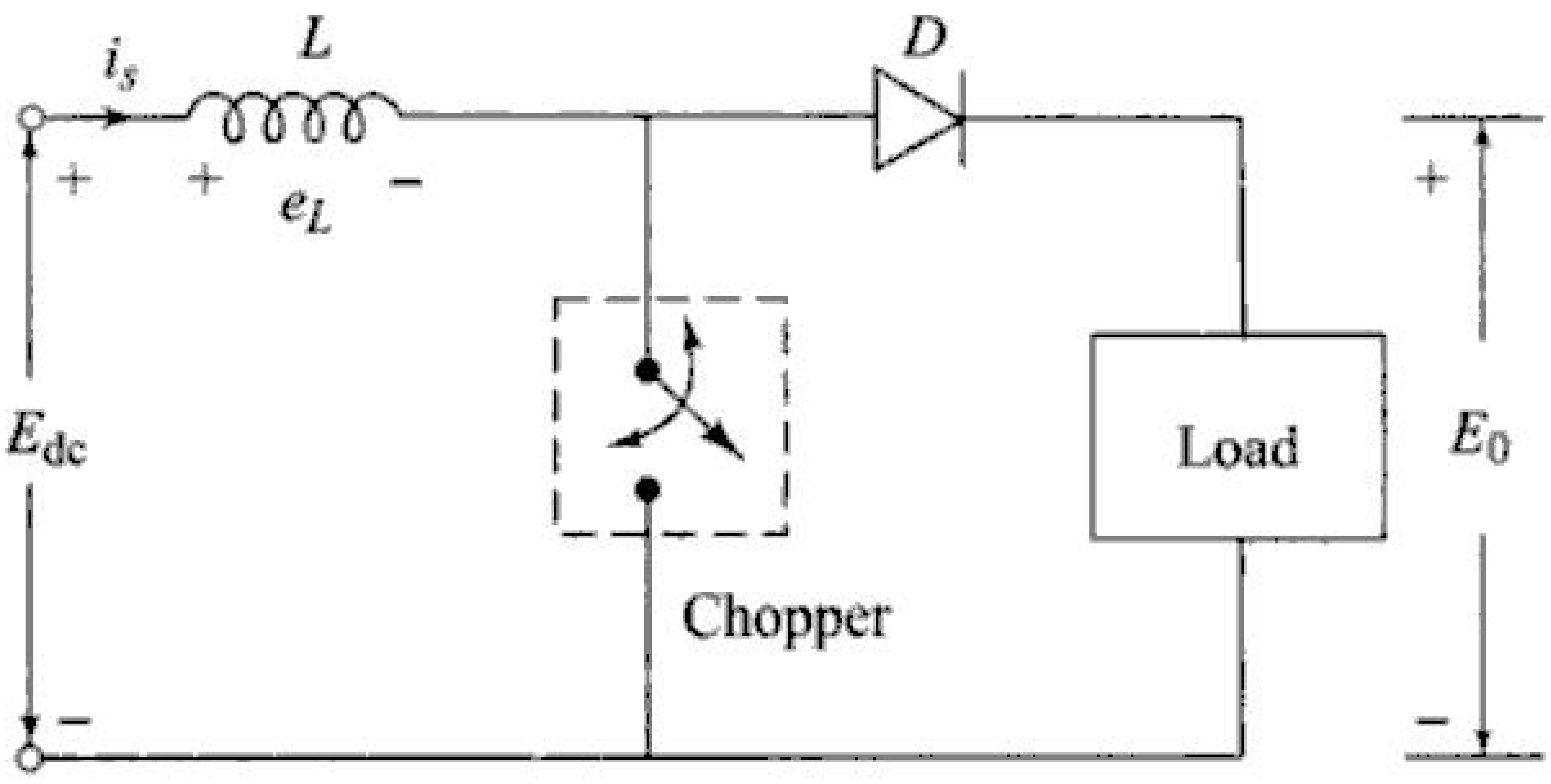

Fig. 8.6 *Step-up chopper or boost choppers*

When the chopper is ON, the inductor L is connected to the supply E_{dc}, and inductor stores energy during on-period, T_{on}.

When the chopper is OFF, the inductor current is forced to flow through the diode and load for a period T_{off}. As the current tends to decrease, polarity of the emf induced in inductor L is reversed to that of shown in Fig. 8.6, and as a result voltage across the load E_0 becomes

$$E_0 = E_{dc} + L\frac{di_s}{dt}$$

that is, the inductor voltage adds to the source voltage to force the inductor current into the load. In this manner, the energy stored in the inductor is released to the load. Here, higher value of inductance L is preferred for getting lesser ripple in the output.

During the time T_{on}, when the chopper is ON, the energy input to the inductor from the source is given by

$$W_i = E_{dc}\, I_s\, T_{on} \tag{8.7}$$

Equation 8.7 is based on the assumption that the source current is free from ripples.

Now, during the time T_{off}, when chopper is OFF, energy released by the inductor to the load is given by

$$W_0 = (E_0 - E_{dc})\, I_s\, T_{off} \tag{8.8}$$

Considering the system to be lossless, and, in the steady-state, these two energies will be equal.

$$\therefore \quad E_{dc} \cdot I_s\, T_{on} = (E_0 - E_{dc})\, I_s\, T_{off}$$

or
$$E_0 = E_{dc} \frac{T_{on} + T_{off}}{T_{off}} \tag{8.9}$$

or
$$E_0 = E_{dc} \frac{T}{T - T_{on}} \tag{8.10}$$

or
$$E_0 = E_{dc} \frac{1}{T/T - T_{on}/T}, \text{ But, } \frac{T_{on}}{T} = \alpha$$

$$\therefore \quad E_0 = \frac{E_{dc}}{1-\alpha} \tag{8.11}$$

For $\alpha = 0$, $E_0 = E_{dc}$; and $\alpha = 1$, $E_0 = \infty$.

Hence, for variation of a duty cycle α in the range $0 < \alpha < 1$, the output voltage E_0 will vary in the range $E_{dc} < E_0 < \infty$. This principle of step-up chopper can be employed for regenerative breaking of the d.c. motors even at lower operating speeds. Let E_{dc} represent the d.c. motor generated voltage and E_0 the d.c. source voltage in Fig. 8.6. Regenerative breaking takes place when $\left(E_{dc} + L\frac{di_s}{dt}\right)$ exceeds E_0. Even at decreasing motor speeds, duty cycle α can be so adjusted that $\left(E_{dc} + L\frac{di_s}{dt}\right)$ is more than the fixed supply voltage E_0.

Solved Example

Example 8.4 A step-up chopper is used to deliver load voltage of 500 V from a 220V d.c. source. If the blocking period of the thyristor is 80 μs, compute the required pulse width.

Solution: From Eq. (8.10) we have, $E_0 = E_{dc} \frac{T_{on} + T_{off}}{T_{off}}$

$$\therefore \quad 500 = 220 \frac{T_{on} + 80 \times 10^{-6}}{80 \times 10^{-6}}, \quad \therefore T_{on} = 101.6 \times 10^{-6} = 101.6\ \mu s.$$

8.3.3 Principle of Step-Up/Down Choppers

A chopper can also be used both in step-up and step-down modes by continuously varying its duty cycle. The principle of operation is illustrated in Fig. 8.7. As shown, the output, voltage polarity is opposite to that of input voltage E_{dc}.

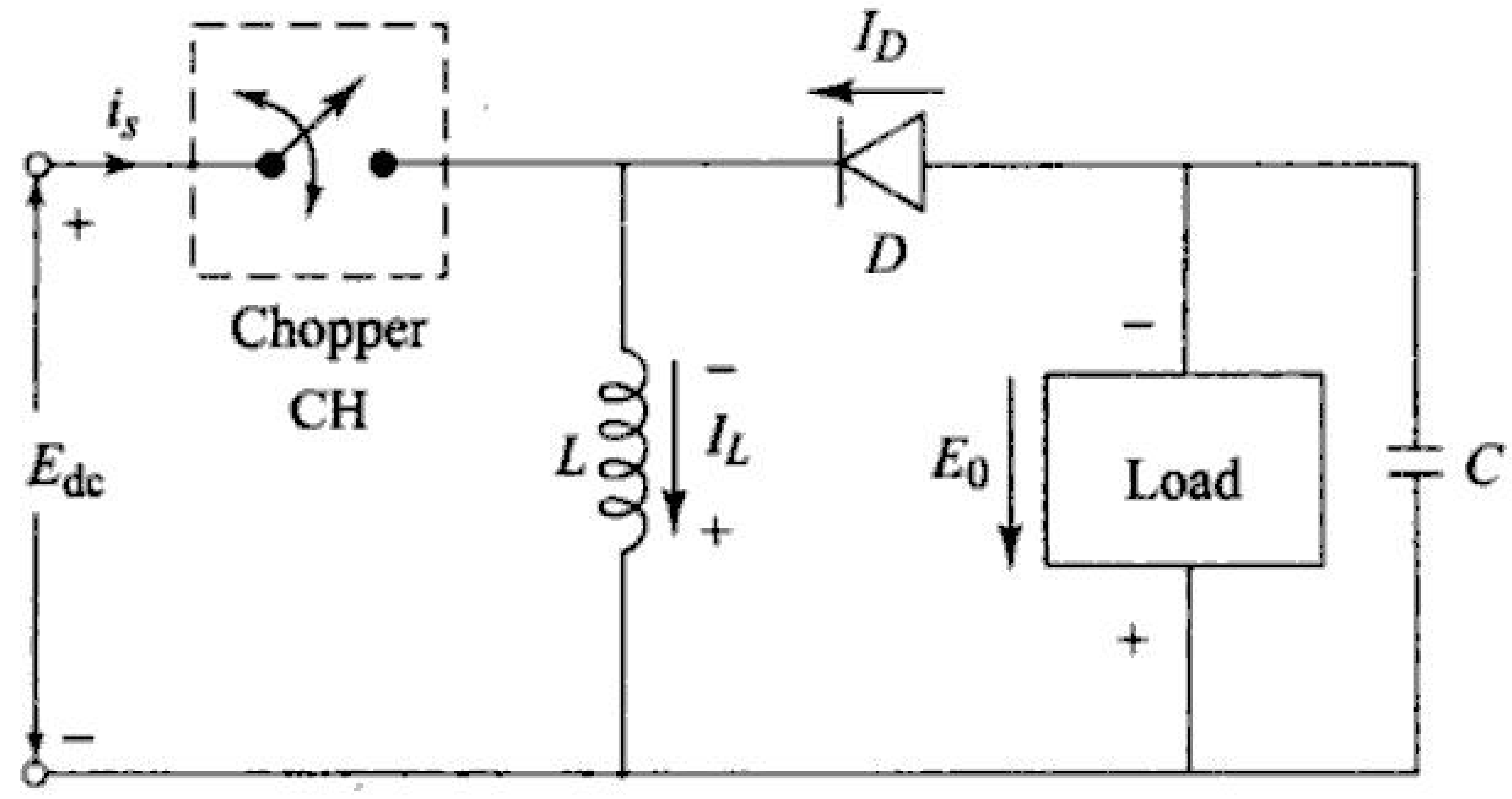

Fig. 8.7 *Step-up/down chopper*

When the chopper is ON, the supply current flows through the path $E_{dc+} - CH - L - E_{dc-}$. Hence, inductor L stores the energy during the T_{on} period.

When the chopper CH is OFF, the inductor current tends to decrease and as a result, the polarity of the emf induced in L is reversed as shown in Fig. 8.7. Thus, the inductance energy discharges in the load through the path,

$$L_+ - \text{Load} - D - L_-.$$

During T_{on}, the energy stored in the inductance is given by

$$W_i = E_{dc} I_s T_{on} \tag{8.12}$$

During T_{off}, the energy fed to the load is

$$W_o = E_0 I_s T_{off} \tag{8.13}$$

For a lossless system, in steady-state: Input energy, W_i = output energy, W_o

$$\therefore \quad E_{dc} \cdot I_s \cdot I_{on} = E_0 I_s T_{off}, \text{ or } E_0 = E_{dc} \cdot \frac{T_{on}}{T_{off}} \tag{8.14}$$

or $$E_0 = E_{dc} \cdot \frac{T_{on}}{T - T_{on}} = E_{dc} \cdot \frac{1}{T/T_{on} - T_{on}/T_{on}}$$

Substituting $$\frac{T_{on}}{T} = \alpha, \text{ we get, } E_0 = E_{dc} \cdot \frac{1}{1/\alpha - 1}$$

or $$E_0 = E_{dc} \frac{\alpha}{1-\alpha} \tag{8.15}$$

For $0 < \alpha < 0.5$, the step-down chopper operation is achieved and for $0.5 < \alpha < 1$, step-up chopper operation is obtained.

8.4 CONTROL STRATEGIES

It is seen from Eq. (8.3), that, average value of output voltage, E_0 can be controlled by periodic opening and closing of the switches. The two types of control strategies for operating the switches are employed in d.c. choppers. They are:

(1) Time-ratio control (TRC), and
(2) Current limit control.

8.4.1 Time-Ratio Control (TRC)

In the time-ratio control, the value of $\frac{T_{on}}{T}$ is varied. This is effected in two ways. They are variable frequency operation and constant frequency operation.

1. Constant Frequency System In this type of control strategy, the on-time T_{on}, is varied but the chopping frequency f ($f = 1/T$, and hence the chopping period T) is kept constant. This control strategy is also called as the *pulse-width modulation control.*

Figure 8.8 illustrates the principle of pulse-width modulation. As shown, chopping period T is constant. In Fig. 8.8(a), $T_{on} = \frac{1}{4}T$, so that duty cycle $\alpha = 25\%$. In Fig. 8.8 (b), $T_{on} = \frac{3}{4}T$, so that duty cycle $\alpha = 75\%$. Hence, the output voltage E_0 can be varied by varying the on-time T_{on}.

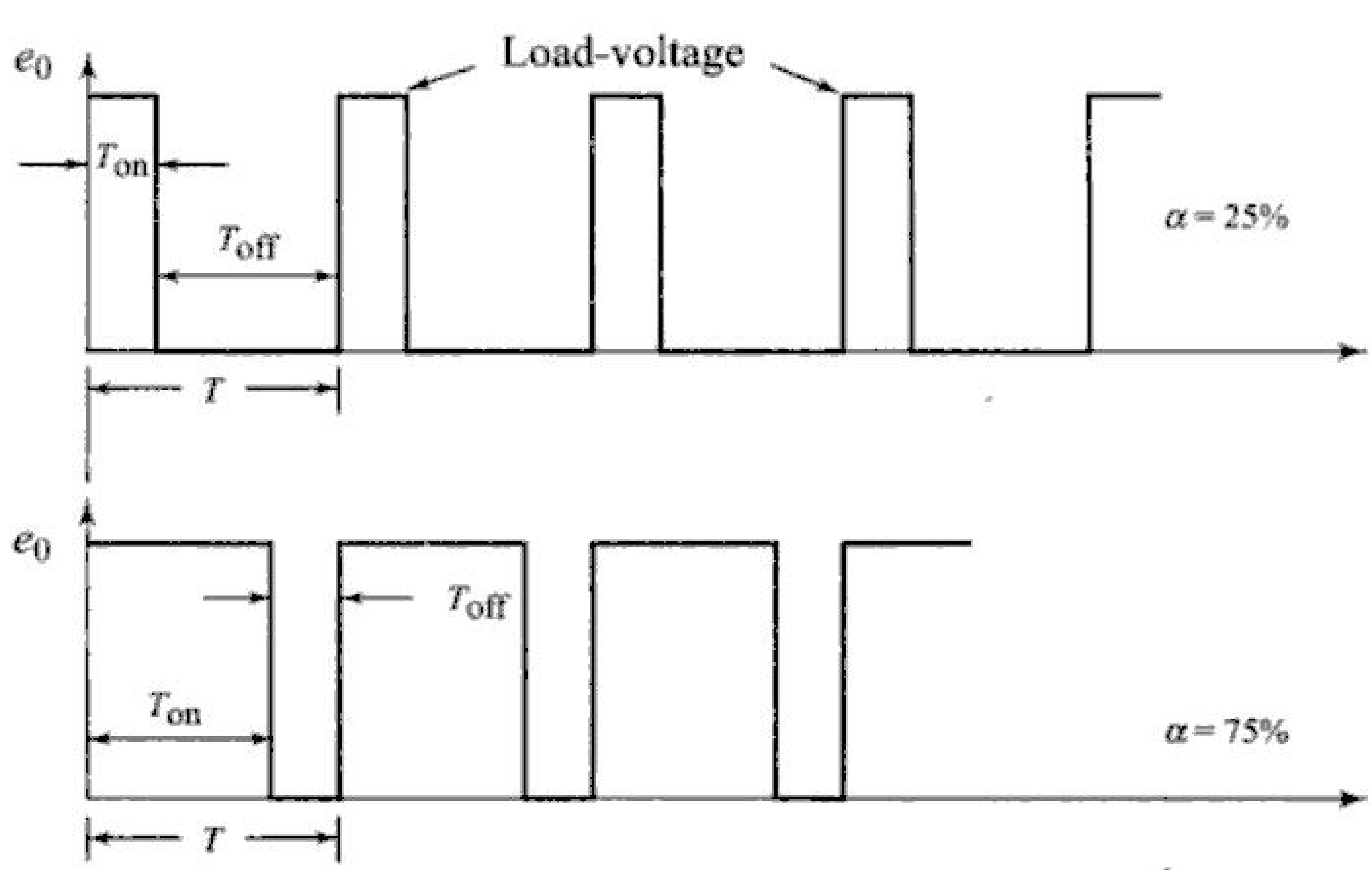

Fig. 8.8 *Pulse-width modulation control (constant frequency f)*

2. Variable Frequency System In this type of control strategy, the chopping frequency f is varied and either–

(a) ON-time, T_{on}, is kept constant or (b) OFF-time, T_{off}, is kept constant. This type of control strategy is also called as *frequency modulation control.*

Figure 8.9 illustrates the principle of frequency modulation. As shown in Fig. 8.9(a), chopping period T is varied but on-time T_{on} is kept constant. The output voltage waveforms are shown for two different duty cycles. In Fig. 8.9(b), chopping period T is varied but T_{off} is kept constant.

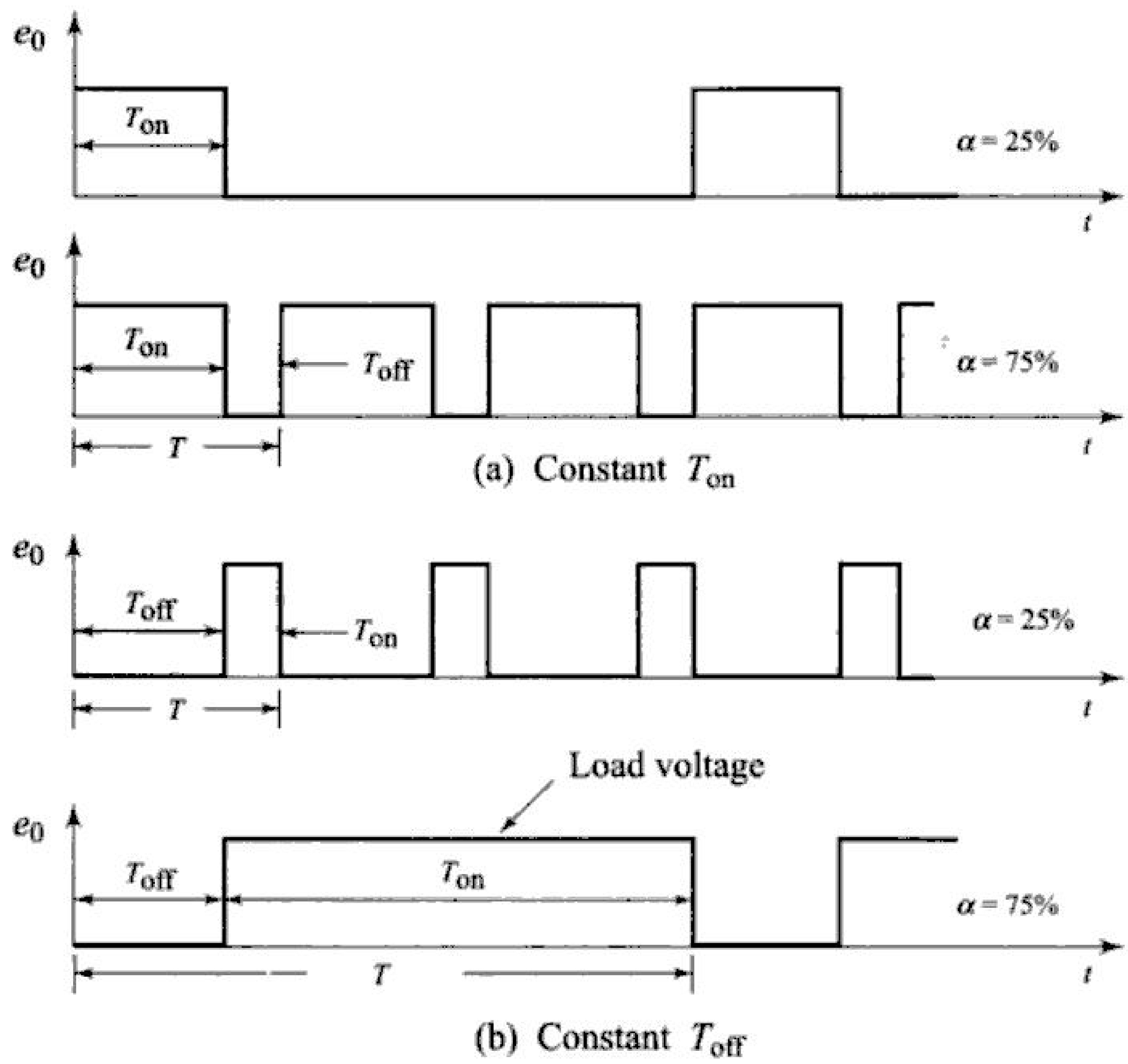

Fig. 8.9 *Output voltage waveforms for variable frequency system*

Frequency modulation control strategy has the following major disadvantages compared to pulse-width modulation control.

(i) The chopping frequency has to be varied over a wide range for the control of output voltage in frequency modulation. Filter design for such wide frequency variation is, therefore, quite difficult.

(ii) For the control of duty cycle, frequency variation would be wide. As such, there is a possibility of interference with signalling and telephone lines in frequency modulation technique.

(iii) The large OFF-time in frequency modulation technique may make the load current discontinuous, which is undesirable.

Thus, the constant frequency system (PWM) is the preferred scheme for chopper drives.

8.4.2 Current Limit Control

In current limit control strategy, the chopper is switched ON and OFF so that the current in the load is maintained between two limits. When the current exceeds upper limit, the chopper is switched OFF. During OFF period, the load current freewheels and decreases exponential. When it reaches the lower limit, the chopper is switched ON. Current limit control is possible either with constant frequency or with constant T_{on}. The current limit control is used only when the load has energy storage elements. The reference values are the load current or load-voltage. Figure 8.10 illustrates the principle of current limit control. Since the chopper operates between prescribed current limits, discontinuity cannot occur. The difference between I_{0max} and I_{0min}, decides the switching frequency. The ripple in the load current can be reduced if the difference between the I_{0max} and I_{0min} limits is minimum. This in turn increases chopper frequency thereby increasing the switching losses.

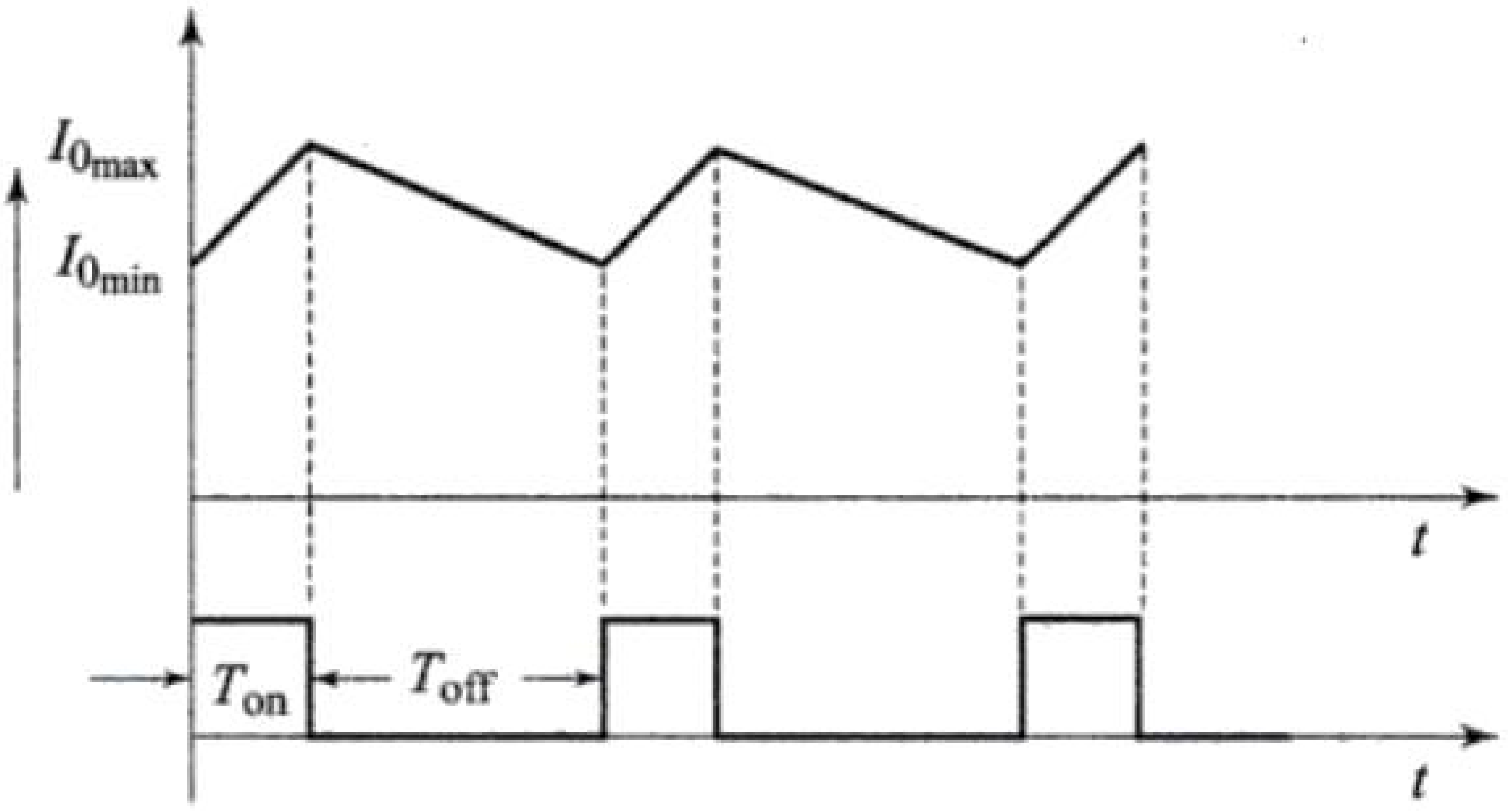

Fig. 8.10 *Current limit control*

SOLVED EXAMPLES

Example 8.5 A chopper circuit is operating on TRC principle at a frequency of 2 kHz on a 220 V d.c. supply. If the load voltage is 170 V, compute the conduction and blocking period of thyristor in each cycle.

Solution: From Eq. (8.2), $E_0 = E_{dc} \cdot T_{on} \cdot f$

Given : $f = 2$ kHz, $E_{dc} = 220$ V, $E_o = 170$.

Conduction period, $$T_{on} = \frac{E_0}{E_{dc} \cdot f} = \frac{170}{220 \times 2 \times 10^3} = T_{on} = 0.386 \text{ ms.}$$

But, chopping period, $$T = \frac{1}{f} = \frac{1}{2 \times 10^3} = 0.5 \text{ ms}$$

$\therefore$ Blocking period of SCR, $T_{off} = T - T_{on} = 0.5 - 0.386 = 0.114$ m sec.

Example 8.6 In a 110 V dc chopper drive using the CLC scheme, the maximum possible value of the accelerating current is 300 A, the lower-limit of the current pulsation is 140 A. The ON- and OFF periods are 15 ms and 12 ms, respectively. Calculate the limit of current pulsation, chopping frequency, duty cycle and the output voltage.

Solution: Given: $T_{on} = 15$ ms, $T_{off} = 12$ ms, $I_{0max} = 300\,A$, $I_{0min} = 140\,A$

Now, maximum limit of current pulsation = 300 – 140 = 160 A.

$$\text{Chopping frequency} = \frac{1}{T} = \frac{1}{15+12} = 37 \text{ Hz \& ratio, } \alpha = \frac{T_{on}}{T} = \frac{15}{27} = 0.56$$

$$\text{Output voltage, } E_0 = \alpha E_{dc} = 0.56 \times 110 = 61.60 \text{ V}$$

8.5 CHOPPER CONFIGURATION

Choppers may be classified according to the number of quadrants of the $E_0 - I_0$ diagram in which they are capable of operating. A classification that is convenient for the discussion that follows is shown in Fig. 8.11. The polarity of the output voltage and the direction of energy flow cannot be changed in Figs 8.4 and 8.6. By various combination of connections it is possible to realize any combination of output voltage and current polarity. With reference to the combination shown in Fig. 8.11, if the load is a separately excited motor of constant field, then the positive voltage and positive current in the first quadrant give rise to a "forward drive." Changing the polarity of both the armature voltage and the armature current results in a "reverse" drive (quadrant III). In II and IV quadrants, the direction of energy flow is reversed and the motor operates as a *generator braking* rather than driving.

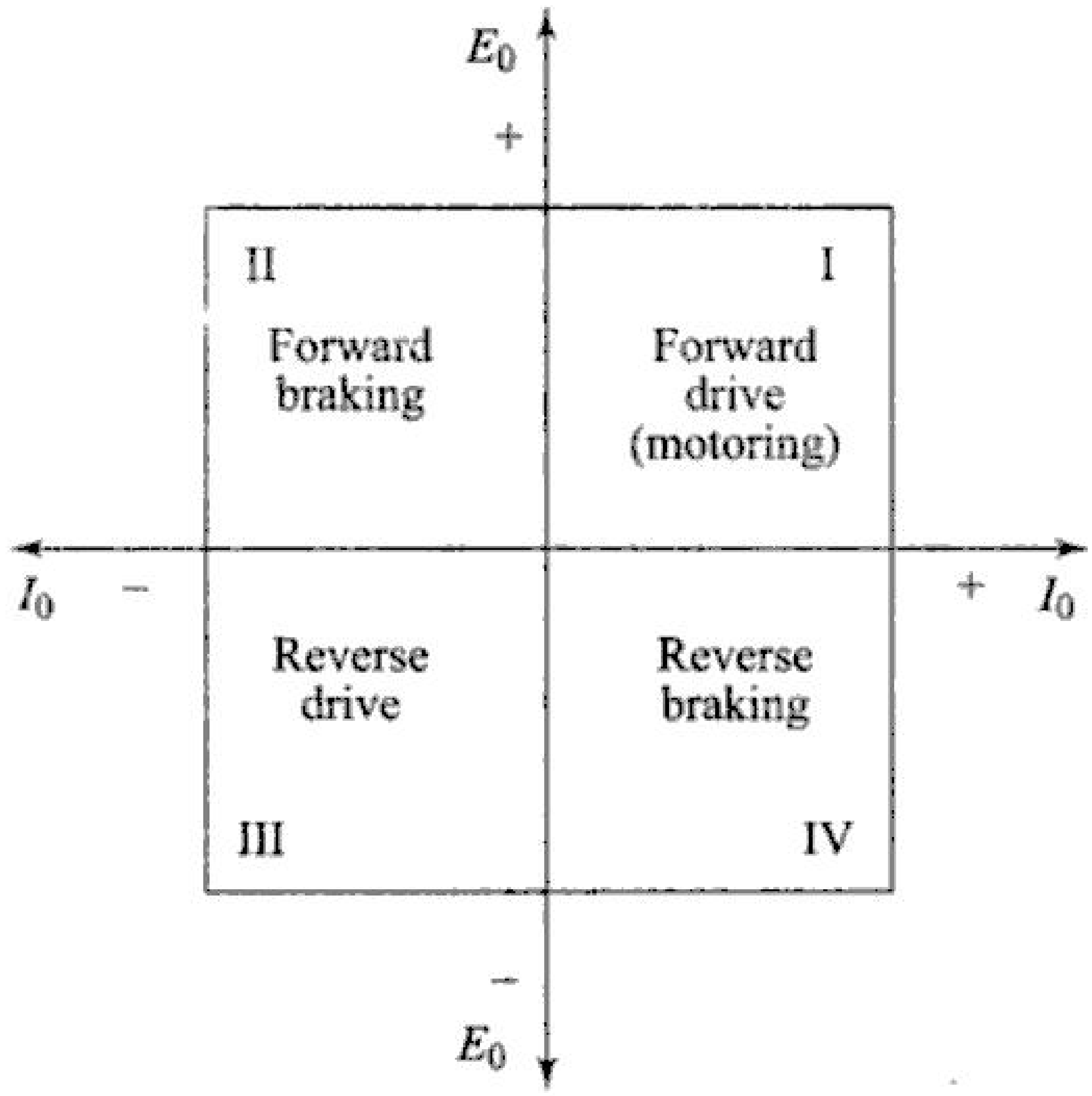

Fig. 8.11 *Polarities of output voltage and current*

In regenerative breaking, most of the breaking energy is returned to the supply. The condition for regeneration is that the rotational emf must be more than the applied voltage so that the current is reversed and the mode of operation changes from motoring to generating. It was observed that about 35% of the energy put into an automotive vehicle during typical urban traction is theoretically recoverable by regenerative breaking. However, the exact value of the recoverable energy is a function of the type of driving, the efficiency of the drive train, gear ratios in the drive/train etc. Therefore, the choppers which gives this regenerative breaking facility are widely used compared to systems without regenerative breaking.

D.C. chopper circuits are combined in accordance with the quadrants, in which a d.c. motor assumed as a load is required to operate. In the first and third quadrants, for instance, a resistance may also serve as a load, but a generating mode can be maintained over any significant span of time only, if the load is capable of delivering sustained power. This section describes the classification of various chopper configurations.

8.5.1 First Quadrant or Class A Chopper [Step-down Chopper with R–L Load]

Figure 8.12 illustrates the basic power circuit of first quadrant chopper. The term 'first quadrant' signifies that circuit parameters E_0 and I_0 occur only in the first quadrant of $E_0 - I_0$ diagram.

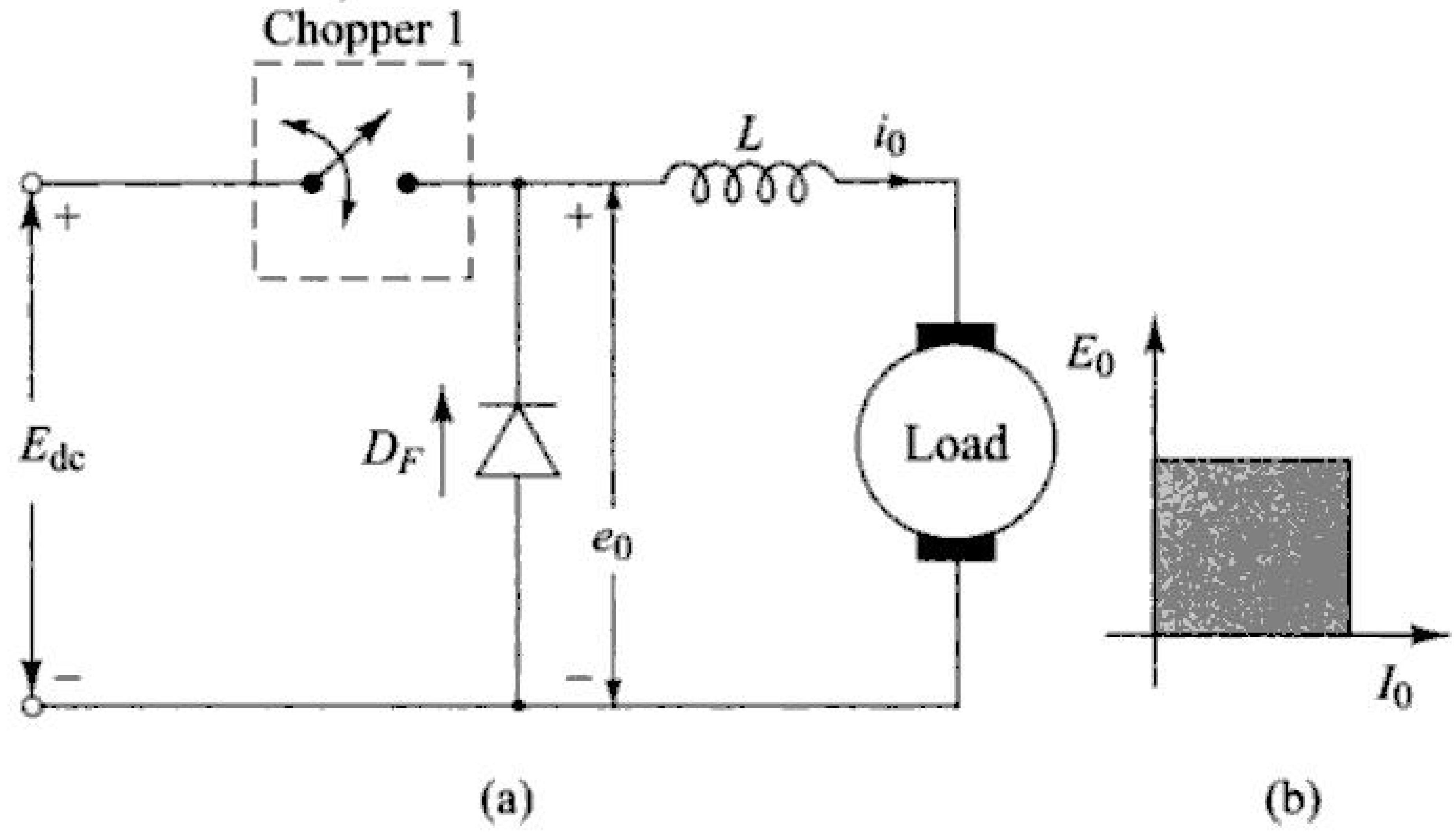

Fig. 8.12 *Type A chopper circuit and $E_0 - I_0$ characteristic*

Commutating circuitry is not shown in Fig. 8.12 for simplicity. When the chopper CH_1 is ON, $e_0 = E_{dc}$ and current flows in the direction shown in Fig. 8.12. When the chopper CH_1 is OFF, $e_0 = 0$ but the current i_0 flows in the load in the same direction through freewheeling diode D_f. Therefore, both average load voltage E_0 and current I_0 are positive and thus power flows from source to load. This operation is shown by the hatched area in Fig. 8.12(b). Therefore, this configuration is used for motoring operation of d.c. motor load. Class A chopper circuit is also called as step-down chopper as average output voltage E_0 is always less than the d.c. input voltage E_{dc}. Due to the motoring operation, this chopper is also called as motoring chopper.

1. Steady-state Time-domain Analysis Class A chopper circuit of Fig. 8.12 can also be drawn in terms of three separate circuit elements, as shown in Fig. 8.13. Here, load is R–L E_b type load. E_b is the load voltage which may be a d.c. motor or a battery.

The operation of this system may be understood from the consideration of the waveforms of the circuit variables shown in Fig. 8.14. This Fig. 8.14 shows the two modes of circuit operation.

(i) When chopper CH_1 is ON, the supply voltage E_{dc} appears at the terminals of the armature circuit and, the current i_0 would increase until it reached the steady-state value expressed by

$$i_0 = \frac{E_{dc} - E_b}{R} \tag{8.16}$$

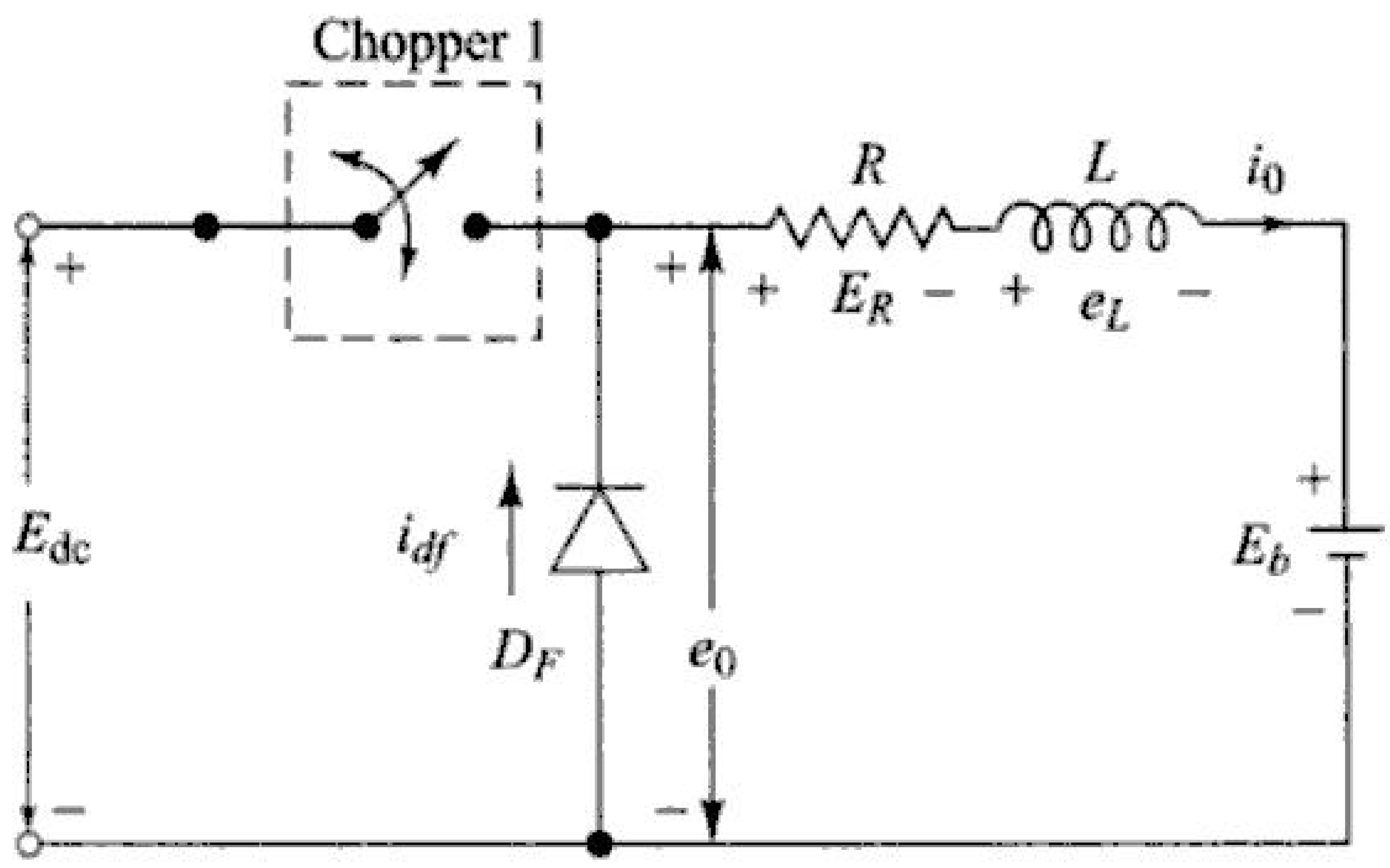

Fig. 8.13 *First quadrant chopper with R – L load*

The average current I_0 in the circuit can be controlled by commutating chopper CH_1 before the current has reached the value given by Eq. (8.16), and allowing it to decay through diode DF either to zero, as shown in Fig. 8.14(a), or to some lower value than it had attained while CH_1 was conducting, as shown in Fig. 8.14(b). If this process of turning chopper CH_1 ON and OFF is repeated at regular intervals, then average value of i_0 is controlled.

As shown in Fig. 8.14(a), the turn-on time of chopper T_{on} is shorter in relation to chopping period T, which results in a discontinuous current. Therefore, the current waveform consists of a series of pulses and these pulses become identical when steady-state conditions have been reached.

If turn-on time T_{on} is longer in relation to T, the load current will not decay to zero during the interval $T_{on} < t < T$, but will merely decrease until CH_1 is again turned-on. Therefore, in the steady state, the current will flow continuously as shown in Fig. 8.14(b).

***Mode 1*: $0 \le t \le T_{on}$** When the chopper is ON, current flows through the path $E_{dc+} - R - L - E_b - E_{dc-}$. For this mode of operation, the differential equation governing its performance is given by

$$E_{dc} = R \cdot i_0 + L\frac{di_0}{dt} + E_b,\ \text{for } 0 \le t \le T_{on} \tag{8.17}$$

***Mode 2*: $T_{on} \le t \le T$** When chopper is OFF, the load current continuously flowing through the freewheeling diode D_f. For this mode of operation, the differential equation governing its performance is given by

$$0 = R \cdot i_0 + L\frac{di_0}{dt} + E_b,\ \text{for } T_{on} \le t \le T \tag{8.18}$$

From Fig. 8.14(b), it is observed that the initial value of current for Eq. (8.17) is I_{0min} and I_{0max} for Eq. (8.18).

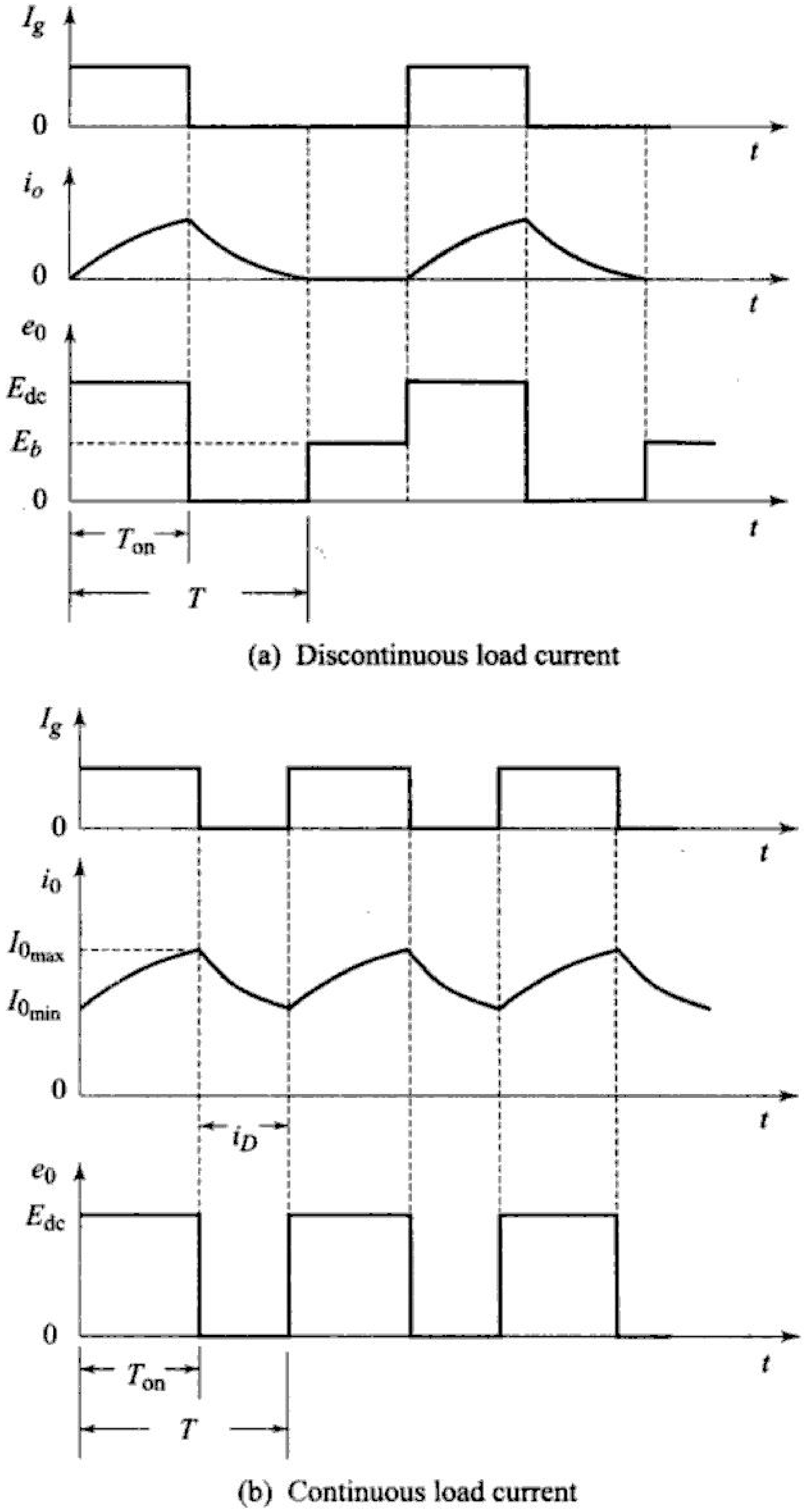

Fig. 8.14 *First quadrant chopper, two modes operation*

Now, by taking Laplace-transforms of Eqs (8.17) and (8.18), we can write

$$\frac{(E_{dc} - E_b)}{s} = R\, I_{0(s)} + L[sI_{0(s)} - I_{0\min}] \tag{8.19}$$

and

$$\frac{-E_b}{s} = RI_{0(s)} + L[sI_{0(s)} - I_{0\max}] \tag{8.20}$$

Equation 8.19 can also be written as

$$I_0(s) = \frac{(E_{dc} - E_b)}{s(R + Ls)} + \frac{LI_{0\min}}{(R + Ls)}$$

or
$$I_0(s) = \frac{(E_{dc} - E_b)}{sL(s + R/L)} + \frac{L \cdot I_{0\min}}{L(s + R/L)}$$

or
$$I_0(s) = \frac{(E_{dc} - E_b)}{sL(s + R/L)} + \frac{I_{0\min}}{(s + R/L)} \tag{8.21}$$

Now, by taking inverse-Laplace of Eq. 8.21, we get

$$i_0(t) = \frac{(E_{dc} - E_b)}{R}\left(1 - e^{-R/L \cdot t}\right) + I_{0\min} \cdot e^{-R/L \cdot t},\ 0 \le t \le T_{on} \tag{8.22}$$

Let us define time-constant, $\tau = L/R$, so Eq. (8.22) becomes

$$i_0(t) = \frac{(E_{dc} - E_b)}{R}\left(1 - e^{-t/\tau}\right) + I_{0\min} \cdot e^{-t/\tau}, 0 \le t \le T_{on} \tag{8.23}$$

When chopper is commutated at $t = T_{on}$, $i_0(t) = I_{0\max}$.
Thus, Eq. (8.23) becomes

$$I_{0\max} = \frac{(E_{dc} - E_b)}{R}\left(1 - e^{-T_{on}/\tau}\right) + I_{0\min}\, e^{-T_{on}/\tau} \tag{8.24}$$

From Eq. (8.20), we can write, $I_{0(s)}\,[R + Ls] = \dfrac{-E_b}{s} + L \cdot I_{0\max}$

or $I_{0(s)} = \dfrac{-E_b}{s(R + Ls)} + \dfrac{L \cdot I_{0\max}}{(R + Ls)}$ = or $I_{0(s)} = \dfrac{-E_b}{s \cdot L \cdot (s + R/L)} + \dfrac{L \cdot I_{0\max}}{(s + R/L)}$

or
$$I_{0(s)} = \frac{-E_b}{sL(s + R/L)} + \frac{I_{0\max}}{(s + R/L)} \tag{8.25}$$

Now, by taking inverse-Laplace transform of Eq. (8.25) we get

$$i_{0(t)} = \frac{-E_b}{R}\left(1 - e^{-t/\tau}\right) + I_{0\max}e^{-t/\tau}, T_{on} \le t \le T \tag{8.26}$$

For interval $T_{on} \le t \le T$, let us define $t' = t - T_{on}$, so that when

$t = T_{on}$, $t' = 0$, and for $t = T$, $t' = T - T_{on} = T_{off}$.

Substituting t' in Eq. (8.26), we get

$$i_0(t') = \frac{-E_b}{R}\left(1 - e^{-t'/\tau}\right) + I_{0\max}e^{-t'/\tau}, T_{on} \le t \le T \tag{8.27}$$

Now, at $t' = T - T_{on} = T_{off}$, $i_0(t') = I_{0\min}$.
Thus, Eq. (8.27) becomes

$$\therefore \quad I_{0\min} = \frac{-E_b}{R}\left(1 - e^{-(T - T_{on})/\tau}\right) + I_{0\max}e^{-(T - T_{on})/\tau} \tag{8.28}$$

Equations (8.24) can be solved for $I_{0\max}$ and $I_{0\min}$, as follows:
From Eq. (8.24), we can write

$$I_{0\max} = \frac{E_{dc}}{R}\left(1 - e^{-T_{on}/\tau}\right) - \frac{E_b}{R}\left(1 - e^{-T_{on}/\tau}\right) + I_{0\min} e^{-T_{on}/\tau} \tag{8.29}$$

Substituting Eq. (8.28) for $I_{0\min}$ in Eq. (8.29), gives

$$I_{0\max} = \frac{E_{dc}}{R}\left(1 - e^{-T_{on}/\tau}\right) - \frac{E_b}{R}\left(1 - e^{-T_{on}/\tau}\right)$$

$$- \frac{E_b}{R} e^{-T_{on}/\tau}\left(1 - e^{-(T - T_{on})/\tau}\right) + I_{0\max} e^{-(T - T_{on})/\tau} \cdot e^{-T_{on}/\tau}$$

$$= \frac{E_{dc}}{R}\left(1 - e^{-T_{on}/\tau}\right) - \frac{E_b}{R} + \frac{E_b}{R} e^{-T_{on}/\tau} - \frac{E_b}{R} e^{-T_{on}/\tau}$$

$$+ \frac{E_b}{R} e^{-(T - T_{on})/\tau} e^{-T_{on}/\tau} + I_{0\max} e^{-T/\tau} e^{+T_{on}/\tau} e^{-T_{on}/\tau}$$

$$= \frac{E_{dc}}{R}\left(1 - e^{-T_{on}/\tau}\right) - \frac{E_b}{R}\left(1 - e^{-T/\tau}\right) + I_{0\max} e^{-T/\tau}$$

or,

$$I_{0\max} - I_{0\max} e^{-T/\tau} = \frac{E_{dc}}{R}\left(1 - e^{-T_{on}/\tau}\right) - \frac{E_b}{R}\left(1 - e^{-T/\tau}\right)$$

$$I_{0\max}(1 - e^{-T/\tau}) = \frac{E_{dc}}{R}\left(1 - e^{-T_{on}/\tau}\right) - \frac{E_b}{R}\left(1 - e^{-T/\tau}\right)$$

or,
$$I_{0\max} = \frac{E_{dc}}{R}\left[\frac{1 - e^{-T_{on}/\tau}}{1 - e^{-T/\tau}}\right] - \frac{E_b}{R} \tag{8.30}$$

Now, substitute value of $I_{0\max}$ from Eq. (8.30) into Eq. (8.28),

$$\therefore \quad I_{0\min} = \frac{-E_b}{R} + \frac{E_b}{R} e^{-(T - T_{on})/\tau} + \frac{E_{dc}}{R}\left[\frac{1 - e^{-T_{on}/\tau}}{1 - e^{-T/\tau}}\right]$$

$$\times e^{-(T - T_{on})/\tau} - \frac{E_b}{R} e^{-(T - T_{on})/\tau}$$

$$= \frac{E_{dc}}{R}\left[\frac{1 - e^{-T_{on}/\tau}}{1 - e^{-T/\tau}}\right]\frac{e^{T_{on}/\tau}}{e^{T/\tau}} - \frac{E_b}{R}$$

or,
$$I_{0\min} = \frac{E_{dc}}{R}\left[\frac{e^{+T_{on}/\tau} - 1}{e^{+T/\tau} - 1}\right] - \frac{E_b}{R} \tag{8.31}$$

When chopper CH_1 is continuously turned-on, then, $T_{on} = T$ and both I_{0max} and I_{0min} have the value given by Eq. (8.16), i.e.

$$I_{0max} = I_{0min} = \frac{E_{dc} - E_b}{R} \tag{8.32}$$

Thus, for given value of E_{dc}, E_b, R, α and τ, the maximum I_{0max} and minimum I_{0min} value of load current can be obtained from Eqs (8.30) and (8.31) respectively.

2. Steady-state Ripple From Fig. 8.14(b), it is observed that load-current i_o varies between the value I_{0max} and I_{0min}. Therefore, the ripple current $(I_{0max} - I_{0min})$ can be calculated from Eqs (8.30) and (8.31) as follows:

$$\therefore \quad (I_{0max} - I_{0min}) = \frac{E_{dc}}{R}\left[\frac{(1-e^{-T_{on}/\tau})}{(1-e^{-T/\tau})} - \frac{e^{T_{on}/\tau} - 1}{e^{T/\tau} - 1}\right]$$

$$= \frac{E_{dc}}{R}\left[\frac{(1-e^{-T_{on}/\tau})}{(1-e^{-T/\tau})} - \frac{(1-e^{-T_{on}/\tau})e^{T_{on}/\tau}}{(1-e^{-T/\tau})e^{T/\tau}}\right]$$

$$= \frac{E_{dc}}{R}\left[\frac{(1-e^{-T_{on}/\tau}) - (1-e^{-T_{on}/\tau})e^{(T_{on}-T)/\tau}}{(1-e^{-T/\tau})}\right]$$

$$= \frac{E_{dc}}{R}\left[\frac{(1-e^{-T_{on}/\tau})(1-e^{-(T-T_{on})/\tau})}{(1-e^{-T/\tau})}\right] \tag{8.33}$$

It is seen from Eq. (8.33) that, ripple-current is independent of back emf E_b.

Now, we know that $\alpha = T_{on}/T \quad \therefore\ T_{on} = \alpha \cdot T$ (8.34)

Also $\quad T - T_{on} = (1 - \alpha)T$ (8.35)

Substitute Eqs (8.34) and (8.35) into Eq. (8.33) gives

$$(I_{0max} - I_{0min}) = \frac{E_{dc}}{R}\left[\frac{(1-e^{-\alpha T/\tau})(1-e^{-(1-\alpha)T/\tau})}{(1-e^{-T/\tau})}\right]$$

$$\therefore \quad \text{Per unit (PU) ripple current} = \frac{(I_{0max} - I_{0min})}{E_{dc}/R}$$

$$= \frac{(1-e^{-\alpha T/\tau})(1-e^{-(1-\alpha)T/\tau})}{(1-e^{-T/\tau})} \tag{8.36}$$

For duty cycle $\alpha = 50\%$ (i.e. $\alpha = 0.5$) and $T/\tau = 5$, per unit ripple current become 0.848. Similarly, for $\alpha = 0.5$ and $T/\tau = 25$, per unit ripple current = 1. In this way, the variation of per unit ripple current as a function of duty cycle α and ratio T/τ can be plotted, as shown in Fig. 8.15. The PU ripple current has the maximum value when $\alpha = 0.5$. As the inductance L is increased, time-constant τ also increases and ratio T/τ reduces, therefore PU ripple current decreases, as shown in Fig. 8.15.

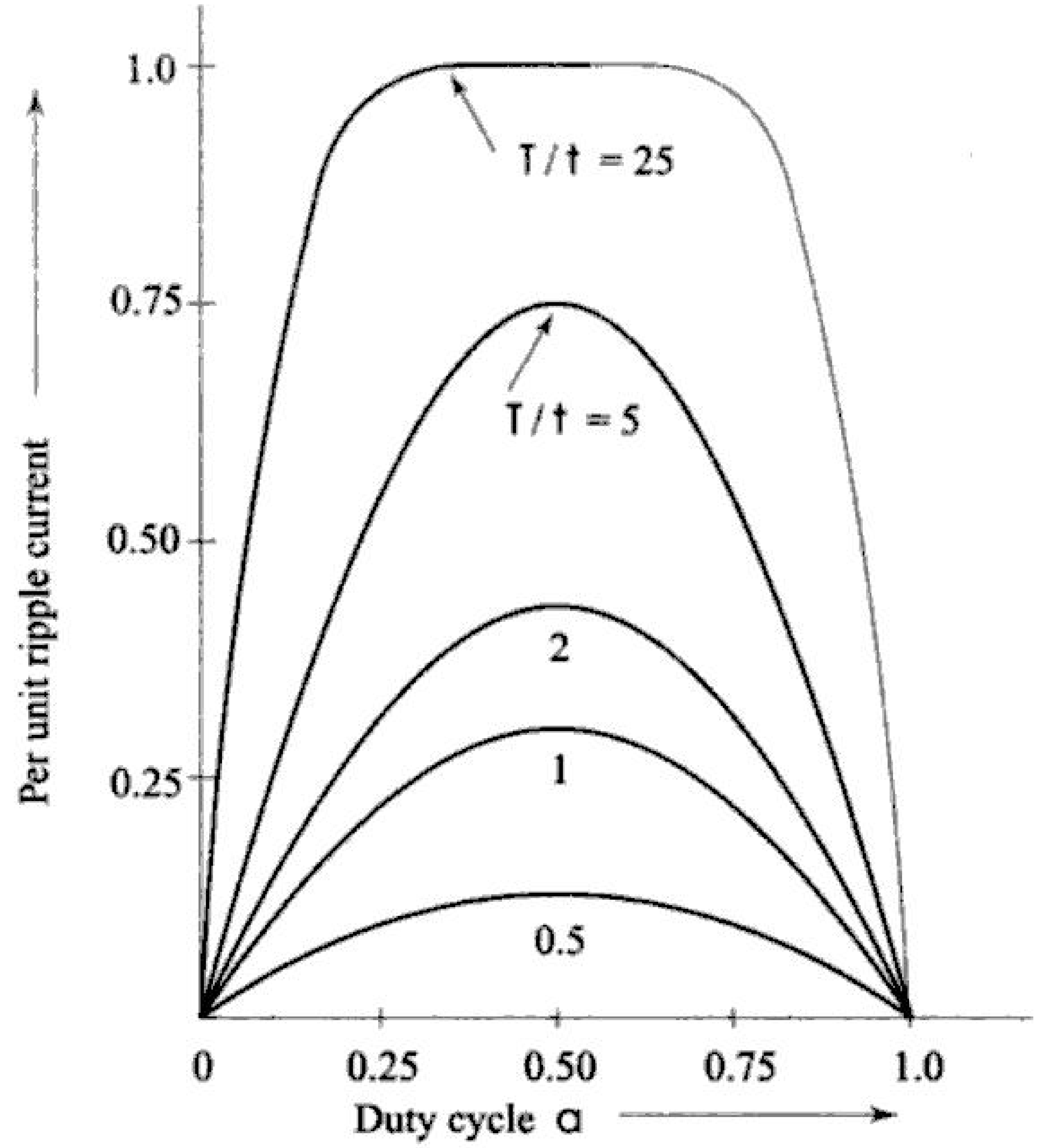

Fig. 8.15 *PU ripple current as a function of a and T/τ*

3. Fourier Analysis of Output Voltage Figure 8.14(b) illustrates the load voltage waveform e_0, for continuous load current. As shown, this voltage waveform is periodic in nature and is independent of load-circuit parameters. This voltage waveform may be described by the Fourier-series as

$$e_0 = E_0 + \sum_{n=1}^{\infty} C_n \tag{8.37}$$

where C_n = value of nth harmonic voltage

$$= \frac{2E_{dc}}{n\pi} \sin n\pi\alpha \sin (n\,\omega_0 t + \theta_n) \tag{8.38}$$

E_0 = average voltage of output voltage = αE_{dc}

$$\alpha = \text{duty cycle} = \frac{T_{on}}{T}, \text{ and } \theta_n = \tan^{-1}\frac{\sin 2\pi n\alpha}{1-\cos 2\pi n\alpha}$$

The average output voltage can be controlled by varying the duty-cycle α. From Eq. (8.38), it becomes clear that the amplitude of the harmonic voltage $\left(= \frac{2E_{dc}}{n\pi}\sin n\pi\alpha\right)$ depends on the order of harmonic n and also on the duty cycle α. The maximum value of the nth harmonic occurs when $\sin n\pi\alpha = 1$ and its value is

$$\frac{2E_{dc}}{n\pi} = \frac{0.6366\ E_{dc}}{n} \text{ V, and its RMS value is}$$

$$\frac{2E_{dc}}{\sqrt{2}n\pi} = \frac{0.45\ E_{dc}}{n} \text{ V} \tag{8.39}$$

Now, the harmonic current in the load is given by $i_n = \dfrac{C_n}{Z_n}$

where Z_n is the load impedance at harmonic frequency nf Hz and is given by

$$Z_n = \sqrt{R_L^2 + (n\omega_0 L)^2}$$

For negligible load resistance, R_L, $i_n = \dfrac{C_n}{n\omega_0 L}$ or $i_n \propto \dfrac{1}{n^2}$ (8.40)

Thus, the harmonic current decreases, as the order of the harmonic (n) increases. Another technique for measure of the harmonic content of a waveform, without calculating its harmonic components, is the a.c. ripple voltage E_r. It is defined as,

$$E_r = \sqrt{E_{rms}^2 - E_0^2} \tag{8.41}$$

In the above equation, E_{rms} and E_0 are the RMS and average value of the output-voltage respectively. Now, the RMS value of output voltage is given by

$$E_{rms} = \left[\alpha \cdot E_{dc}^2\right]^{1/2} = \sqrt{\alpha} \cdot E_{dc}$$

Therefore, Eq. (8.41) becomes

$$\therefore \qquad E_r = \sqrt{\alpha \cdot E_{dc}^2 - \alpha^2 E_{dc}^2} = E_{dc}\sqrt{\alpha - \alpha^2} \tag{8.42}$$

Ripple factor (RF) is defined as the ratio of a.c. ripple voltage to average voltage, and is given by

$$\text{RF} = \frac{E_r}{E_0}, \text{ or, RF} = \frac{E_{dc}\sqrt{\alpha - \alpha^2}}{\alpha \cdot E_{dc}} = \frac{E_{dc}\sqrt{\alpha}\sqrt{1-\alpha}}{\alpha \cdot E_{dc}}$$

$$= \frac{\sqrt{1-\alpha}}{\sqrt{\alpha}} = \sqrt{\frac{1-\alpha}{\alpha}} \tag{8.43}$$

4. Continuous Conduction Limit With pulse-width modulation control in class A chopper circuit, the "on" time (T_{on}) can be reduced by increasing "off" time T_{off}. At a particular low value of T_{on}, the off-time is large and current i_0 may go to zero. As discussed previously, that current i_0 in class A chopper cannot reverse, hence it stays at zero. Therefore, the limit of continuous conduction is reached when current I_{0min} given by Eq. (8.31) goes to zero.

The duty-cycle (α') and the limit of continuous conduction is given by Eq. (8.31) to zero. Therefore,

$$I_{0\min} = \frac{E_{dc}}{R}\left[\frac{e^{T_{on}/\tau}-1}{e^{T/\tau}-1}\right] - \frac{E_b}{R} = 0$$

or
$$\frac{e^{T_{on}/\tau}-1}{e^{T/\tau}-1} = \frac{E_b}{E_{dc}}$$

Let us define, $g = \dfrac{E_b}{E_{dc}} \quad \therefore \quad \dfrac{e^{T_{on}/\tau}-1}{e^{T/\tau}-1} = g$

or
$$(e^{T_{on}/\tau}-1) = g(e^{T/\tau}-1) \text{ or } e^{T_{on}/\tau} = 1 + g(e^{T/\tau}-1)$$

or
$$\alpha' = \frac{T_{on}}{T} = \left(\frac{\tau}{T}\right)\ln\left[1 + g(e^{T/\tau}-1)\right] \tag{8.44}$$

The load current is continuous if the actual-duty cycle (α) is more than the duty-cycle (α') obtained from Eq. (8.44), and, it becomes discontinuous if α is less than α'. The limit of continuous conduction for one-quadrant chopper can also be explained with the help of graph shown in Fig. 8.16. This graph shows the variation of duty cycle α' with respect to normalised back emf (g). The duty cycle α' can be calculated for various values of α' from 0 to 1 and by considering $\tau/T = 2$. For example, for $g = 0.4$,

$$\therefore \quad \alpha' = 2 \ln [1 + 0.4(e^{0.5} - 1)] = 0.4614$$

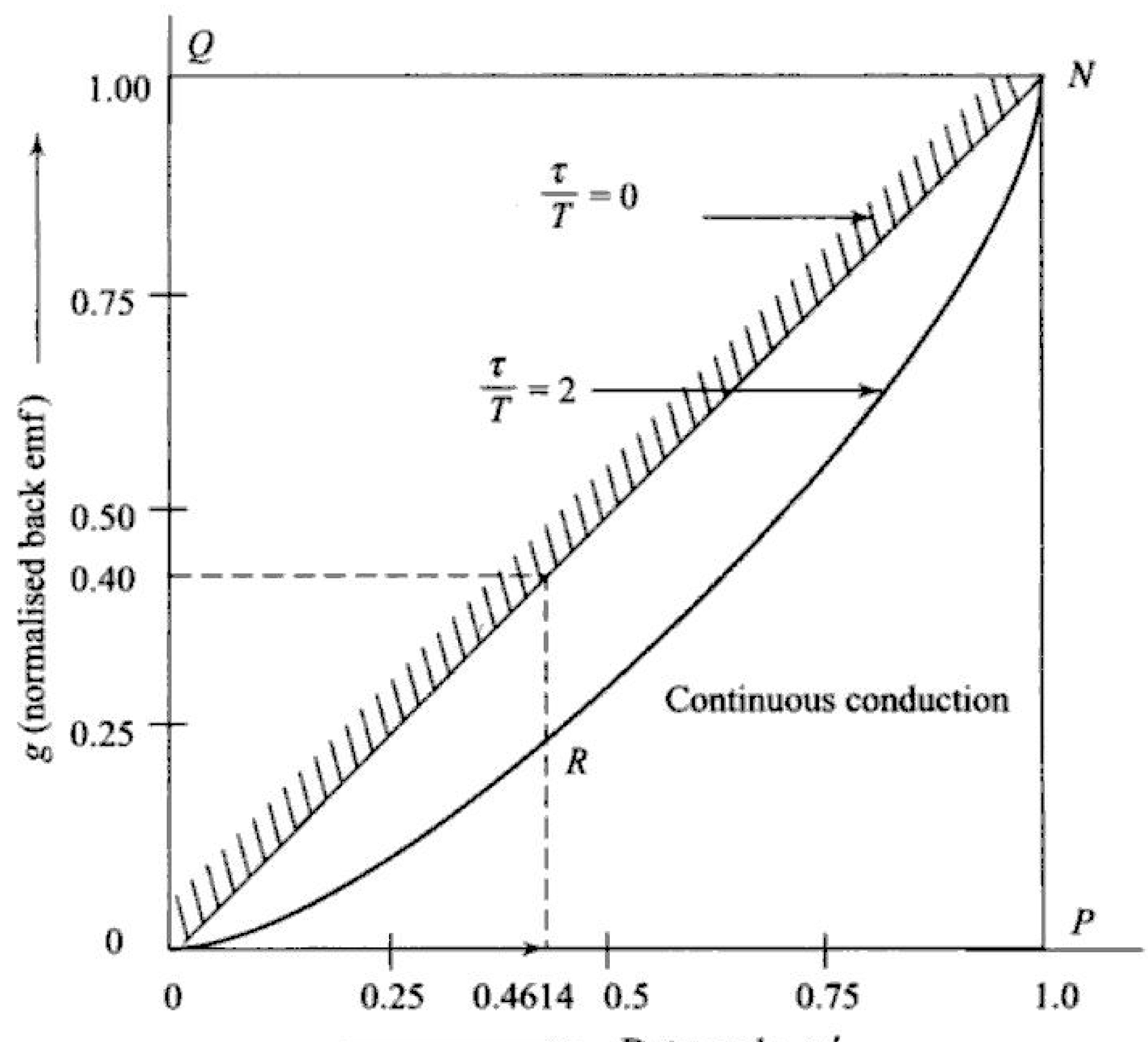

Fig. 8.16 *Continuous conduction limit*

As shown, for the value of $\tau/T = 2$, the region ORNPO represents the continuous conduction region and the other region ORNQO represents the discontinuous conduction region. Point marked R in Fig. 8.16 gives the limit of continuous conduction with duty-cycle $\alpha'(= 0.4614)$, for $\tau/T = 2$, and $g = 0.4$. For these values of $\frac{\tau}{T}$ and g, if actual duty cycle (α) is more than $\alpha'(= 0.4614)$, then the point will lie in the continuous conduction region, and if α is less than α', then the point will lie in the discontinuous conduction region. The straight line ON corresponds to $\tau/T = 0$ value.

5. *Expression for Average Load Current* Figure 8.17 shows the various voltage and current waveforms for one-quadrant chopper with R-L E_b load. Now, the average-load current (I_{0Av}) over a complete cycle can be obtained by adding the average value of the input current (or thyristor current I_{TAV}) and the average value of the freewheeling diode current (I_{DF}). Therefore, first we calculate the values of I_{TAV} and I_{DF}.

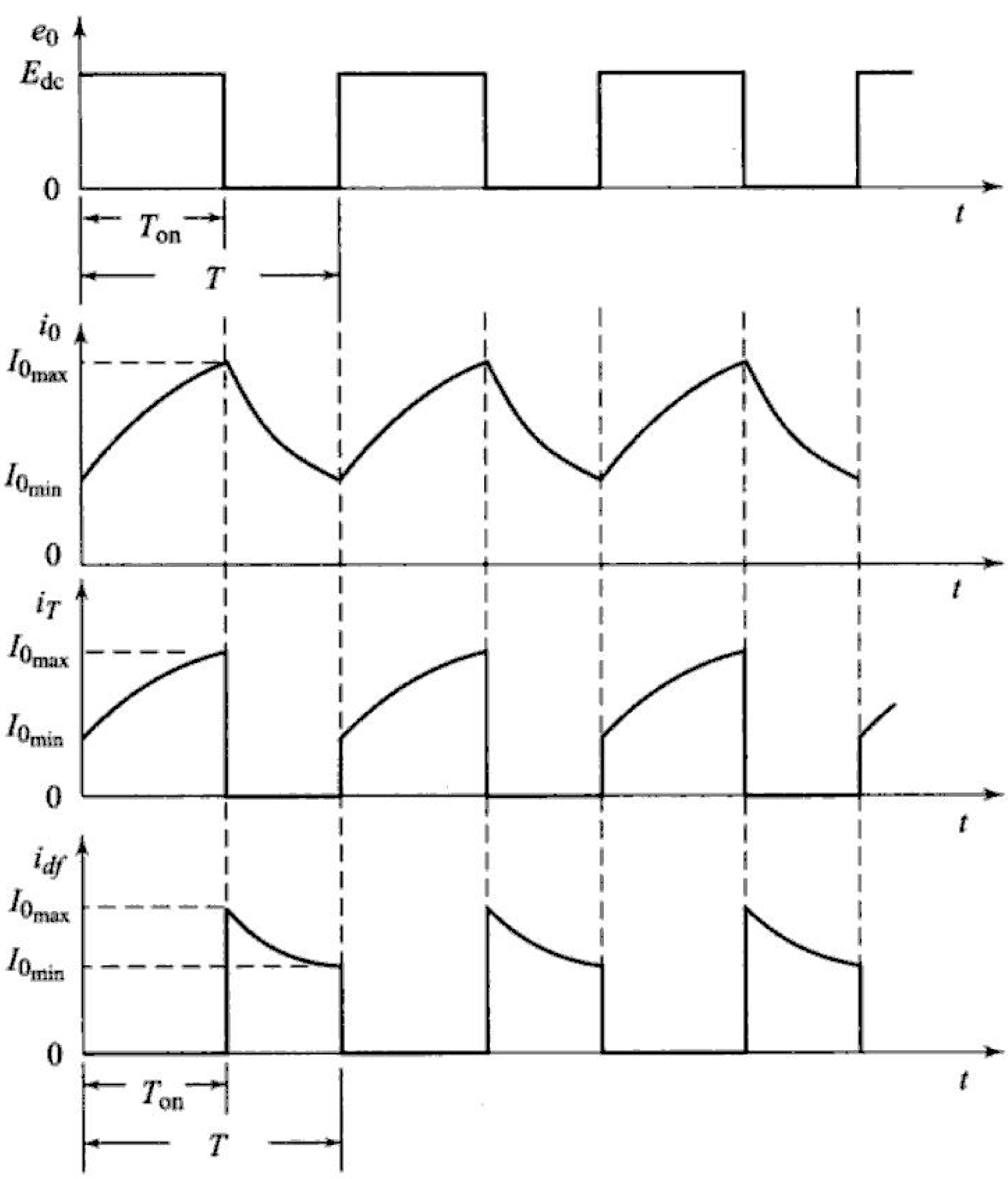

Fig. 8.17 *Voltage and current waveforms*

(a) Expression for I_{TAV} When chopper CH_1 is ON, the voltage equation for the chopper circuit of Fig. 8.13 by taking source or thyristor current i_t can be written as, $E_{dc} = Ri_T + L\frac{di_T}{dt} + E_b$ or, $(E_{dc} - E_b)dt = Ri_T\,dt + L\frac{di_T}{dt}\cdot dt$

Now, the average value of above equation is,

$$\frac{(E_{dc} - E_b)}{T}\int_0^{T_{on}} dt = R\cdot\frac{1}{T}\int_0^{T_{on}} i_t\cdot dt + \frac{1}{T}\int_0^{T_{on}} L\cdot di_T$$

$$\therefore \qquad (E_{dc} - E_b)\frac{T_{on}}{T} = R\cdot I_{TAV} + \frac{1}{T}\int_{I_{0min}}^{I_{0max}} L\,di_T$$

or,

$$(E_{dc} - E_b)\alpha = R\cdot I_{TAV} + \frac{L}{T}(I_{0\,max} - I_{0\,min})$$

or

$$\frac{(E_{dc} - E_b)\alpha}{R} - \frac{L}{RT}(I_{0max} - I_{0min}) = I_{TAV} \qquad (8.45)$$

(b) Expression for I_{DF} When chopper CH_1 is OFF, freewheeling diode D_f conducts and the voltage equation is given by

$$R\cdot i_{df} + L\frac{di_{df}}{dt} + E_b = 0$$

The average value of the above equation is given by

$$R\cdot\frac{1}{T}\int_{T_{on}}^{T} i_{df}\cdot dt + L\cdot\frac{1}{T}\int_{T_{on}}^{T}\frac{di_{df}\cdot dt}{dt} + E_b\cdot\frac{1}{T}\int_{T_{on}}^{T} dt = 0$$

or

$$R\cdot I_{DF} + \frac{L}{T}\int_{I_{0max}}^{I_{0min}} di_{df} = -E_b\cdot\left(\frac{T - T_{on}}{T}\right)$$

or

$$RI_{DF} + \frac{L}{T}(I_{0\,min} - I_{0\,max}) = -E_b(1 - \alpha)$$

$$\therefore \qquad I_{DF} = \frac{L}{T\cdot R}(I_{0\,max} - I_{0\,min}) - \frac{E_b}{R}(1 - \alpha) \qquad (8.46)$$

Now $\qquad I_{0AV} = I_{TAV} + I_{DF} \qquad (8.47)$

Substituting Eqs (8.45) and (8.46) in Eq. (8.47), we get

$$I_{0AV} = \frac{(E_{dc} - E_b)\alpha}{R} - \frac{L}{RT}(I_{0max} - I_{0min}) + \frac{L}{RT}(I_{0max} - I_{0min}) - \frac{E_b}{R}(1-\alpha)$$

$$= \frac{E_{dc}\cdot\alpha - E_b\cdot\alpha - E_b + E_b\cdot\alpha}{R} = \frac{\alpha\cdot E_{dc} - E_b}{R} \qquad (8.48)$$

Also, average output voltage can be expressed as,

$$E_0 = E_{dc}\cdot\frac{T_{on}}{T} = E_{dc}\cdot\alpha$$

Therefore, $\qquad I_{0AV} = \frac{\alpha E_{dc} - E_b}{R} = \frac{E_0 - E_b}{R} \qquad (8.49)$

Thus, the average output current can only be the average output voltage minus the back emf divided by the d.c. impedance of the load, i.e. its resistance.

SOLVED EXAMPLES

Example 8.7 For the ideal type A chopper circuit, following conditions are given: E_{dc} = 220 V, chopping frequency, f = 500 Hz; duty cycle α = 0.3 and R = 1 Ω; L = 3 mH; and E_b = 23 V. Compute the following quantities.

(i) Check whether the load current is continuous or not.
(ii) Average output current.
(iii) Maximum and minimum values of steady-state output current.
(iv) RMS values of first, second and third harmonics of load current.
(v) Average value of source current.
(vi) The input power, power absorbed by the back emf E_b and power loss in the resistor.
(vii) RMS value of output current using the result of (ii) and (iv).
(viii) The RMS value of load current using the results of (iv). Compare the result with that obtained in part (vii) above.

Solution:

(i) We know from the chopper theory, that the load current is continuous only when actual value of duty cycle α is greater than α'. Therefore, first calculate α'. From Eq. (8.44), we write, $\alpha' = \left(\frac{\tau}{T}\right)\ln\left[1+g\left(e^{T/\tau}-1\right)\right]$

where $\tau = L/R = \frac{3\times10^{-3}}{1} = 3\times10^{-3}$ s.

$$T=\frac{1}{f}=\frac{1}{500}=2000\ \mu\text{s}\cdot g=\frac{E_b}{E_{dc}}=\frac{23}{220}=0.105.$$

$$\therefore\ \alpha'=\left(\frac{3\times10^{-3}}{2000\times10^{-6}}\right)\ln\left[1+0.105\left(e^{0.67}-1\right)\right]=1.5\ln[1.100]\ \alpha'=0.143$$

Since $\alpha > \alpha'$, load current is continuous.

(ii) Average output current,

$$I_{0av}=\frac{\alpha\cdot E_{dc}-E_b}{R}=\frac{0.3\times220-23}{1}=43\text{ A}.$$

(iii) From Eq. (8.30), maximum value of output current is given by

$$I_{0max}=\frac{E_{dc}}{R}\left[\frac{1-e^{-T_{on}/\tau}}{1-e^{-T/\tau}}\right]-\frac{E_b}{R}$$

Now, $\alpha=\frac{T_{on}}{T}$ $0.3=\frac{T_{on}}{2000\times10^{-6}}$ $\therefore\ T_{on}=600\ \mu$s.

Also, $\frac{T_{on}}{\tau}=\frac{600\times10^{-6}}{3\times10^{-3}}=200\times10^{-3}$.

$$\therefore \quad I_{0\max} = \frac{220}{1}\left[\frac{1-e^{-200\times10^{-3}}}{1-e^{-0.67}}\right]-\frac{23}{1} \quad \therefore I_{0\max} = 58.64 \text{ A.}$$

From Eq. (8.31), $I_{0\min} = \frac{E_{dc}}{R}\left[\frac{e^{T_{on}/\tau}-1}{e^{T/\tau}-1}\right]-\frac{E_b}{R}$

$$= \frac{220}{1}\left[\frac{e^{0.2}-1}{e^{0.67}-1}\right]-\frac{23}{1} = 28.05 \text{ A.}$$

(iv) The RMS value of first harmonic voltage is given by

$$E_1 = \frac{2E_{dc}}{\sqrt{2}\pi}\sin\pi = \frac{2\times220}{\sqrt{2}\pi}\sin(\pi\times0.3) = 80.121 \text{ V.}$$

Now, $\quad Z_1 = \sqrt{R^2+(WL)^2} = \sqrt{(1)^2+(2\pi\times500\times3\times10^{-3})^2} = 9.48\ \Omega.$

$$\therefore \quad I_1 = \frac{E_1}{Z_1} = \frac{80.121}{9.48} = 8.452 \text{ A.}$$

Similarly, $\quad I_2 = \frac{2\times220}{2\sqrt{2}\pi}\sin 2\pi\alpha\frac{1}{\sqrt{1^2+\left(2\pi\times500\times2\times3\times10^{-3}\right)^2}} = 2.494 \text{ A}$

$$I_3 = \frac{2\times220}{3\sqrt{2}\pi}\sin(162^\circ)\frac{1}{\sqrt{1^2+\left(2\pi\times3\times500\times3\times10^{-3}\right)^2}} = 0.624 \text{ A.}$$

(v) From Eq. (8.45), the average value of source current is given by

$$I_{TAV} = \frac{(E_{dc}-E_b)\alpha}{R}-\frac{L}{RT}\left(I_{0\max}-I_{0\min}\right)$$

$$= \frac{(220-23)0.3}{1}-\frac{3\times10^{-3}}{1\times2000\times10^{-6}}(58.64-28.05)$$

$$= 59.1-1.5\,(30.59) = 13.215$$

(vi) Input power = E_{dc} × average source current = 220 × 13.215 = 2907.3 W

Power absorbed by load emf = E_b × average load current = 23 × 43 = 989 W.

Power loss in resistor R = Input power – power absorbed by load emf

$$= 2907.3 - 989 = 1918.3 \text{ W.}$$

(vii) $I_{rms} = \sqrt{I_{0av}^2+I_1^2+I_2^2+I_3^2} = \sqrt{(43)^2+(8.452)^2+(2.494)^2+(0.624)^2}$

$$= 1927.05 \text{ A} = 43.89 \text{ A.}$$

(viii) Power loss in resistor I^2R = 1918.3 W

$$\therefore \quad I_{rms} = \sqrt{\frac{1918.3}{1}} = 43.798 \text{ A}$$

The value of I_{rms} in both parts is nearly the same.

Example 8.8 An ideal chopper operating at a chopping period of 2 ms supplies a load of 4 Ω having an inductance of 8 mH from a 80 V battery. Assuming the load is shunted by a perfect commutating diode, and battery to be lossless,

(a) compute the load current waveform $f_{on}\dfrac{T_{on}}{T_{off}}$ values of

(ii) 1/1 (ii) 4/1 (iii) 1/4.

(b) Also, calculate the mean value of load voltage and current at each setting.

Solution:

(a) During the on-period, the battery is switched to a series R_L load, having an initial current I_{0min}.
During the off-period, the load current decays in the R–L load through the diode, having an initial value of I_{0max}. Fig. Ex. 8.8 shows the waveforms for each setting.

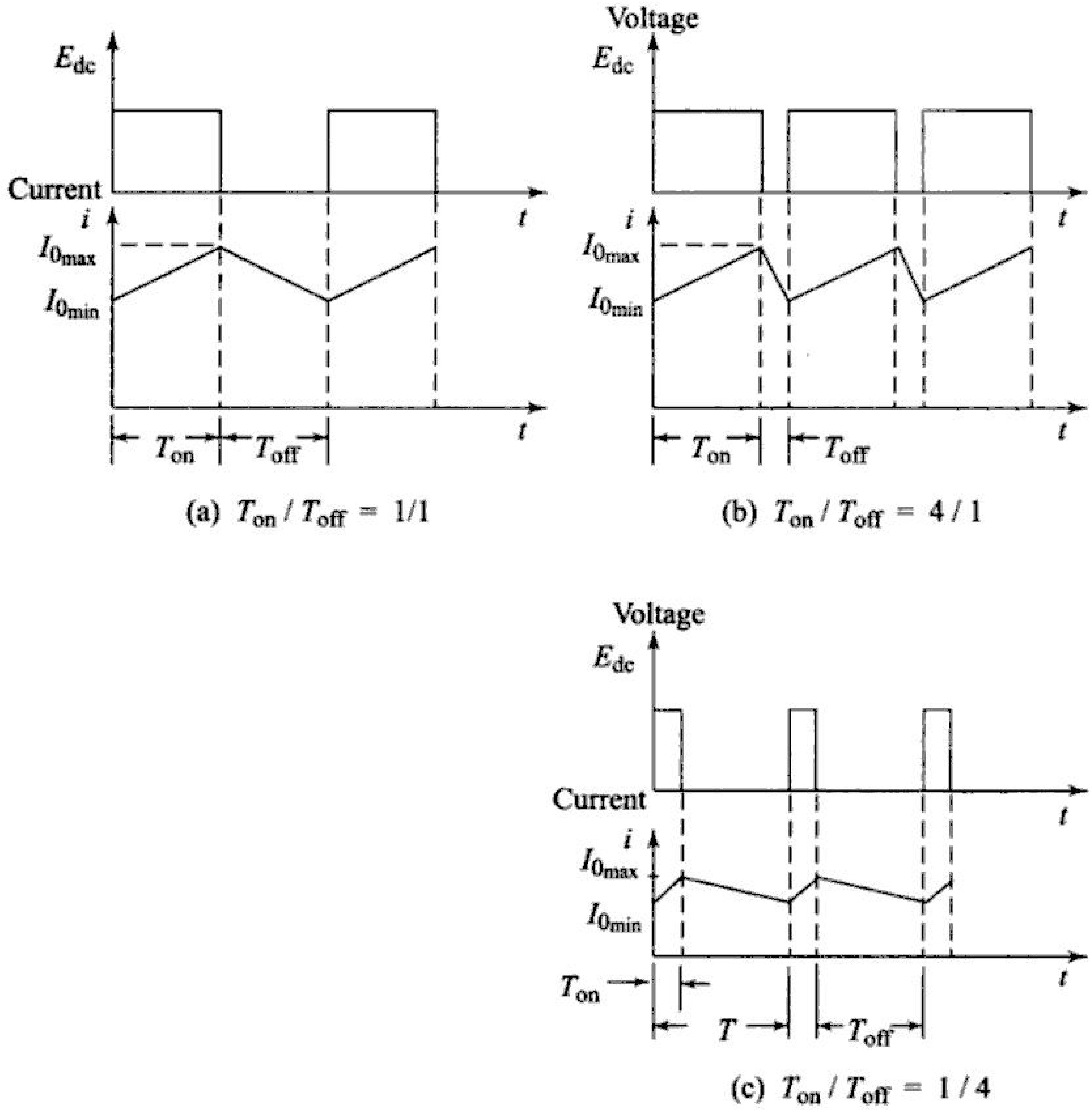

Fig. Ex. 8.8 *Three different waveforms*

When chopper is ON, $i = I_{0\,min} \cdot \left(\dfrac{E_{dc}}{R} - I_{0\,min}\right)\left(1 - e^{-T_{on}/\tau}\right) = I_{0max}$ (a)

When chopper is OFF, $i = I_{0max}\, e^{-T_{off}/\tau} = I_{0min}$ (b)

From Eqs (a) and (b), we can write $I_{0\max} = \dfrac{E_{dc}}{R}\left(\dfrac{1-e^{-T_{on}/\tau}}{1-e^{-T/\tau}}\right)$ (c)

and $I_{0\,min} = I_{0\,max}\, e^{-T_{off}/\tau}$ (d)

Now, $\dfrac{E_{dc}}{R} = \dfrac{80}{4} = 20$ A. $\tau = L/R = \dfrac{0.008}{4} = 0.002$ s. $T = 2$ ms. $= 0.002$ s

(i) When $\dfrac{T_{on}}{T_{off}} = 1/1$,

$$T_{on} = T_{off} = 1 \text{ ms} = 0.001 \text{ s.} \quad \therefore I_{0\,max} = 20\left(\frac{1-e^{-\frac{0.001}{0.002}}}{1-e^{-0.002/0.002}}\right) = 12.45 \text{ A.}$$

and $I_{0\,min} = 12.45\, e^{-0.001/0.002} = 7.55$ A.

(ii) When $\dfrac{T_{on}}{T_{off}} = 4/1, T_{on} = 4\,T_{off}$

$\therefore$ $T_{on} = 0.0016$ s, and $T_{off} = 0.0004$ s

$$\therefore \quad I_{0\,max} = 20\left(\frac{1-e^{-\frac{0.0016}{0.002}}}{1-e^{-0.002/0.002}}\right) = 17.42 \text{ A.}$$

$I_{0\,min} = 17.42\,(e^{-0.004/0.002}) = 2.36$ A

(iii) When $\dfrac{T_{on}}{T_{off}} = 1/4, T_{off} = 0.001\,6$ s, $T_{on} = 0.0004$ s.

$$\therefore \quad I_{0\,max} = 20\left(\frac{1-e^{-\frac{0.004}{0.002}}}{1-e^{-0.002/0.002}}\right) = 5.73 \text{ A.}$$

$I_{0\,min} = 5.73\,(e^{-0016/0.002}) = 2.57$ A.

(b) Now, average load voltages and currents are given by

(i) $E_0 = E_{dc}\left(\dfrac{T_{on}}{T}\right) = 80\left(\dfrac{1}{2}\right) = 40$ V, $I_{0av} = \dfrac{E_0}{R} = \dfrac{40}{4} = 10$ A

(ii) $E_0 = 80(4/5) = 64$ V, $I_{0av} = \dfrac{64}{4} = 16$ A

(iii) $E_0 = 80\,(1/5) = 16$ V, $I_{0av} = \dfrac{16}{4} = 4$ A.

Example 8.9 An R–L E_b type load is operating in a chopper circuit from a 400 volts d.c. source. For the load, L = 0.05 H and R = 0. For a duty cycle of 0.3, find the chopping frequency to limit the amplitude of load current excursion to 8 A.

Solution: The related circuit diagram is shown in Fig. Ex. 8.9.

The average output voltage is given by, $E_0 = \alpha \cdot E_{dc}$

As the average value of voltage drop across inductance L is zero,

$$E_b = E_0 = \alpha \cdot E_{dc} = 0.3 \times 400 = 120\text{ V}$$

During the on-period of the chopper T_{on}, the difference in source voltage E_{dc} and load back emf E_b, i.e. $(E_{dc} - E_b)$, appears across L, as shown in Fig. Ex. 8.9.

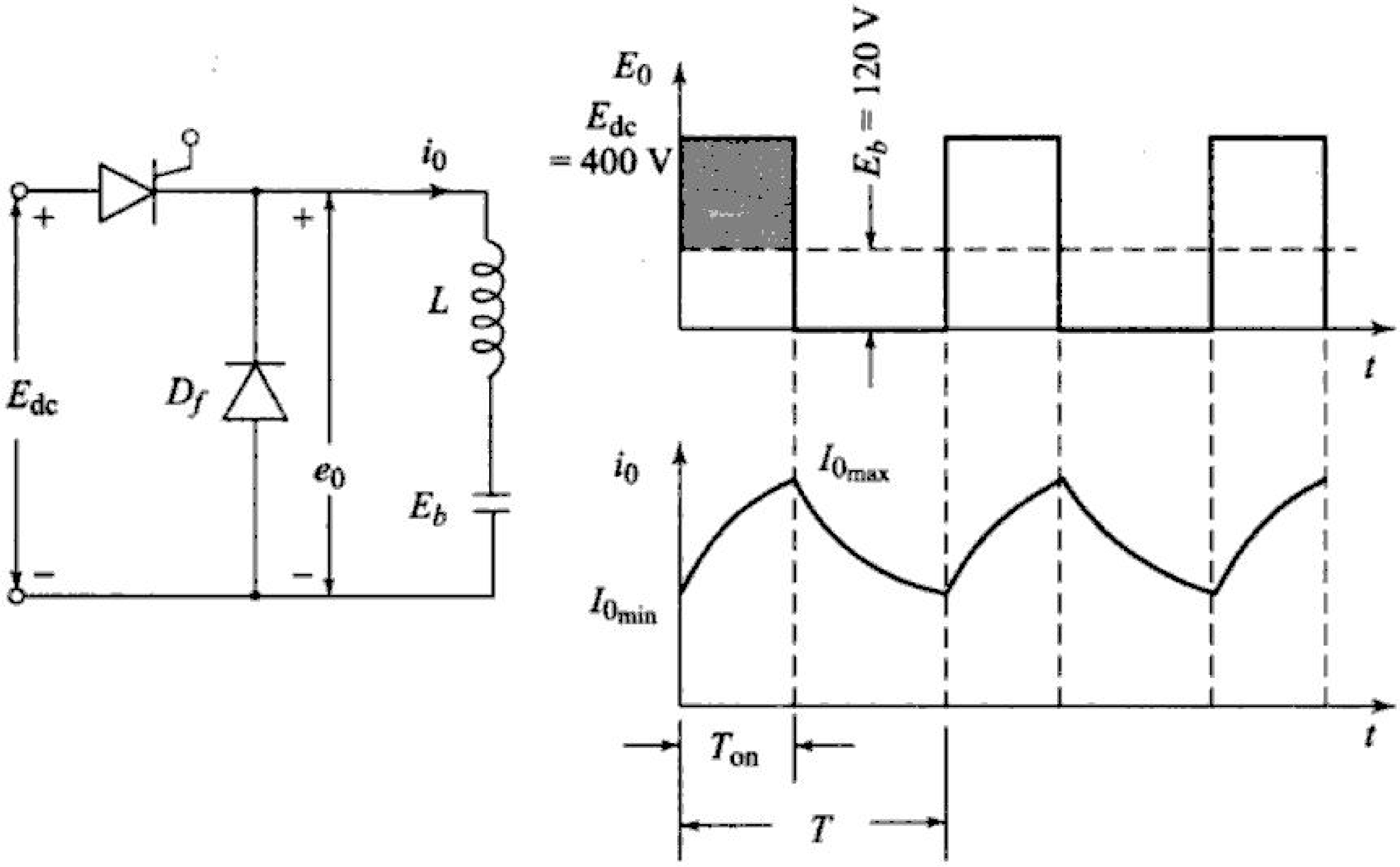

Fig. Ex. 8.9 *Chopper circuit and waveforms*

$\therefore$ During T_{on}, volt–time area applied to inductance = (400 – 120) T_{on} = 280 T_{on} $V - s$ (a)

As shown in Fig. Ex. 8.9, the current through inductance L rises from $I_{0\,min}$ to $I_{0\,max}$. From this, volt-time area across L during current change is given by

$$\int_0^{T_{on}} E_L dt = \int_0^{T_{on}} L\frac{di_0}{dt}dt = \int_{T_{0max}}^{T_{0max}} L \cdot di = L\,(I_{0\,max} - I_{0\,min}) = L\,\Delta I_0 \qquad \text{(b)}$$

During T_{on}, the volt–time areas given by Eqs (a) and (b) must be equal.

$$\therefore \qquad 280\,T_{on} = L\,\Delta I_0$$

$$\therefore \quad T_{on} = \frac{0.05 \times 8}{280} = 1.43\text{ ms}$$

$$\therefore \text{ Chopping frequency, } f = 1/T = \frac{\alpha}{T_{on}} = \frac{0 \cdot 3}{1.43 \times 10^{-3}} = 209.79\text{ Hz.}$$

Example 8.10 A simple d.c. chopper is operating at a frequency of 2 kHz from a 96 V d.c. source to supply a load resistance of 8 Ω. The load time constant is 6 ms. If the average load voltage is 57.6 V, find the T_{on} period of the chopper, the average load current, the magnitude of the ripple current and its RMS value.

Solution: Chopping period, $T = 1/f = \dfrac{1}{2000} = 0.5$ ms.

Given load time constant = 6 ms

$\therefore$ Load time constant = 12 T, therefore treat as a linear current variation.

(i) Now, $E_0 = E_{dc} \cdot \dfrac{T_{on}}{T} \quad \therefore \dfrac{57.6}{96} = \dfrac{T_{on}}{0.5 \times 10^{-3}} \quad \therefore T_{on} = 0.3$ ms.

(ii) The RMS value of the load voltage is given by

$$F_{L_{RMS}} = E_{dc}\left(\frac{T_{on}}{T}\right)^{1/2} = 96 \times \left(\frac{0.3}{0.5}\right)^{1/2} = 74.36 \text{ V}$$

(iii) Therefore, the average load current $= \dfrac{E_0}{R} = \dfrac{57.6}{8} = 7.2$ A

(iv) Now, current ripple $= \Delta_i = \dfrac{(E_{dc} - E_0)\Delta t}{L}$

Load time constant $\tau = L/R, \quad \therefore L = 6 \times 10^{-3} \times 8 = 48$ mH.

$$\therefore \qquad \Delta_i = \frac{(96 - 57.6) \times 0.3 \times 10^{-3}}{48 \times 10^{-3}} = 0.24 \text{ A}$$

(v) From Example (8.8), we have

$$I_{0\,max} = \frac{E_{dc}}{R}\left(\frac{1 - e^{-T_{on}/\tau}}{1 - e^{-T/\tau}}\right) = \frac{96}{8}\left(\frac{1 - e^{-\frac{0.3\text{ ms}}{6\text{ms}}}}{1 - e^{-0.5/6\text{ ms}}}\right) = 7.32 \text{ A.}$$

Similarly,

$$I_{0\,min} = I_{0\,max}\, e^{-T_{off}/\tau} = 7.32\, e^{-0.2\text{ ms}/6\text{ ms}} = 7.08 \text{ A}$$

The RMS value of the ripple current is given by

$$I_{r,\,RMS} = \frac{(I_{0\,max} - I_{0\,min})}{2\sqrt{3}} = \frac{(7.32 - 7.08)}{2\sqrt{3}} = 0.0693 \text{ A.}$$

Example 8.11 A d.c. motor with armature resistance $R_a = 0.4$ Ω and armature inductance $t_a = 8$ mH, is having a back emf of 80V while carrying a current of 10 A. The motor is connected to a d.c. source of 180 V by the main SCR of the chopper. If the SCR turns off after 1 ms, compute the current in the motor

(i) at the instant the thyristor turns off, and
(ii) 8 ms after SCR turns off.

Solution: The differential equation with the given chopper conditions is given by

$$E_{dc} = R_a \cdot i_a + L_a \frac{di_a}{dt} + E_b, \text{ Now, } \tau = L/R = 8 \text{ mH}/0.4 = 20 \text{ ms.}$$

The solution of the above equation is given by

$$i(t) = \frac{E_{dc} - E_b}{R_a}\left(1 - e^{-t/\tau}\right) + I_0 \cdot e^{-t/\tau} = \frac{180 - 80}{0.4}\left(1 - e^{-t/20 \times 10^{-3}}\right) + 10(e^{-t/20 \times 10^{-3}})$$

$$= 250\left(1 - e^{-t/20 \times 10^{-3}}\right) + 10\, e^{-t/20 \times 10^{-3}}$$

(i) At $t = 1 \times 10^{-3}$ s, $I(t) = 250\left(1 - e^{-1 \times 10^{-3}/20 \times 10^{-3}}\right) + 10\, e^{-1/10^{-3}/20 \times 10^{-3}}$

$$I(t) = 12.193 + 9.512\, I(t) = 21.705 \text{ A.}$$

(ii) Current is freewheeled through the load for the period of 9 ms.

$$\therefore \quad i_f = I(t) \cdot e^{-t/\tau} = i_f = 21.705 e^{-9 \times 10^{-3}/20 \times 10^{-3}} = 13.84 \text{ A}$$

Example 8.12 A DC chopper operates on 230 V dc and frequency of 400 Hz, feeds an R-L load. Determine the ON time of the chopper for output of 150 V.

Solution:

Given: $E_{dc} = 230$ V, $f = 400$ Hz, $E_0 = 150$ V

We have, $E_0 = \alpha \cdot E_{dc} \quad \therefore 150 = \alpha \cdot 230, \quad \therefore \alpha = 0.65$

Time period of output voltage wave is given by

$$T = 1/F = 1/400 = 2.5 \times 10^{-3} \text{ sec}$$

Now, $\alpha = \dfrac{T_{on}}{T}, \quad \therefore t_{on} = \alpha \cdot T = 0.65\,(2.5 \times 10^{-3})$

$\therefore$ On-time of chopper, $t_{on} = 1.6305$ m sec

Example 8.13 A single-quadrant type A chopper is operated with the following specifications:

(i) ideal battery of 220 V (ii) on-time $t_{on} = 1$ msec (iii) off-time $t_{off} = 1.5$ msec

Determine: (a) Average and RMS output voltages (b) Ripple and form factor

Solution:

Time period $T = t_{on} + t_{off} = (1 + 1.5) = 2.5$ msec, Duty cycle $\alpha = \dfrac{T_{on}}{T} = \dfrac{1}{2.5} = 0.4$

(a) Average output voltage, $E_0 = \alpha \cdot E_{dc} = (0.4)(220) = 88$ V.

$$\text{RMS output voltage } E_{0rms} = \sqrt{\alpha} \cdot E_{dc} = \sqrt{0.4}\ (220) = 139.14 \text{ V}$$

(b) Form-factor (FF) $= \dfrac{\text{RMS Value}}{\text{Average Value}} = \dfrac{\sqrt{\alpha} \cdot E_{dc}}{\alpha \cdot E_{dc}} = \dfrac{1}{\sqrt{\alpha}} = \dfrac{1}{\sqrt{0.4}} = 1.58$

Ripple factor (RF) $= \sqrt{(FF)^2 - 1} = \sqrt{\dfrac{1}{\alpha} - 1} = \sqrt{\dfrac{1 - \alpha}{\alpha}} = \sqrt{\dfrac{1 - 0.4}{0.4}} = 1.23$

8.5.2 Second-Quadrant or Class B Chopper [Step-up Chopper with R–L Load]

Figure 8.18(a) shows the basic power circuit of the second-quadrant chopper. The term 'second-quadrant' signifies that circuit parameters E_0 and I_0 occur only in the second-quadrant of E_0–I_0 diagrams. Figure 8.18(b) shows the chopper with R–L load.

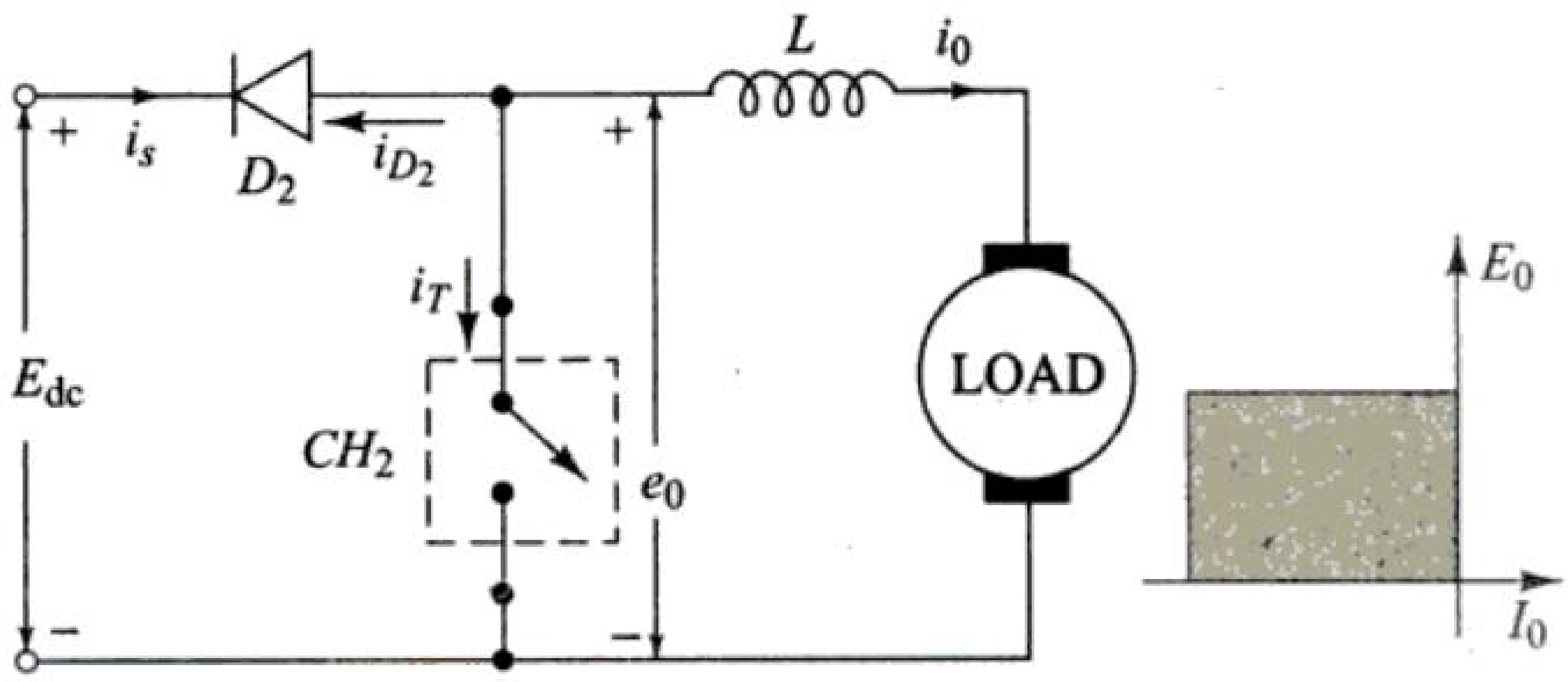

Fig. 8.18(a) *Type-B chopper circuit and E_0–I_0 characteristic*

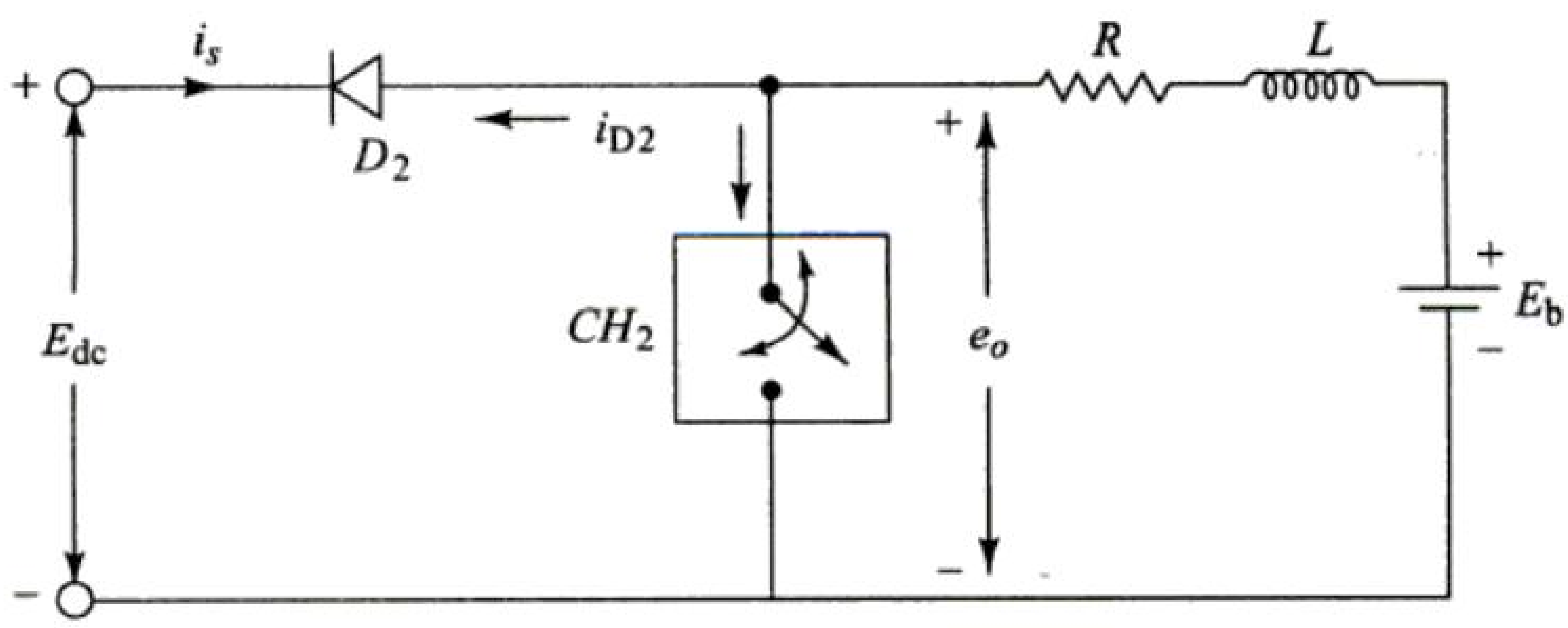

Fig. 8.18(b) *Class B with R–L load*

If the chopper is turned ON and OFF during regular intervals of period T, emf E_b stores energy in inductance L whenever chopper is conducting and part of that stored energy is delivered to source E_{dc} by current through diode D_2 when CH_2 is commutated. Therefore, when the chopper is ON, $e_0 = 0$ and when chopper is OFF and diode D_2 conducting, $e_0 = E_{dc}$. When the chopper is OFF, load current i_0 has the direction opposite to that shown in Fig. 8.18. Hence, average load voltage E_0 is positive and average load current I_0 is negative. It means that, power flow takes place from load to source. Since active load is capable of providing continuous power output, the reversal power-flow is possible in this type of chopper configuration. Because of power flow from load of lower-voltage e_0 to the source of higher-voltage E_{dc}, this configuration is also referred to as step-up chopper. This configuration is used for regenerative breaking of d.c. motors. A typical application is the chopper drive of a subway-train.

The related circuit waveforms are shown in Fig. 8.19. Here, the interval during which diode D_2 conducts is designated as T_{off}. Hence, the cycle of operation starts at $t = 0$ in Fig. 8.19, at the instant when chopper CH_2 is commutated.

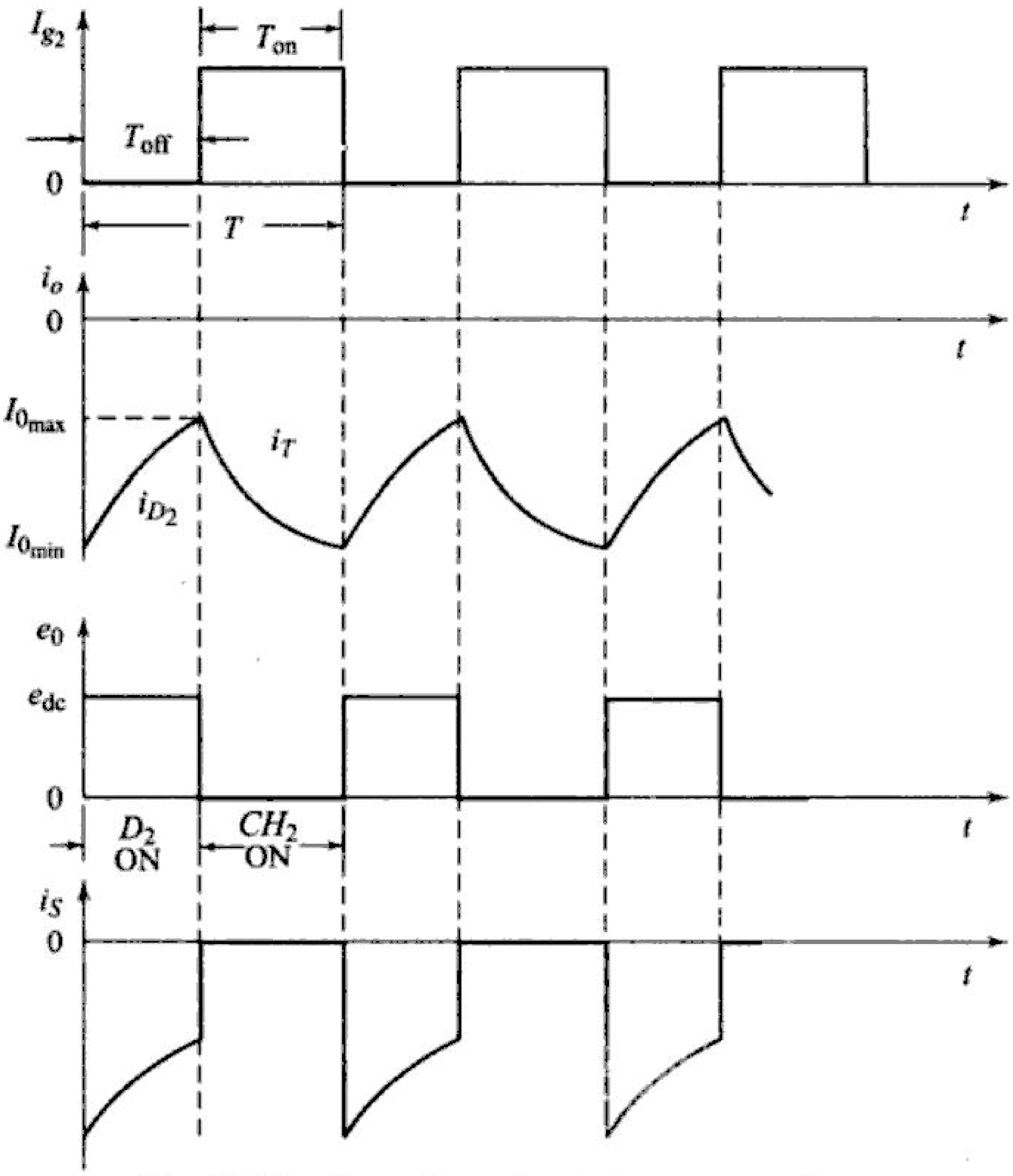

Fig. 8.19 *Second-quadrant chopper waveform*

As shown in Fig. 8.19, let i_0 has value I_{0min} at $t = 0$. For interval $0 < t < T_{off}$, diode D_2 conducts and $e_0 = E_{dc}$. During this interval, the voltage equation becomes

$$L\frac{di_0}{dt} + Ri_0 = E_{dc} - E_b \tag{8.50}$$

or

$$\frac{di_0}{dt} + \frac{R}{L}i_0 = \frac{E_{dc} - E_b}{L} \tag{8.51}$$

The solution of the above Eq. (8.51) for the stated initial conditions is

$$I_{0(t)} = \left(\frac{E_{dc} - E_b}{R}\right)\left(1 - e^{-t/\tau}\right) + I_{0\min} \cdot e^{-t/\tau} \tag{8.52}$$

At $t = T_{off}$, I_0 has reached a magnitude I_{0max}, where $I_{0min} < I_{0max} < 0$. Thus,

from Eq. (8.52), $$I_{0max} = \left(\frac{E_{dc} - E_b}{R}\right)\left(1 - e^{-T_{off}/\tau}\right) + I_{0\min} \cdot e^{-T_{on}/\tau} \tag{8.53}$$

At $t = T_{off}$, chopper CH_2 is turned-on and at T_{off}, e_0 becomes zero and $i_0 = I_{0max}$. During the interval $T_{off} < t < T$, voltage equation becomes

$$\frac{di_0}{dt'} + \frac{R \cdot i_0}{L} = \frac{-E_b}{L} \tag{8.54}$$

where $$t' = t - T_{off} \tag{8.55}$$

The solution to Eq. (8.54) for the stated initial conditions is

$$I_0 = \frac{-E_b}{R}(1 - e^{-t'/\tau}) + I_{0\max} e^{-t'/\tau} \tag{8.56}$$

Thus, at the end of the cycle, when $t = T$, or $t' = T - T_{off}$, i_0 must have returned to its initial value $I_{0\min}$. From Eq. (8.56),

$$I_{0\min} = \frac{-Eb}{R}\left(1 - e^{-(T-T_{off})/\tau}\right) + I_{0\max}\, e^{-(T-T_{off})/\tau} \tag{8.57}$$

Equations (8.53) and (8.57) are idential to Eqs (8.26) and (8.28), therefore, they may be solved simultaneously to yield Eqs (8.30) and (8.31). Fourier analysis of the waveforms of currents i_0 and i_T may be carried out as for Class A operation.

8.5.3 Two-Quadrant Type A Chopper (or Class C Chopper)

Though switching from Class A to a Class B configuration is a satisfactory method to obtaining regenerative breaking for some applications but in applications like machine-tool drives, a very smooth transition from driving to breaking is essential. This required drive is provided by connecting Type A and Type B choppers in parallel, as shown in Fig. 8.20(a). Figure 8.20(b) shows class C with R–L Load. The circuit shown, modifies first-quadrant operation and converts it to second-quadrant operation. For first quadrant operation, CH_1 and D_1 perform the functions and if the average load current I_0 is high enough, CH_2 and D_2 do not conduct, even though CH_2 receives a gating signal. For second quadrant operation, CH_2 and D_2 perform the functions and if the average load current I_0 has a sufficiently large negative value, CH_1 and D_1 do not conduct, even though CH_1 receives a gating signal. Figure 8.21 shows the gate current, load voltage and supply current waveforms.

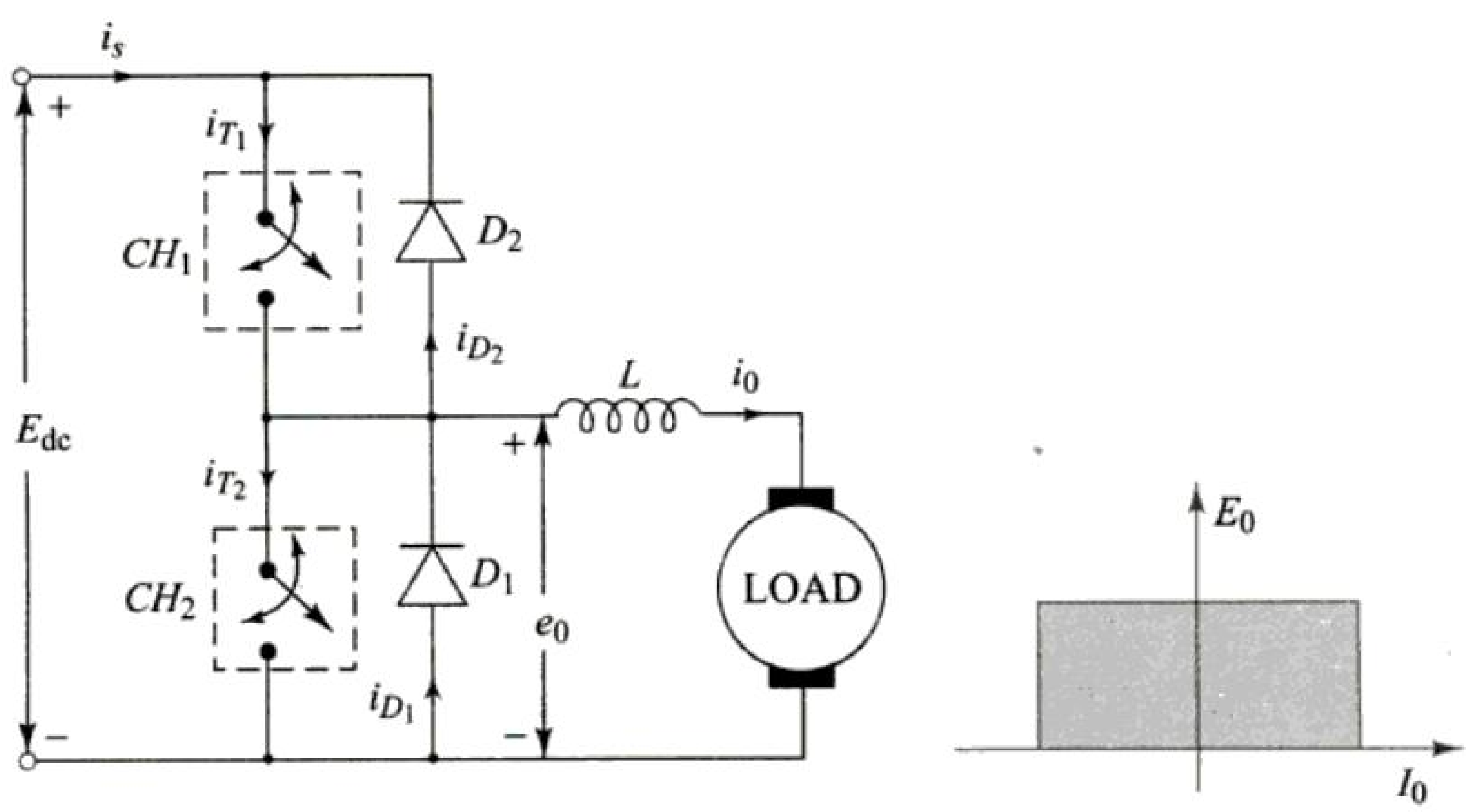

Fig. 8.20(a) *Type-C chopper circuit and $E_0 - I_0$ characteristics*

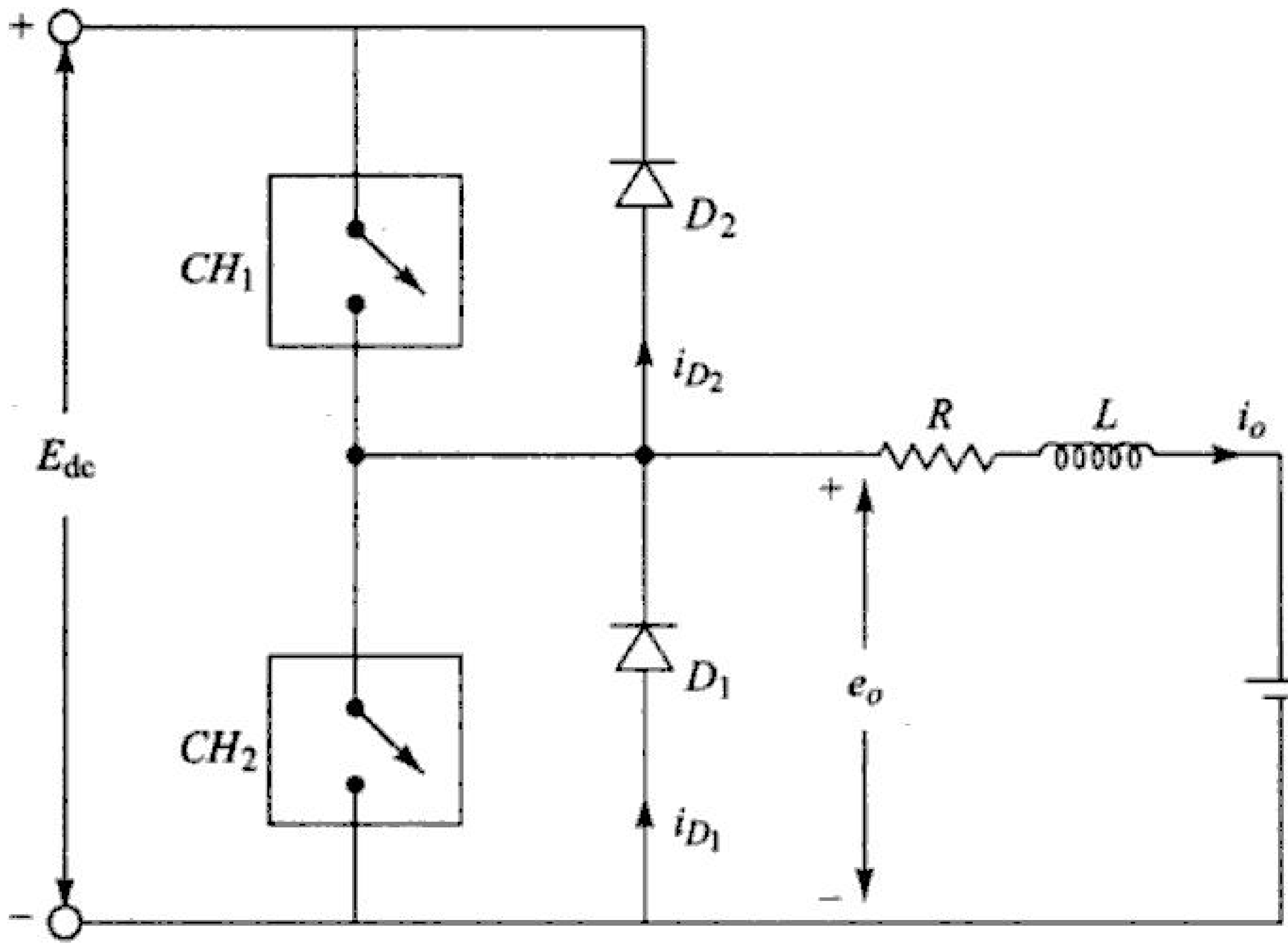

Fig. 8.20(b) *Class-C chopper with R-L load*

Initially, when both the choppers are OFF, both the diodes D_1 and D_2 become also OFF, and therefore, load is isolated from the supply. As shown in Fig. 8.21, at point P, chopper CH_1 is triggered and it starts to conduct. The load current i_0 is positive and the load receives power from the supply. Therefore, the output voltage $e_0 = E_{dc}$ when chopper CH_1 or diode D_2 conducts. At point Q, chopper CH_1 is turned OFF and inductance L forces the load current to flow through diode D_1 till the value of $L\dfrac{di_s}{dt}$ becomes equal to the back emf (E_b) of the load and the load-current i_0 becomes zero. Therefore, diode D_1 conducts from point Q to point R, as shown in Fig. 8.21. At this point R, if the gate signal to chopper CH_2 is available the back emf (E_b) of the motor forces current in the opposite direction through L and CH_2. This continues until CH_2 is turned-OFF and CH_1 is turned-ON. Now, when CH_2 is turned-OFF, the energy of the inductance forces current through diode D_2 to the supply. The input current becomes negative. During this period, CH_1 cannot conduct due to reverse bias but comes into conduction when the input current reduces to zero, provided the gate signal is available to CH_1 and both the load and input current becomes positive.

Hence, it becomes clear that load voltage $e_0 = 0$ if chopper CH_2 or diode D_1 conducts, and $e_0 = E_{dc}$ if chopper CH_1 or diode D_2 conducts. Therefore, average load voltage E_0 is positive. However, load current i_0 have both positive and negative directions. It is positive if CH_1 is ON or D_1 conducts and negative if CH_2 is ON or D_2 conducts. Since average load voltage E_0 is positive and average load current I_0 is reversible, power flow is reversible. It is also clear that both thyristors may not be turned-ON simultaneously because that would short-circuit source E_{dc}. They are turned-ON alternately, as shown by the gating signal waveforms in Fig. 8.21. This chopper configuration is, therefore, used for both motoring and regenerative breaking of d.c. motor.

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The circuit operation of a Type D chopper can be considered into two different modes of operation; one mode for which $T_{on} > T/2$ and the two gating signals overlap, the other mode for which $T_{on} < T/2$ and only one chopper is turned-ON at any instant or none of the chopper is turned-ON. Here, the load current is assumed to be continuous for circuit analysis.

(a) Mode 1 Operation: $T_{on} > T/2$ When both the choppers are turned-ON, the current flows through the path, $E_{dc} - CH_1 - \text{load} - CH_2 - E_{dc}$. Therefore, both the diodes D_1 and D_2 are turned-OFF. The supply voltage E_{dc} is applied to the load circuit and load current i_0 increases.

When only one chopper is turned-ON, that chopper and one of the diodes short-circuit the load branch and provide a path in which some of the energy stored in inductance L may be dissipated in maintaining a decreasing load current i_0.

Circuit analysis: The associated waveforms for this mode of operation is shown in Fig. 8.23. For steady-state operation, it is necessary in this mode that $E_{dc} > E_b$. Since, one cycle of the load-circuit variables takes place in time $T/2$, two-durations are to be considered.

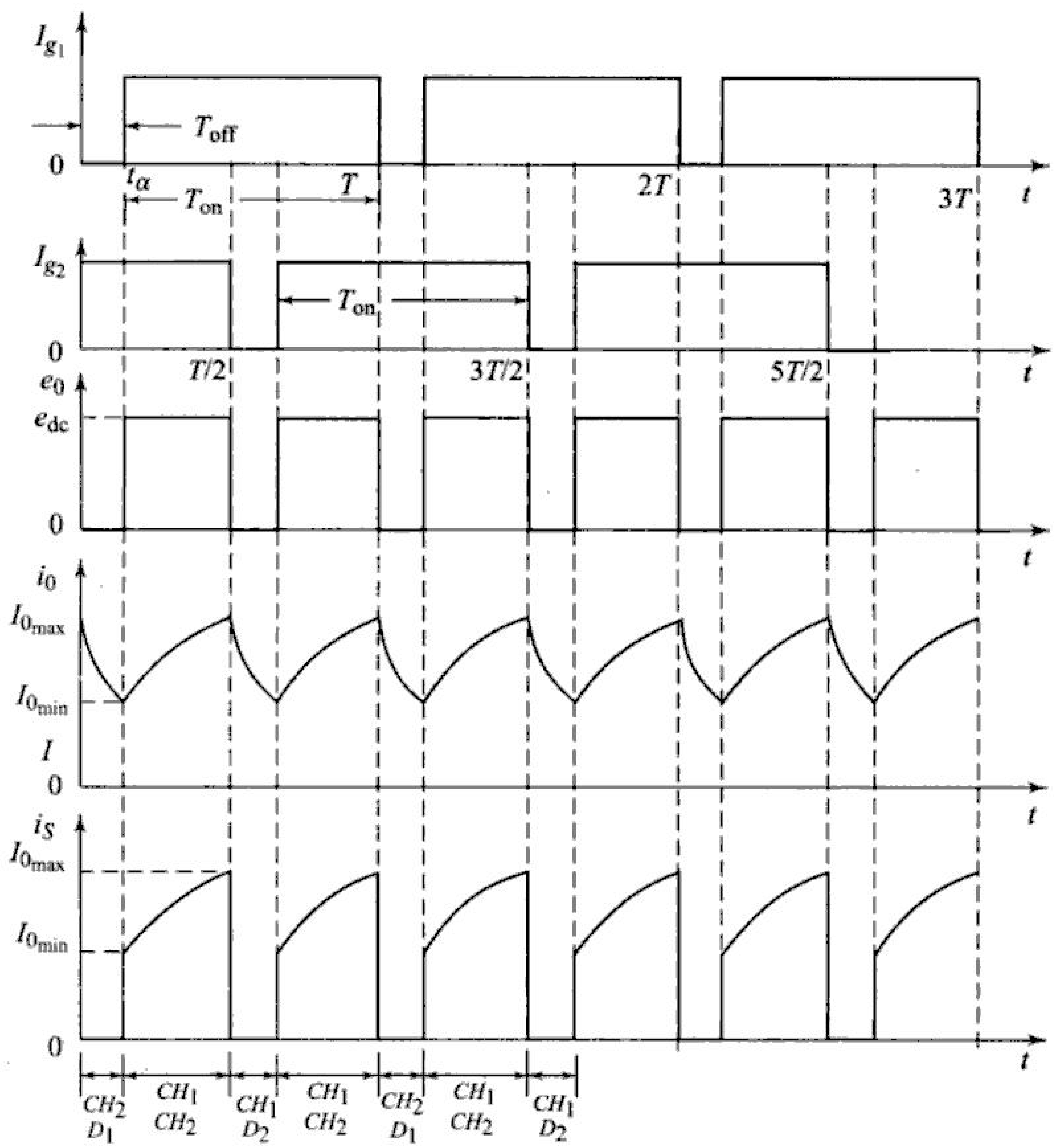

Fig. 8.23 *Mode 1 waveforms*

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and $e_0 = -E_{dc}$ if both the choppers are off and both diodes D_1 and D_2 are conducting. Also, it becomes clear that average output voltage E_0 is positive when $t_{on} > t_{off}$ and becomes negative when $t_{on} < t_{off}$. In this configuration, since average load current I_0 is positive and average load voltage E_0 is reversible, power-flow is also reversible. This Type D chopper configuration may be used for both motoring and regenerative breaking of the d.c. motor.

1. Fourier analysis of output voltage The load voltage waveform (e_0) of Figs 8.23 and 8.24 may be described by the Fourier series as

$$e_0 = E_0 + \sum_{n=1}^{\infty} C_n \sin(n\omega_0 t + \theta_n) \tag{8.79}$$

where n is a positive integer and ω_0 is defined by

$$\omega_0 = \frac{4\pi}{T} \text{ rad/s} \tag{8.80}$$

Equation (8.80) is based on the fact that one cycle of e_0 takes place in $T/2$ seconds. Also, the average value of e_0 is given by

$$E_0 = \left(1 - \frac{2t_\alpha}{T}\right) E_{dc} \tag{8.81}$$

or

$$E_0 = \left(\frac{2T_{on}}{T} - 1\right) E_{dc} \tag{8.82}$$

$$C_n = \frac{4E_{dc}}{n\pi} \sin\frac{n\omega_0 t_\alpha}{2} = \frac{4E_{dc}}{n\pi} \sin\frac{2\pi n t_\alpha}{T} \tag{8.83}$$

and

$$\theta_n = \frac{\pi}{2} - \frac{n\omega_0 t_\alpha}{2} = \frac{\pi}{2} - \frac{2n\pi t_\alpha}{T} \text{ rad} \tag{8.84}$$

The amplitude of the fundamental frequency in the waveform of e_0 is given by

$$C_1 = \frac{4E_{dc}}{\pi} \sin\frac{\omega_0 t\alpha}{2} = \frac{4E_{dc}}{\pi} \sin\frac{2\pi t_\alpha}{T} \tag{8.85}$$

Amplitude C_1 has its maximum value when $\omega_0 t_\alpha = \pi$ or 3π

That is, $$\frac{t_\alpha}{T} = 0.25 \text{ or } 0.75$$

The second value in above two cases corresponds to operation in the fourth quadrant, as shown in Fig. 8.24.

The average value of load-current I_0 is given by

$$I_0 = \frac{E_0 - E_b}{R} = \frac{1}{R}\left[\left(1 - \frac{2t_\alpha}{R}\right) E_{dc} - E_b\right] \tag{8.86}$$

Assuming $\omega_0 L >> R$, the RMS value of the fundamental component of current is

$$I_{R_1} = \frac{2\sqrt{2}E_{dc}}{\pi\omega_0 L} \frac{\sin 2\pi t_\alpha}{T} = \frac{E_{dc}}{\sqrt{2}\cdot\pi^2 L} \sin\frac{2\pi t_\alpha}{T} \tag{8.87}$$

The RMS load current is given by

$$I_{\text{RMS}} = \sqrt{(I_0)^2 + \left(I_{R_1}\right)^2} \tag{8.88}$$

On the assumption that load current is constant at magnitude I_0, the source current waveform is similar to that of e_0, and, the pulses of source current is having magnitude I_0. Therefore, with the similar analysis of e_0, the average value of source current is given by

$$I_s = \left(1 - \frac{2t_\alpha}{T}\right) I_0 \tag{8.89}$$

The output power P_0 is given by, $P_0 = E_0 \cdot I_0$

$$= \left(1 - \frac{2t_\alpha}{T}\right) E_{\text{dc}} \cdot I_0 = E_{\text{dc}} \cdot I_s = p_{\text{in}} \tag{8.90}$$

SOLVED EXAMPLES

Example 8.14 A Class C chopper is operated from a 220 V battery. The load is a dc motor with $R = 0.1\ \Omega$, $L = 10$ mH and $E_b = 100$ V. Determine the following:

(i) Duty cycle for the motoring mode
(ii) Critical duty-cycle for the regenerative mode
(iii) Duty cycle to achieve regenerative braking at the rated current of 10 Amp
(iv) Power returned to the source during braking

Solution:

Given $E_{\text{dc}} = 220$ V, $R = 0.1\ \Omega$, $L = 10$ mH, $E_b = 100$

(i) The average load current is given by

$$i_0 = \frac{E_o - E_b}{R} = \frac{\alpha \cdot E_{\text{dc}} - E_b}{R}$$

$$\therefore \quad \alpha = \frac{i_o \cdot R + E_b}{E_{\text{dc}}} = \frac{(10 \times 0.1) + 100}{220}, \quad \therefore \quad \alpha = 0.459$$

(ii) Critical duty cycle for regenerative braking $= \dfrac{E_b}{E_{\text{dc}}} = 0.4545$

(iii) Duty cycle to achieve regenerative braking at the rated current of $i_0 = 10$ Amp.

$\therefore$ Rated load current, $i_0 = \dfrac{\alpha \cdot E_{\text{dc}} - E_b}{R}$

For regeneration this current should be negative.

$$\therefore \quad -10 = \frac{(\alpha \cdot 220) - 100}{0.1}, \quad \therefore \quad D = 0.45$$

(iv) Power returned to source during braking

$= E_b\, i_0 - i_0^2 R = 100 \times 10 - (10^2 \times 0.1) = 990$ Watts

Example 8.15 A two-quadrant chopper operating in the first and fourth quadrant is operated from a 220 V battery. The load is dc motor with $R = 0.1\ \Omega$, L = 10 mH and $E_b = 100$ V, determine:

(i) Duty cycle α_m for motoring mode
(ii) Critical duty cycle for regenerative braking
(iii) Duty-cycle to achieve regenerative braking at the rated current of 10 Amp
(iv) Power returned to the source during braking
(v) The switching frequency of the devices if the output frequency is 5 kHz.

Solution:

Given: $E_{dc} = 220$ V, $R = 0.1\ \Omega$, $L = 10$ mH, $E_b = 100$ V, $i_0 = 10$ Amp

Class-D chopper operates in first and fourth quadrant

(i) Duty-cycle for motoring mode (α_m):

From equation (8.82), $E_0 = (2 \cdot \alpha_m - 1)\, E_{dc}$

$$\text{Average-load current } I_0 = \frac{E_0 - E_b}{R}$$

$$10 = \frac{(2\,\alpha_m - 1)\cdot(220) - (110)}{0.1} \qquad \therefore\ \alpha_m = 0.73$$

(ii) Critical duty-cycle for regenerative braking is given by

$$\alpha_c = (1 - \alpha_m) = (1 - 0.73) = 0.27$$

(iii) Duty-cycle for regeneration of rated armature current (α_R) :

$$\text{Rated average armature current} = \frac{E_b - E_0}{R}$$

But $\qquad E_0 = -(2\alpha_R - 1)$ during braking

$$\therefore\quad 10 = \frac{100 + (2\,\alpha_R - 1)\,220}{0.1} \qquad \therefore\ \alpha_R = 0.275$$

(iv) Power-returned to the source during braking interval:

$P = E_b \cdot i_0 - i_0^2 R_a = (100 \times 10) - (100 \times 0.1) = 990$ W

(v) Switching frequency of device:

In Class-D chopper, the switching frequency of power switch is half the output frequency.

$$\therefore \qquad f_s = 2.5\ \text{kHz.}$$

8.5.5 Four-Quadrant Chopper (or Class E Chopper)

Figure 8.25(a) shows the basic power circuit of Type E chopper. From Fig. 8.25, it is observed that the four-quadrant chopper system can be considered as the parallel combination of two Type C choppers. In this chopper configuration, with motor load, the sense of rotation can be reversed without reversing the polarity of excitation. In Fig. 8.25, CH_1, CH_4 D_2 and D_3 constitute one Type C chopper and CH_2, CH_3, D_1 and D_4 form another Type C chopper circuit. Figure 8.25(b) shows Class-E with R–L load.

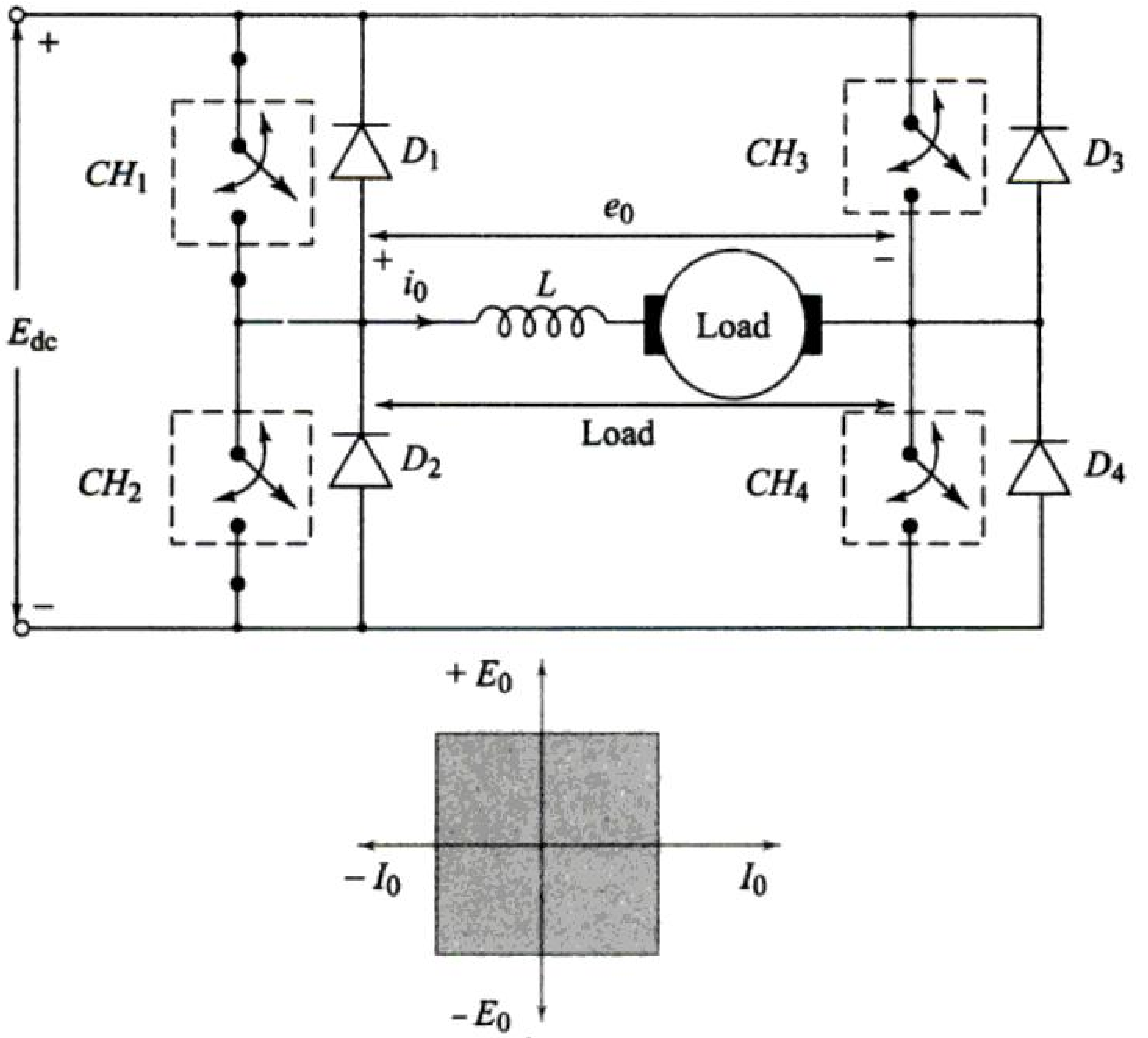


Fig. 8.25(a) *Type E chopper circuit and characteristic*

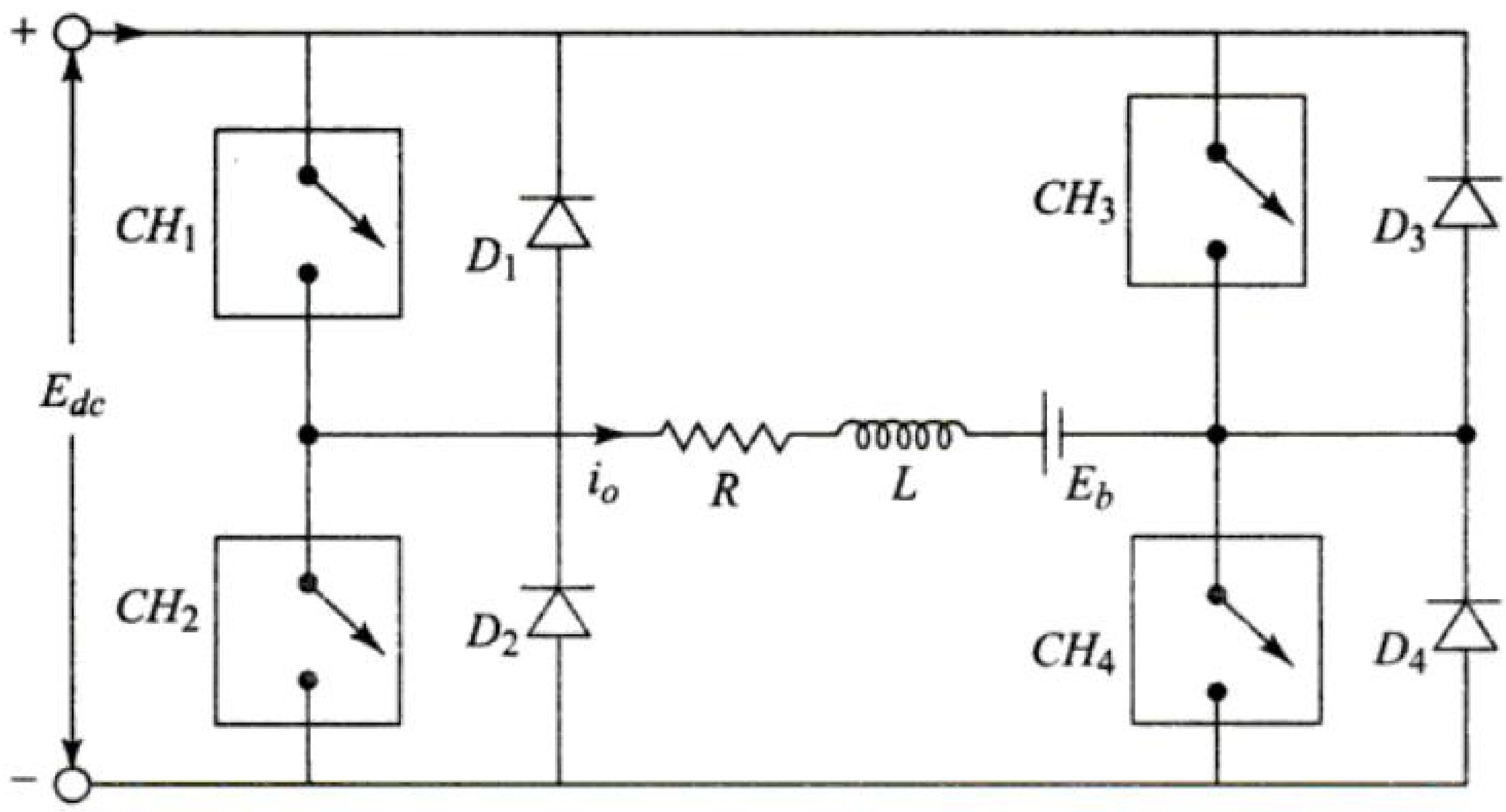


Fig. 8.25(b) *Class E chopper with R–L load*

If chopper CH_4 is turned on continuously, the antiparallel connected pair of devices CH_4 and D_4 constitute a short-circuit. Chopper CH_3 may not be turned on at the same time as CH_4 because that would short circuit source E_{dc}.

With CH_4 continuously on, and CH_3 always off, operation of choppers CH_1 and CH_2 will make E_0 positive and I_0 reversible, and operation in the first and second quadrants is possible. On the other hand, with CH_2 continuously on and CH_1 always off, operation of CH_3 and CH_4 will make E_0 negative and I_0 reversible, and operation in the third and fourth quadrants is possible.

The operation of the four-quadrant chopper circuit is explained in detail as follows:

When choppers CH_1 and CH_4 are turned-on, current flows through the path, $E_{dc+} - CH_1$ – load – $CH_4 - E_{dc-}$. Since both E_0 and I_0 are positive, we get the first quadrant operation. When both the choppers CH_1 and CH_4 are turned-off, load dissipates its energy through the path load–$D_3 - E_{dc+} - E_{dc-} - D_2$ – load. In this case, E_0 is negative while I_0 is positive, and fourth-quadrant operation is possible.

When choppers CH_2 and CH_3 are turned-on, current flows through the path, $E_{dc+} - CH_3$ – load – $CH_2 - E_{dc-}$. Since both E_0 and I_0 are negative, we get the third-quadrant operation. When both choppers CH_2 and CH_3 are turned-off, load dissipates its energy through the path load– $D_1 - E_{dc+} - E_{dc-} - D_2$ – load. In this case, E_0 is positive and I_0 is negative, and second-quadrant operation is possible.

This four-quadrant chopper circuit consists of two bridges, forward bridge and reverse bridge. Chopper bridge CH_1 to CH_4 is the forward bridge which permits energy flow from source to load. Diode bridge D_1 to D_4 is the reverse bridge which permits the energy flow from load-to-source. This four-quadrant chopper configuration can be used for a reversible regenerative d.c. drive.

SOLVED EXAMPLES

Example 8.16 A four-quadrant chopper is driving a separately excited dc motor load. The motor parameters are $R = 0.1$ ohm, $L = 10$ mH. The supply voltage is 200 V d.c. If the rated current of the motor is 10 A and if the motor is driving the rated torque. Determine:

(i) the duty cycle of the chopper if $E_b = 150$ V.
(ii) the duty cycle of the chopper if $E_b = -110$ V.

Solution:

For a four-quadrant chopper, the average voltage in all the four-modes is given by

$$E_0 = 2\,E_{dc} \cdot (\alpha - 0.5)$$

(i) The average current, $i_0 = \dfrac{E_0 - E_b}{R} = \dfrac{2\,E_{dc} \cdot (\alpha - 0.5) - E_b}{R}$

$$10 = \frac{2 \times 200\,(\alpha - 0.5) - 150}{0.1} \qquad \therefore\ \alpha = 0.876$$

Since, $\alpha > 0.5$, this mode is forward-motoring

(ii) Now, $10 = \dfrac{2 \times 200\,(\alpha - 0.5) - 110}{0.1}, \quad \therefore\ \alpha = 0.228$

As $\alpha < 0.5$, this mode is reverse motoring mode.

8.6 THYRISTOR CHOPPER CIRCUITS

In the previous sections, a chopper has been considered as an ideal on-off switch. The power switch used can be any power semiconductor devices like, SCR, power BJT, Power MOSFET, IGBT, MCT, etc. the power devices used as a switch must satisfy the required voltage and current ratings. The use of these devices however decides the performance of chopper in the following manner:

(i) As the operating frequency increases, the size of the inductance required to make the current continuous decreases. Hence, the size and cost of the chopper decreases. The efficiency and reliability increases. The operating frequency of the power devices is minimum for SCR and maximum for power MOSFET.

(ii) The power-devices have different power-capabilities, operating frequency and different gating requirements. The power-level of SCR is highest and power-level for MOSFET is the lowest. Gating requirements of transistor are complex while for MOSFET, IGBT and MCT are simplest. Hence, different power-devices are suitable for different requirements, e.g. for high-power-levels, SCR is the choice whereas for low power-levels, MOSFET can be used so that the gating requirements are simplest and operating frequency can be made higher to reduce the size of the chopper.

SCR based chopper circuit consists of a main power SCR switch together with the commutation circuitry to turn it OFF. There are several ways in which an SCR can be turned-off. The commutation techniques used for dc choppers are:

1. Forced Commutation In this type of commutation, current through the thyristor is forced to become zero to turn it OFF. This can be accomplished in two ways:

(a) Voltage commutation: In this scheme, a charged capacitor momentarily reverse-biases the conducting SCR and turns it OFF.

(b) Current commutation: In this scheme, a current pulse is forced in the reverse direction through the conducting SCR. As the net current becomes zero, the thyristor is turned OFF.

2. Load Commutation In this type of commutation, the load current flowing through the SCR either becomes zero (as in natural or line commutation employed in converters) or is transferred to another device from the conducting thyristors.

8.6.1 Voltage or Impulse Commutated Chopper

Figure 8.26 shows the basic power circuit diagram of voltage commutated chopper. This commutation circuit comprises an auxiliary SCR T_2, a diode D, inductor L and capacitor C; the complete chopper circuitry has been outlined with a dotted box. The main power switch is SCR T_1.

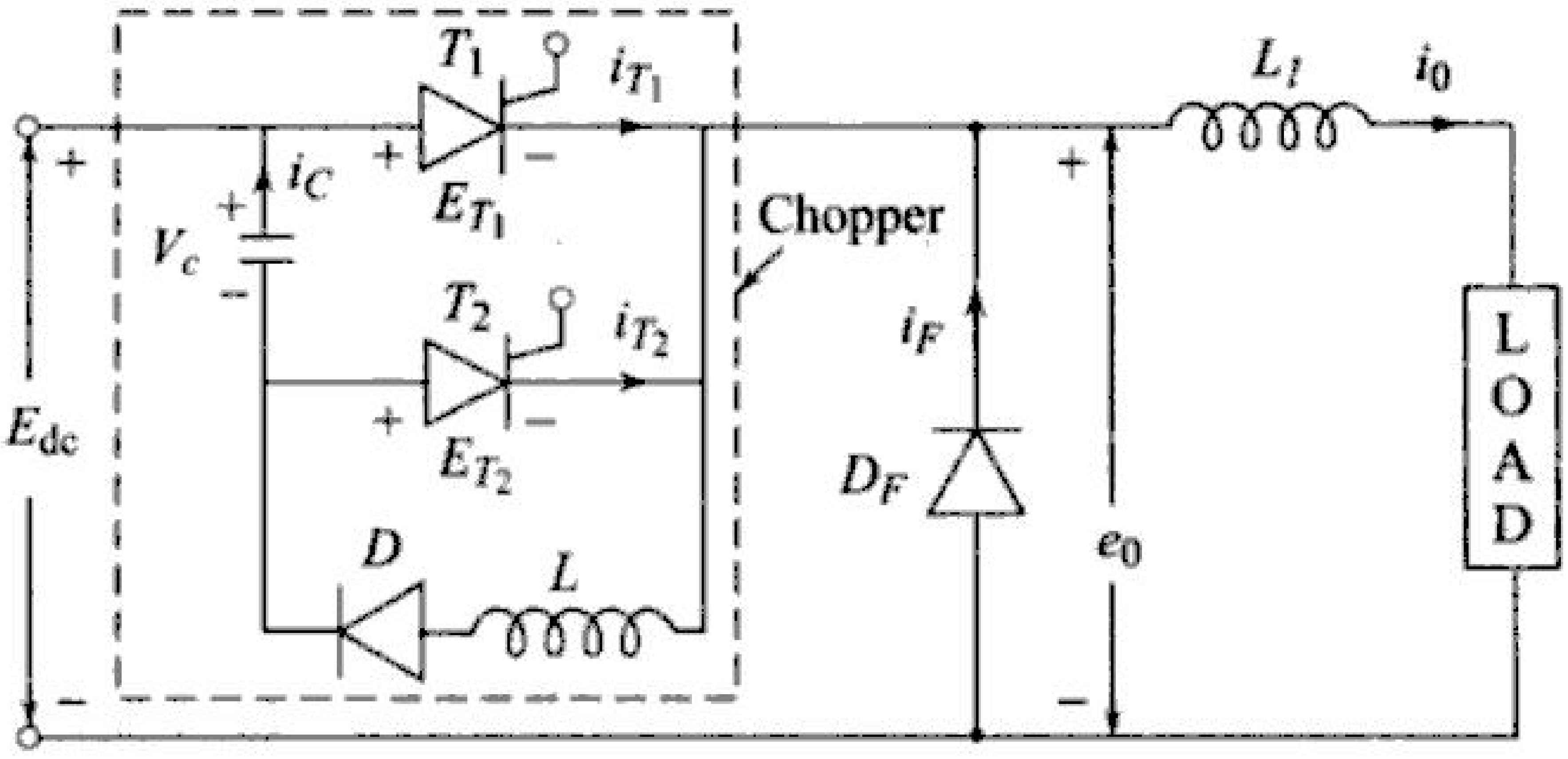


Fig. 8.26 *Voltage commutated chopper*

To start the circuit, capacitor C is initially charged with the polarity shown, by triggering the auxiliary SCR T_2. Capacitor C gets charged through the path $E_{dc+} - C_+ - C_- - T_2 - L_1$ load $- E_{dc-}$. As the charging current decays to zero, thyristor T_2 will be turned OFF. Figure 8.27 shows the associated voltage and current waveforms. For convenience, the chopper operation is divided into certain modes and is explained as under:

***(i) Mode I Operation** $(0 < t < t_2)$:* The main SCR T_1 is triggered at t_0. Source current flows in two paths, load current i_o constitutes one path and commutation current i_c, the other path. With the triggering of SCR T_1, load gets connected to the supply and the load voltage, $e_0 = E_{dc}$.

Load current i_0 flows through the path, $E_{dc+} - T_1 -$ load $- E_{dc-}$, whereas the commutating current i_c flows through the path, $C_+ - T_1 - L - D - C_-$. The capacitor current first rises from zero to a maximum value when voltage across capacitor C is zero at $t = t_1/2$. As i_c decreases to zero, capacitor is charged to a reverse voltage $(-E_{dc})$ at $t = t_1$ as shown in Fig. 8.27. This reverse voltage on capacitor is held constant by diode D.

At $t = 0$, voltage across auxiliary thyristor T_2 is $(-E_{dc})$, whereas it is zero at $t_1/2$ and E_{dc} at t_1. This voltage variation is shown as cosine wave in Fig. 8.27. Therefore, at $t = t_1$, $i_{T_1} = I_0$, $V_c = -E_{dc}$, $E_{T_2} = E_{dc}$, $e_0 = E_{dc}$, as shown in Fig. 8.27. These conditions continue upto the period t_2.

***(ii) Mode II Operation** $(t_2 < t < t_3)$:* At a desired instant t_2, the auxiliary SCR T_2 is to be triggered for turning-off the main SCR T_1. With the turning-on of T_2, reverse capacitor voltage $(-E_{dc})$ appears across T_1, which reverse-biases it, and turns it OFF. Since the capacitor voltage commutates the main SCR T_1, the given circuit of Fig. 8.26 is called as voltage commutated chopper. Current i_{T_1} becomes zero at t_2.

After the SCR T_1 is turned-off, the capacitor C and SCR T_2 provide the path for load current i_0 through $E_{dc} - C - T_2 -$ load. The load voltage is the sum of source voltage and the voltage across the capacitor. Hence, at instant t_2, load voltage is $e_0 = E_{dc} + E_{dc} = 2E_{dc}$, and it decreases linearly as the voltage across the capacitor decreases. During this mode, $V_c = E_{T_1}$, since the capacitor is directly connected across T_1 through T_2. As the capacitor discharges through the load, V_c and E_{T_1} change from $(-E_{dc})$ to zero at $(t_2 + t_q)$. Load-voltage e_0 changes from $2E_{dc}$ at t_2 to E_{dc} at $(t_2 + t_q)$. After $(t_2 + t_q)$, V_c and E_{T_1} start rising from zero towards E_{dc}, whereas e_0 starts falling towards zero. Hence, in this mode, V_c and E_{T_1} change linearly from $(-E_{dc})$ at t_2 to E_{dc} at t_3, since load current i_0 is assumed constant. Similarly, e_0 changes linearity from $2E_{dc}$ at t_2 to zero at t_3.

(iii) Mode III Operation ($t_3 < t < t_4$) : For this mode, $t_3 < t < T$. At t_3, $V_c = E_{T1} = E_{dc}$, $e_0 = 0$ and capacitor current decays to zero, therefore, SCR T_2 turns-off naturally. At t_3, since capacitor is slightly over-charged, freewheeling diode gets forward-biased. The load current after t_3 freewheels through this diode D_F. Note that during freewheeling period from t_3 to T, E_{T_2} is slightly negative as capacitor C is somewhat overcharged.

Thus, during this mode, $i_c = 0$, $i_{T_1} = 0$, $i_f = I_{0m}$, $E_{T_1} = E_{dc}$, $e_0 = 0$, $i_{T_2} = 0$.

Now, at $t = T$, the main thyristor T_1 is triggered again and the cycle as described from $t = 0$ to $t = T$ repeats.

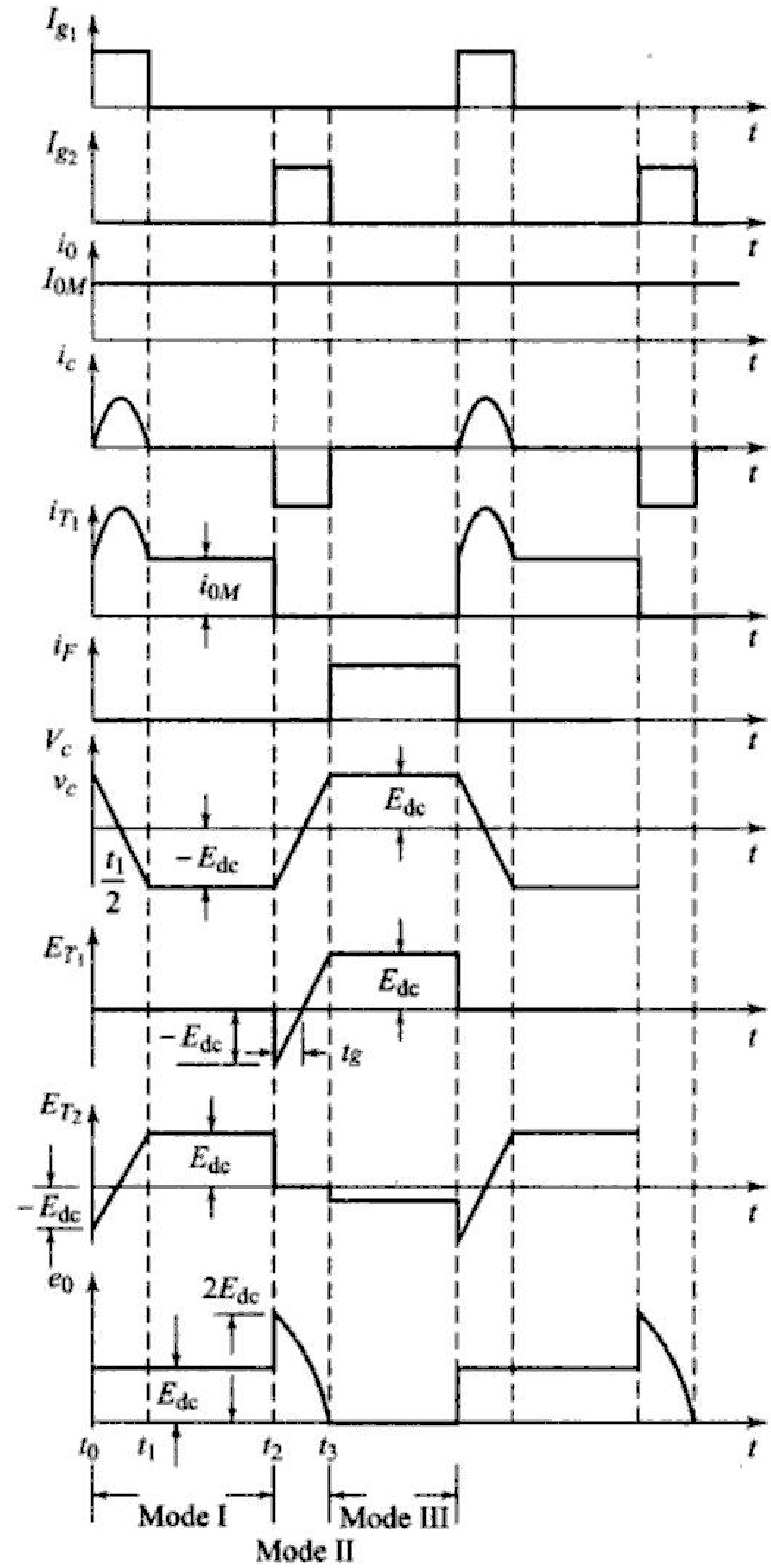


Fig. 8.27 *Related voltage and current waveforms*

1. Disadvantages Since voltage commutated chopper circuit is a simple chopper circuit, it is therefore widely used. However, it suffers from the following disadvantages:

(i) A starting circuit is required, and the starting circuit (such as logic circuit) should be such that it triggers auxiliary SCR T_2 first.

(ii) Load voltage jumps to twice the supply voltage when the commutation is initiated.

(iii) The circuit imposed turn-off time is load dependent. At very low load currents, the capacitor takes longer time to discharge, thus limiting the frequency of the chopper.

(iv) This circuit does not work at no load conditions, because, at no load, capacitor would not get charged from $-E_{dc}$ to E_{dc} when auxiliary SCR T_2 is triggered for commutating the main SCR T_1, that is, the capacitor voltage fails to commutate.

(v) The main thyristor T_1 has to carry the load current as well as the commutation current.

2. Design Considerations In this section, we see the selection method of commutating capacitor C and commutating inductor L.

(i) Commutating Capacitor C The commutating capacitor value is based on the turn-off time (t_q) available for main SCR T_1. During this time t_q, the capacitor voltage rises from ($-E_{dc}$) to zero, as explained in Mode II operation.

It is known that, $i_c = C\dfrac{dV_c}{dt}$

For constant load current I_{0m} during commutation, the above relation can be written as

$$I_{0m} = C\frac{E_{dc}}{t_q} \text{ or } C = \frac{I_{0m}t_q}{E_{dc}} \tag{8.91}$$

where I_{0m} is the maximum-load current.

Circuit turn-off time (t_q) must be greater than the SCR turn-off time (t_{off}), for reliable commutation.

$$\text{Let } t_q = t_{off} + \Delta t \quad \therefore\ C = \frac{I_{0m}(t_{off} + \Delta t)}{E_{dc}} \tag{8.92}$$

(ii) Commutating Inductor L The design criteria for inductor L is based on the peak value of the capacitor current i_c, which flows through T_1 when it is triggered, and the time ($t_1 - t_0$) during which the capacitor current pulse lasts.

When SCR T_1 is triggered, the capacitor current i_c flows through the ringing circuit formed by C, T_1, L, D, and is given by

$$i_c = \frac{E_{dc}}{\omega_r \cdot L}\sin \omega_r \cdot t \tag{8.93}$$

where $\omega_r = \dfrac{1}{\sqrt{LC}} = \dfrac{2\pi}{T_r}$ is the ringing frequency in radians per second and $T_r = 2\,(t_1 - t_0)$

$$i_c = E_{dc} \cdot \sqrt{\frac{C}{L}}\ \sin\omega_r t \tag{8.94}$$

Also, the peak capacitor current (I_{cp}) is

$$I_{cp} = \frac{E_{dc}}{\omega_r \cdot L} = E_{dc} \cdot \sqrt{\frac{C}{L}} \tag{8.95}$$

When T_1 is turned-on, it carries both, load current and the peak capacitor current. It is usual to take I_{cp} less than, or equal to, load current I_{0m}, so that the peak current through T_1 is not unnecessarily large, i.e.

$$I_{cp} \le I_{0m} \quad \text{or} \quad E_{dc}\sqrt{\frac{C}{L}} \le I_{0m} \tag{8.96}$$

or

$$L \ge C\left(\frac{E_{dc}}{I_{0m}}\right)^2 \tag{8.97}$$

By selecting a small value of the commutating inductance L, the resetting time $(t_1 - t_0)$ can be reduced. It can be seen from Eq. (8.95), that the small value of inductance L increases the peak value of the capacitor current. Also, if the duration $(t_1 - t_0)$ is large, the range of load voltage is reduced.

Therefore, the minimum load voltage is given by

$$E_{0(\min)} = \frac{(t_1 - t_0)}{T} \cdot E_{dc} \tag{8.98}$$

where T is the chopping period of the chopper

or

$$E_{0(\min)} = \frac{\pi\sqrt{LC}}{T} E_{dc} \tag{8.99}$$

The minimum value of load, voltage should be equal to or less than 10% of the supply voltage E_{dc} in order to vary the load voltage over a wide range.

Therefore, $\frac{(t_1 - t_0)}{T} E_{dc} \le 0.1\ E_{dc}$ or $\frac{(t_1 - t_0)}{T} \le 0.1$

or

$$\frac{\pi\sqrt{LC}}{T} \le 0.1 \text{ or } L \le \frac{0.01T^2}{\pi^2 C} \tag{8.100}$$

If duty-cycle has to be reduced, inductance L value has to be decreased but the peak capacitor current increases. Hence, a compromise has to be made between the Eqs (8.97) and (8.99).

SOLVED EXAMPLES

Example 8.17 A voltage commutated chopper circuit of Fig. 8.26 controls the battery-powered electric cars. The battery voltage is 80 V, starting current is 80 A and thyristor turn-off time is 20 μs, chopping period 2000 μs. Compute the values of the commutating capacitor C and the commutating inductor L.

Solution: For reliable operation, the circuit turn-off time must be greater than the SCR turn-off time (t_{off}).

Let $t_q = t_{\text{off}} + \Delta t$

Also, let $\Delta t = t_{\text{off}} = 20\ \mu\text{s} \quad \therefore\ t_q = 40\ \mu\text{s}.$

From Eq. (8.92), $C = \dfrac{I_{0m}(t_{\text{off}} + \Delta t)}{E_{\text{dc}}} = \dfrac{80(40\times10^{-6})}{80} = 40\ \mu\text{F}.$

From Eq. (8.97), $L \ge C\left(\dfrac{E_{\text{dc}}}{I_{0m}}\right) \ge 40\times10^{-6}\left(\dfrac{80}{80}\right)^2 \ge 40\ \mu\text{H}$

Also given, chopping period = 2000 μs from Eq. (8.100).

$$\therefore\quad L \le \frac{0.01T^2}{\pi^2 C}\quad L \le \frac{0.01(2000\times10^{-6})^2}{\pi^2\times40\times10^{-6}} \le 101.32\ \mu\text{H}.$$

The value of the commutating inductor is in the range $40 < L < 101.32$ μH. A value of L close to 40 μH will be a good choice because it will allow the minimum load voltage be about 5% of the supply voltage, hence giving a wider range of variation in the load voltage.

8.6.2 Current or Resonant-Pulse Commutated Chopper

Figure 8.28 shows the basic power-circuit for current commutated chopper. Here, T_1 is the main thyristor. The commutation circuit consists of auxiliary thyristor T_2, capacitor C, inductor L, diodes D_1 and D_2. D_F is the freewheeling diode and R is the charging resistor. The main SCR T_1 is commutated by a current pulse generated in the commutation circuitry. The important feature of this type of chopper is that the reverse voltage across the device is applied through a diode connected in antiparallel to the SCR. Since this is limited to about one volt, the turn-off time of SCR increases in comparison with the voltage commutations.

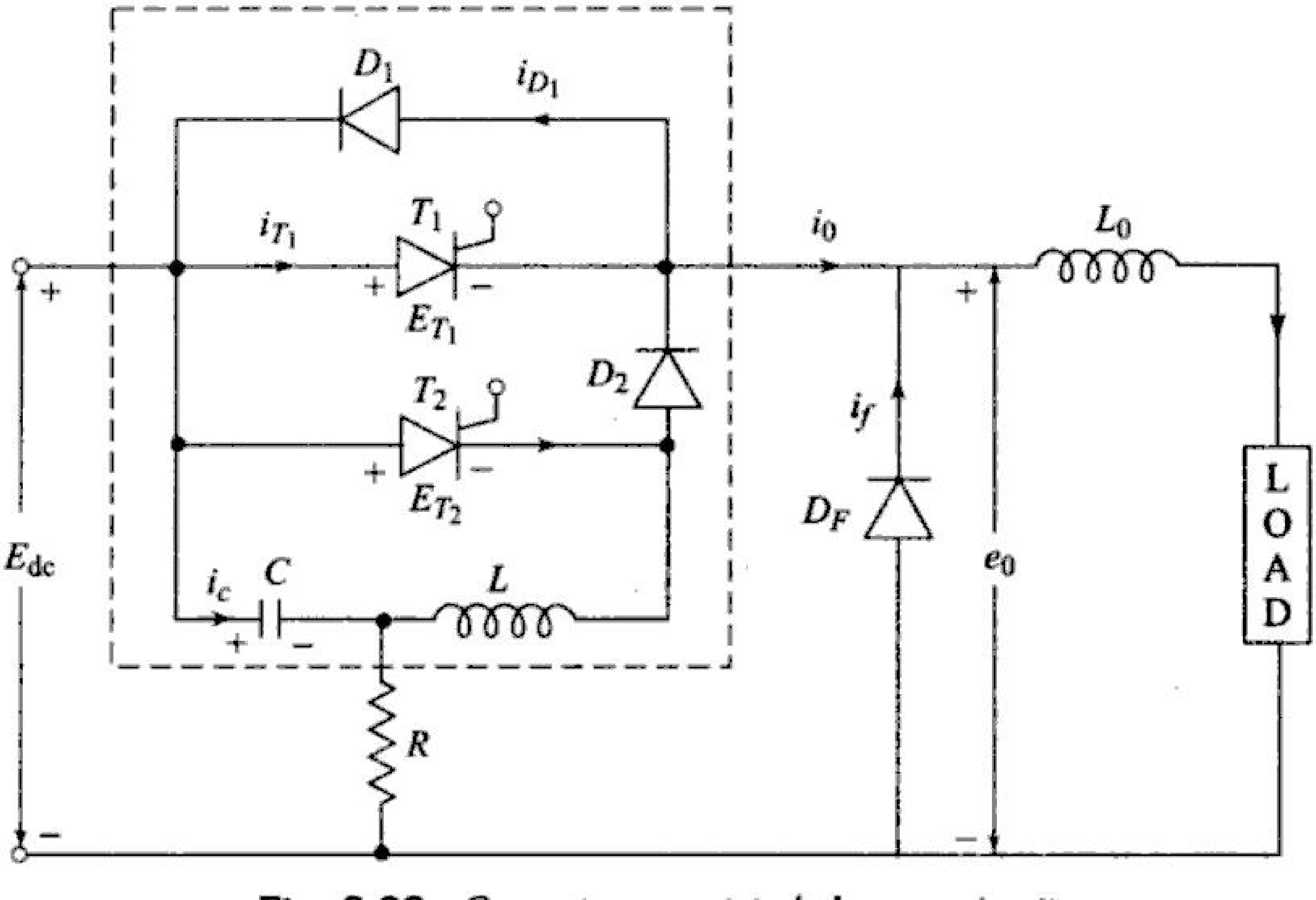


Fig. 8.28 *Current commutated chopper circuit*

As in voltage commutated chopper, here also the energy for current commutation comes from the energy stored in a capacitor. To start the circuit, the capacitor is charged to a voltage E_{dc} through the path $E_{dc+} - C - R - E_{dc-}$. The main thyristor T_1 is triggered at $t = t_0$, so that load voltage $e_0 = E_{dc}$ and load current $i_0 = I_{0m}$, up to $t = t_i$, as shown in Fig. 8.29.

For convenience, the commutation process is divided into certain modes and is explained as follows.

(i) Mode I Operation At time $t = t_1$, auxiliary SCR T_2 is triggered to commutate the main thyristor T_1. When thyristor T_2 is turned-on, an oscillatory current $\left(i_c = \frac{E_{dc}}{\omega_r L} \sin \omega_r t\right)$ is set up in the circuit consisting of C, T_2, and L. At t_2, the capacitor current i_c reverses, therefore, SCR T_2 gets turned-off due to natural commutation, and at t_2, $V_c = -E_{dc}$. In this mode, main thyristor T_1 remains unaffected and hence load voltage and load current remains E_{dc} and I_{0m} respectively.

(ii) Mode II Operation Since T_2 is turned-off at t_2, oscillatory current i_c flows through C, L, D_2 and T_1. As shown in Fig. 8.29, after t_2, current i_c would flow through thyristor T_1 and not through D_1, because D_1 is reverse biased by a small voltage drop across conducting thyristor T_1. Hence, after t_2, i_c would flow through T_1 and not through D_1. As current i_c flows in the opposite direction in T_1, it decreases the current i_{T_1}.

At t_3, $i_c = i_{T_1}$ and so the net current through T_1 is zero and it turns-off. As the oscillatory current through T_1 turns it OFF, it is called as current commutated chopper. During this mode, load voltage remains E_{dc} through T_1.

(iii) Mode III Operation Since T_1 is turned-off at t_3, i_c becomes more than i_0. After t_3, i_c supplies load current i_0 and diode D_1 begins to conduct the current $(i_c - i_0)$ and the drop in D_1 due to this current keeps the thyristor T_1 reverse-biased for the time t_q $(= t_4 - t_3)$.

(iv) Mode IV Operation As shown in Fig. 8.29, at t_4, $i_c = i_0$ and $iD_1 = 0$; therefore, diode D_1 is reverse-biased. After t_4, a constant current equal to i_0 flows through $E_{dc} - c - L - D_L -$ load and therefore, capacitor C is charged linearly to source-voltage E_{dc} at t_5. Therefore, during the period $(t_4–t_5)$, $i_c = i_0$.

As D_1 is turned-off at, t_4, $v_c = E_{t_1}$. Now, the load voltage $e_0 = E_{dc} - V_c$ at t_4 and at t_5, $V_c = E_{dc}$. Hence, at t_5 load voltage become $e_0 = E_{dc} - E_{dc} = 0$. During the interval $(t_4–t_5)$, V_c increases linearity and therefore, load voltage e_0 decreases to zero linearity, during this period.

(v) Mode V Operation As shown in Fig. 8.29, at t_6, capacitor C is actually overcharged to a voltage somewhat greater than source voltage E_{dc}. Therefore at t_5, the freewheeling diode D_F becomes forward biased and starts to conduct the load current i_0. As i_c is not zero at t_5, the capacitor C is still connected to load through source $E_{dc} - C - L$ and D_2, and as a result C is overcharged by the transfer of energy from L to C. Therefore, at t_6, $i_c = 0$ and V_c becomes more than E_{dc}.

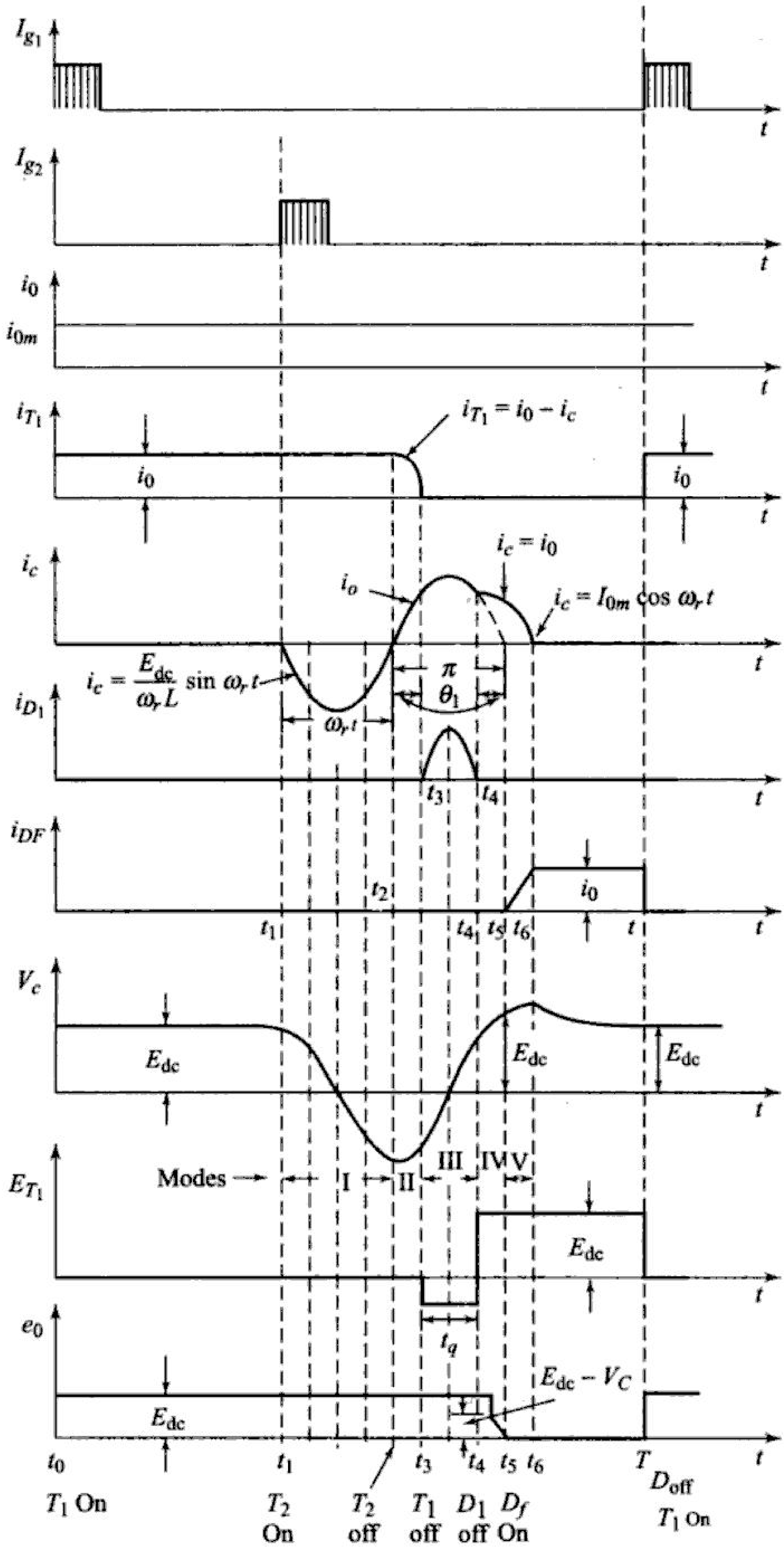


Fig. 8.29 *Voltage and current waveforms for current commutated chopper*

During interval t_5 to t_6, $i_0 = i_c + i_F$ and therefore, as i_c decays, i_F builds up. At t_6, $i_F = i_0$ and $i_c = 0$. Commutation process is completed at t_6 and the commutation interval is $(t_6 - t_1)$.

From t_6 onwards, load current freewheels through D_F and decays. As i_c is zero and D_2 is open circuited, capacitor voltage V_c decays through R for the freewheeling period of the chopper.

At $t = T$, the main thyristor T_1 is triggered again and the cycle repeats.

This chopper was developed by the Hitachi-Electric Company, Japan and is widely used in traction cars.

1. Advantages The following are the main advantages of current commutated chopper:

(i) The capacitor always remains charged with the correct polarity.

(ii) Commutation is reliable as long as load current is less than the peak commutation current I_{cp}.

(iii) The auxiliary thyristor T_2 is naturally commutated as its current passes through zero value.

2. Design Considerations The values of the commutating components L and C are selected to satisfy the following conditions, for reliable commutation of main SCR T_1.

(a) The peak commutating current I_{cp} must be greater than the maximum possible load current I_{0m}. This condition is very essential for reliable commutation of main SCR T_1.

From Eq. (8.95), the oscillating current is given by

$$i_c = E_{dc}\sqrt{\frac{C}{L}}\sin\omega_r t = I_{cp}\cdot\sin\omega_r t$$

From condition (a), we make the relation

$$I_{cp}\left(= E_{dc}\sqrt{\frac{C}{L}}\right) > I_{0m}. \text{ or, } E_{dc}\sqrt{\frac{C}{L}} = x\cdot I_{0m} \tag{8.101}$$

where I_{0m} = maximum load current and x is greater than 1. Therefore,

$$x = \frac{I_{cp}}{I_{0m}} \tag{8.102}$$

(b) The circuit turn-off time (t_q) must be greater than the thyristor T_1 turn-off time (T_{off}), therefore,

$$t_q = t_{off} + \Delta t.$$

From Fig. 8.29 with the current waveform, we can write,

$$t_q = t_4 - t_3 \quad \text{or} \quad \omega_r t_q = \pi - 2\theta_1 \tag{8.103}$$

Also, $I_{cp} \sin \theta_1 = I_{0m}$ or, $\theta_1 = \sin^{-1}\left(\frac{I_{0m}}{I_{cp}}\right) = \sin^{-1}\left(\frac{1}{x}\right)$ (8.104)

Circuit turn-off time for main SCR T_1 from Eq. (8.103),

$$t_q = \frac{1}{\omega_r}(\pi - 2\theta_1) \tag{8.105}$$

Substitute the value of θ_1 from Eq. (8.104),

$$t_q = \frac{1}{\omega_r}\left[\pi - 2\sin^{-1}\left(\frac{I_{0m}}{I_{cp}}\right)\right] \tag{8.106}$$

From Eq. (8.106), it becomes clear that as load current I_{0m} increases, circuit turn-off time for main SCR T_1 decreases. Thus, a certain value of ratio $\left(\frac{I_{0m}}{I_{cp}}\right)$ must be maintained for ensuring necessary turn-off time t_q.

Substituting $\omega_r = \frac{1}{\sqrt{LC}}$ in Eq. (8.106), we get

$$t_q = \sqrt{LC}\left[\pi - 2\sin^{-1}\left(\frac{1}{x}\right)\right] \tag{8.107}$$

or

$$\sqrt{C} = \frac{t_q}{\sqrt{L}\left[\pi - 2\sin^{-1}(1/x)\right]} \tag{8.108}$$

Substituting this value of $\sqrt{C}$ in Eq. (8.101), we get

$$\frac{E_{dc}}{L}\frac{t_q}{\left[\pi - 2\sin^{-1}(1/x)\right]} = x \cdot I_{0m} \text{ or } L = \frac{E_{dc}t_q}{x \cdot I_{0m}\left[\pi - 2\sin^{-1}(1/x)\right]} \tag{8.109}$$

From Eq. (8.107), we have

$$\frac{1}{\sqrt{L}} = \frac{\sqrt{C}}{t_q}\left[\pi - 2\sin^{-1}(1/x)\right]$$

Substituting the above value of $\sqrt{L}$ in Eq. (8.101) gives

$$\frac{E_{dc}\sqrt{C}\sqrt{C}\left[\pi - 2\sin^{-1}(1/x)\right]}{t_q} = x \cdot I_{0m} \text{ or } C = \frac{x \cdot I_{0m} \cdot t_q}{t_q\left[\pi - 2\sin^{-1}(1/x)\right]} \tag{8.110}$$

3. Peak Capacitor Voltage From capacitor voltage waveform of Fig. 8.29, it is clear that the maximum capacitor voltage is reached at t_8. Therefore, voltage at $t_6 = V_{cp}$ = voltage at t_5 + voltage rise due to the energy transferred from L to C during t_5 to t_8.

At instant t_5, energy stored in L is $\frac{1}{2}LI_{0m}{}^2$ and at t_6, this energy is transferred to C. Thus, the voltage rise of capacitor C due to this transfer to energy is,

$$\frac{1}{2}CV_c^2 = \frac{1}{2}LI_{0m}^2 \tag{8.111}$$

or
$$V_c = I_{0m}\sqrt{\frac{L}{C}} \tag{8.112}$$

Now, substituting Eq. (8.112) in Eq. (8.103),

$$\therefore \quad V_{cp} = E_{dc} + I_{0m}\sqrt{\frac{L}{C}} \tag{8.113}$$

The peak voltage and current value of capacitor are also the peak ratings of both the main and auxiliary thyristors.

The charging resistor R is selected such that the chopping period T is much greater than 3 RC.

SOLVED EXAMPLES

Example 8.18 For a current commutated chopper, peak commutating current is thrice the maximum possible load current. The source voltage is 220 V d.c. and main SCR turn-off time is 20 μs. For a maximum load current of 180 A, compute

(a) the value of commutating components L and C
(b) maximum capacitor voltage, and
(c) the peak commutating current.

Solution: Given: $x = 3$ $t_{off} = 20$ μs, $\therefore t_q = t_{off} + \Delta t = 20 + 20 = 40$ μs

(a) From Eq. (8.109), $L = \dfrac{E_{dc} \cdot t_q}{x \cdot I_{0m}\left[\pi - 2\sin^{-1}(1/x)\right]}$

$$= \frac{220 \times 40 \times 10^{-6}}{3 \times 180\,[\pi - 2\sin^{-1}(1/3)]} = 6.62\ \mu\text{H}$$

From Eq. (8.110), $C = \dfrac{x \cdot I_{0m} \cdot t_q}{E_{dc}\left[\pi - 2\sin^{-1}(1/x)\right]}$

$$= \frac{3 \times 180 \times 40 \times 10^{-6}}{220 \times [\pi - 2\sin^{-1}(1/s)]} \quad \therefore \quad C = 39.88\ \mu\text{F}$$

(b) From Eq. (8.113) the peak capacitor voltage is given by

$$V_{cp} = E_{dc} + I_{0m}\sqrt{\frac{L}{C}} = 220 + 180\sqrt{\frac{6.62 \times 10^{-6}}{39.88 \times 10^{-6}}} = 293.34\text{ V.}$$

(c) Peak commutating current

$$i_{cp} = x \cdot I_0 = 3 \times 220 = 660\text{ A}$$

8.6.3 Load Commutated Chopper

Figure 8.30 shows the power-circuit of a load commutated chopper. This chopper circuit consists of four thyristors T_1, T_2, T_3 and T_4, and one commutating capacitor C. Here, thyristors T_1, T_2 form one pair and thyristors T_3, T_4 form another pair which conduct the load current alternatively. When one thyristor pair T_1, T_2 functions as main thyristors, at the same time other thyristor pair T_3, T_4 functions as auxiliary thyristors, and *vice-versa*. Again, operation of the chopper circuit is divided into different operating modes. These modes are described with the associated waveforms as shown in Fig. 8.31.

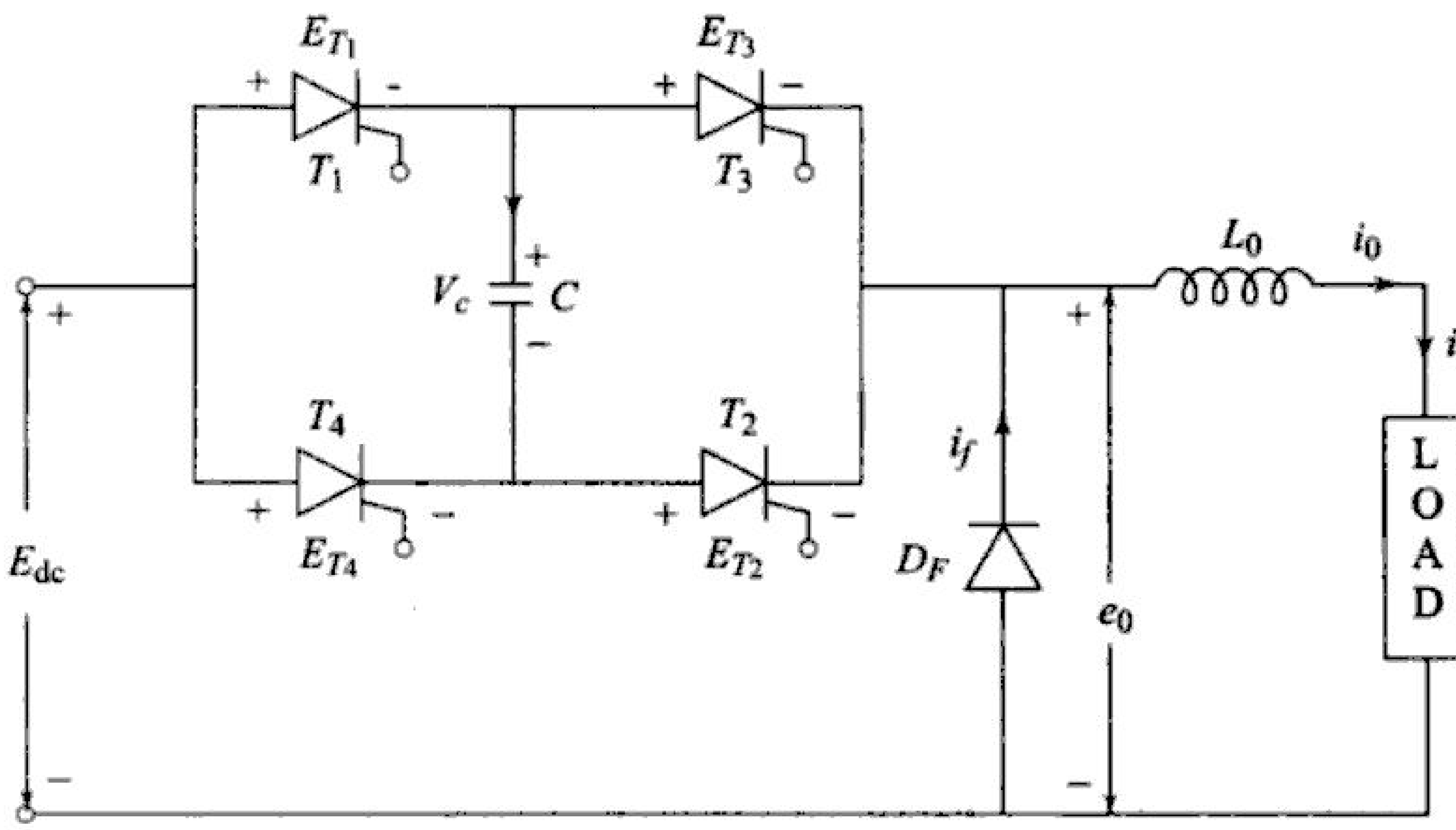


Fig. 8.30 *Load commutated chopper circuit*

The waveforms shown in Fig. 8.31 starts at the instant $t = t_0$. It is assumed that prior to this instant t_0, capacitor C was charged to the reverse voltage ($-E_{dc}$) due to the conduction of thyristors T_3 and T_4. Therefore, before the instant t_0, the capacitor upper plate becomes negative and lower plate positive.

(i) Mode I Operation As shown in Fig. 8.31, at $t = t_0$ both thyristors T_1 and T_2 are triggered. Therefore, load current flows through the path $E_{dc} - T_1$, C, T_2 and the load. Load voltage e_0 now becomes, $e_0 = E_{dc} - V_c$, i.e., 2 E_{dc}. The capacitor C is charged linearly by a constant load current i_0 from ($-E_{dc}$) at $t = 0$ to E_{dc} at t_1.

When the capacitor is charged fully positive at $t = t_1$, the current through the conducting thyristors T_1, T_2 becomes zero and these go into the blocking mode. The load voltage e_0 falls linearly. The freewheeling diode D_f becomes forward biased, and the load current is transferred from T_1 and T_2 to D_f.

(ii) Mode-II Operation As shown in Fig. 8.31, from t_1 to T, the freewheeling diode D_F conducts the load current. For the period t_1 to T, $V_c = E_{dc}$, $i_c = 0$, $i_f = i_0$ and the load voltage $e_0 = 0$. Now, at $t =$ T, the second pair of thyristors T_3, T_4 is triggered. This places the fully charged capacitor across thyristors T_1 T_2, reverse biasing them and turning them off. The cycle now repeats.

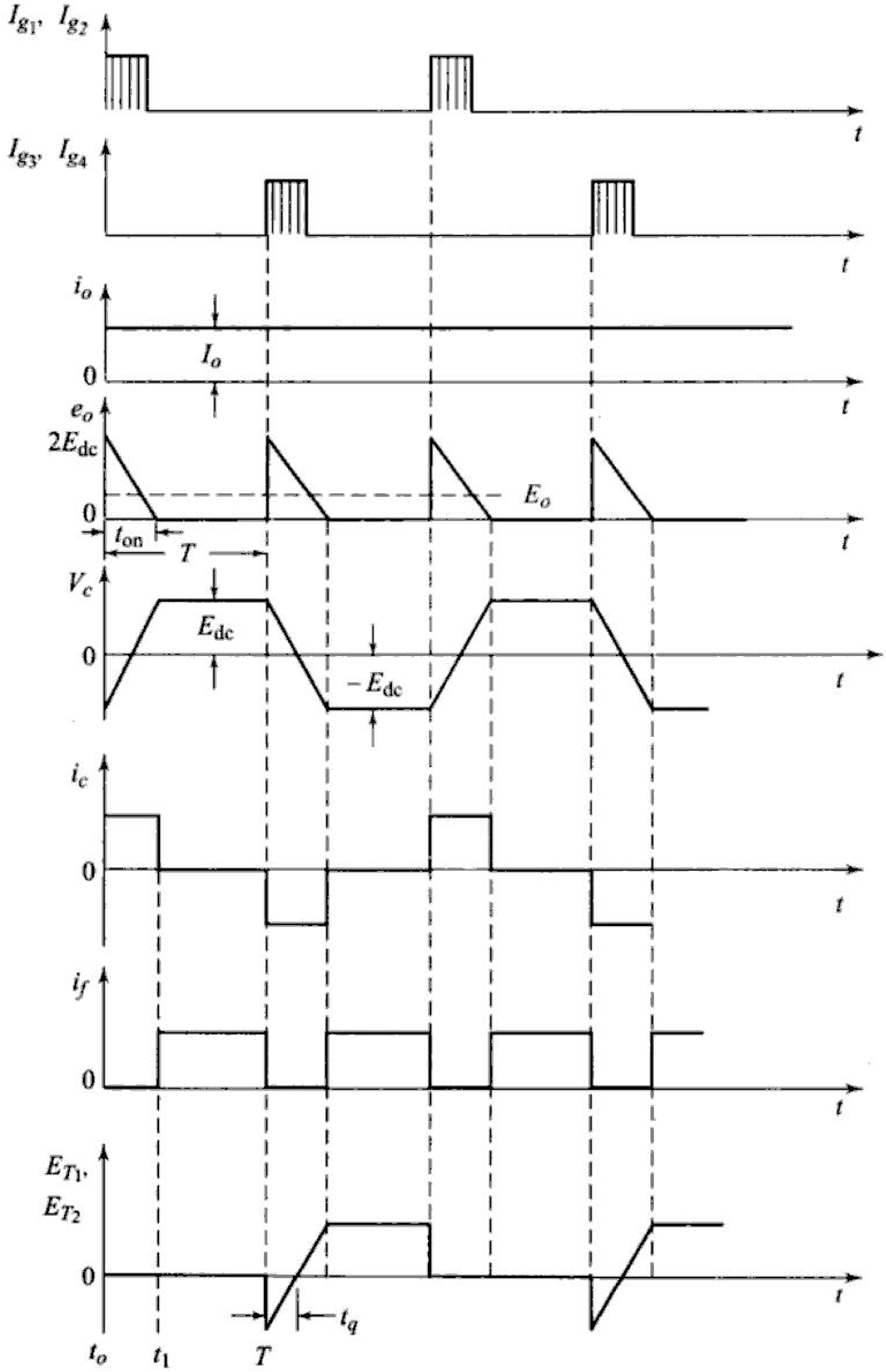


Fig. 8.31 *Voltage and current waveforms of load-commutated chopper*

1. Design Considerations The average value of the chopper output voltage is controlled by changing the firing frequency of the choppers. Thus, it is a frequency modulated chopper.

As shown in Fig. 8.31, for a constant load current I_0, capacitor voltage changes from $(-E_{dc})$ to E_{dc} in time T_{on}, i.e. total change in voltage is $2E_{dc}$ in time t_{on}.

Therefore, $$I_0 = \frac{2E_{dc} \cdot C}{T_{on}} \tag{8.114}$$

or $$T_{on} = \frac{2E_{dc} \cdot C}{I_0} \tag{8.115}$$

The output voltage is, $E_0 = E_{dc} \dfrac{T_{on}}{T} = E_{dc} \cdot T_{on} \cdot f$

Substituting the value of t_{on} from Eq. (8.115) in above equation, we get

$$E_0 = \frac{2E_{dc}^2 cf}{I_0} \tag{8.116}$$

where f = chopper frequency Minimum chopping period $T_{min} = T_{on}$.

$\therefore$ Maximum chopping frequency,

$$f_{max} = \frac{1}{T_{min}} = \frac{1}{T_{on}} \tag{8.117}$$

Substituting value of T_{on} from Eq. (8.115) in Eq. (8.117),

$$f_{max} = \frac{I_0}{2 \cdot E_{dc} \cdot c}$$

Now, output voltage at maximum frequency is given by

$$E_0|_{f_{max}} = \frac{2E_{dc}^2 C}{I_0} \cdot \frac{I_0}{2E_{dc} \cdot C} \quad \therefore E_0|_{f_{max}} = E_{dc} \tag{8.118}$$

From Eqs (8.116) and (8.118), $E_{dc} = \dfrac{2E_{dc}^2 . C}{I_0} f_{max}$

or $$f_{max} = \frac{I_0}{2E_{dc} \cdot C} \tag{8.119}$$

This type of chopper has the following advantages and disadvantages.

2. *Advantages*

(i) This chopper is capable of commutating any amount of current.

(ii) No commutating inductor is required in this chopper circuit which is normally costly, bulky and noisy.

(iii) This circuit can operate at high frequencies of the order of kHz, and therefore filtering requirements to smooth out load current are minimal.

3. *Disadvantages*

This chopper circuit has some minor disadvantages, as follows:

(i) The peak load voltage is twice the supply voltage. However, this peak can be reduced by filtering.
(ii) Because of higher switching losses at high frequencies and losses in the two conducting thyristors in series with the load, efficiency may become low for high power applications.
(iii) Since freewheeling diode D_f is subjected to twice the supply voltage ($2\,E_{dc}$) in a short time, a fast recovery type diode must be used.
(iv) The commutating capacitor has to carry the load current at a frequency half the chopping period.
(v) One thyristor pair should be turned-on only when the other pair is commutated. This can be realised by sensing the capacitor current that is alternating.

SOLVED EXAMPLE

Example 8.19 A load commutated chopper, fed from a 230 V d.c. source has a constant load current of 50 A. For a duty cycle of 0.4 and a chopping frequency of 2 kHz, calculate

(a) the value of commutating capacitance. (b) average output voltage.
(c) circuit turn-off time for one SCR pair. (d) total commutation interval.

Solution:

(a) From Eq. (8.115), we have $C = \dfrac{t_{on} \cdot I_0}{2E_{dc}}$

Given: $\alpha = 0.4 = \dfrac{T_{on}}{T}, T = \dfrac{1}{f} = \dfrac{1}{2\times10^3} = 0.5 \text{ ms}$

$\therefore \quad 0.4 = \dfrac{T_{on}}{0.5 \text{ ms}}, \quad \therefore T_{on} = 0.2 \text{ ms}$

$C = \dfrac{0.2\times10^{-3}\times50}{2\times230}, C = 21.74\ \mu\text{F}$

(b) From Eq. (8.118), $E_0 = \dfrac{2E_{dc}^2 \cdot cf}{I_0}$

$$E_0 = \frac{2\times230\times230\times21.74\times10^{-6}\times2\times10^3}{50} = 92 \text{ V}$$

(c) For load commutated chopper circuit, the circuit turn-off time for each SCR is

$$t_q = \frac{1}{2}T_{on} = \frac{1}{2}\cdot\frac{C\cdot2E_{dc}}{I_0} = \frac{C\cdot E_{dc}}{I_0} = \frac{21.74\times10^{-6}\times230}{50} = 100\ \mu\text{s}$$

(d) Total commutation interval $= \dfrac{2CE_{dc}}{I_0} = \dfrac{2\times21.74\times10^{-6}\times230}{50} = 200\ \mu\text{s}$

8.7 JONES CHOPPER

Figure 8.32 shows the basic power circuit of Jones chopper. This chopper circuit is another example of Class D commutation. In this circuit, SCR T_1 is the main thyristor, whereas SCR T_2, capacitor C, D_2, and autotransformer (T) forms the commutating circuit for the main thyristor T_1. Therefore, the special feature of this circuit is the tapped autotransformer T through a portion of which the load current flows. Here, L_1 and L_2 are closely coupled so that the capacitor always gets sufficient energy to turn-off the main SCR T_1.

If the main thyristor T_1 is ON for a long period, then the motor will reach the maximum steady-state speed determined by the battery voltage, the motor and the mechanical load characteristics. If thyristor T_1 is OFF, the motor will not rotate. Now, if thyristor T_1 is alternatively ON and OFF in a cyclic manner, the motor will rotate at some speed between maximum and zero. Figure 8.33 shows the voltage and current waveforms of the chopper circuit.

Let us assume that initially capacitor C is charged to a voltage E_{dc} with the polarity shown in Fig. 8.32. As shown in Fig. 8.33, SCR T_1 is triggered at time $t = t_1$, current flows through the path $C_A - T_1 - L_2 - D_1 - C_B$ and capacitor C charges to opposite polarity, i.e. plate B is positive and plate A is negative. However, diode D_1 prevents further oscillation of the resonating L_2 C circuit. Hence, capacitor C retains its charge until SCR T_2 is triggered. In Fig. 8.33, the capacitor voltage waveforms are drawn at bottom plate B of capacitor.

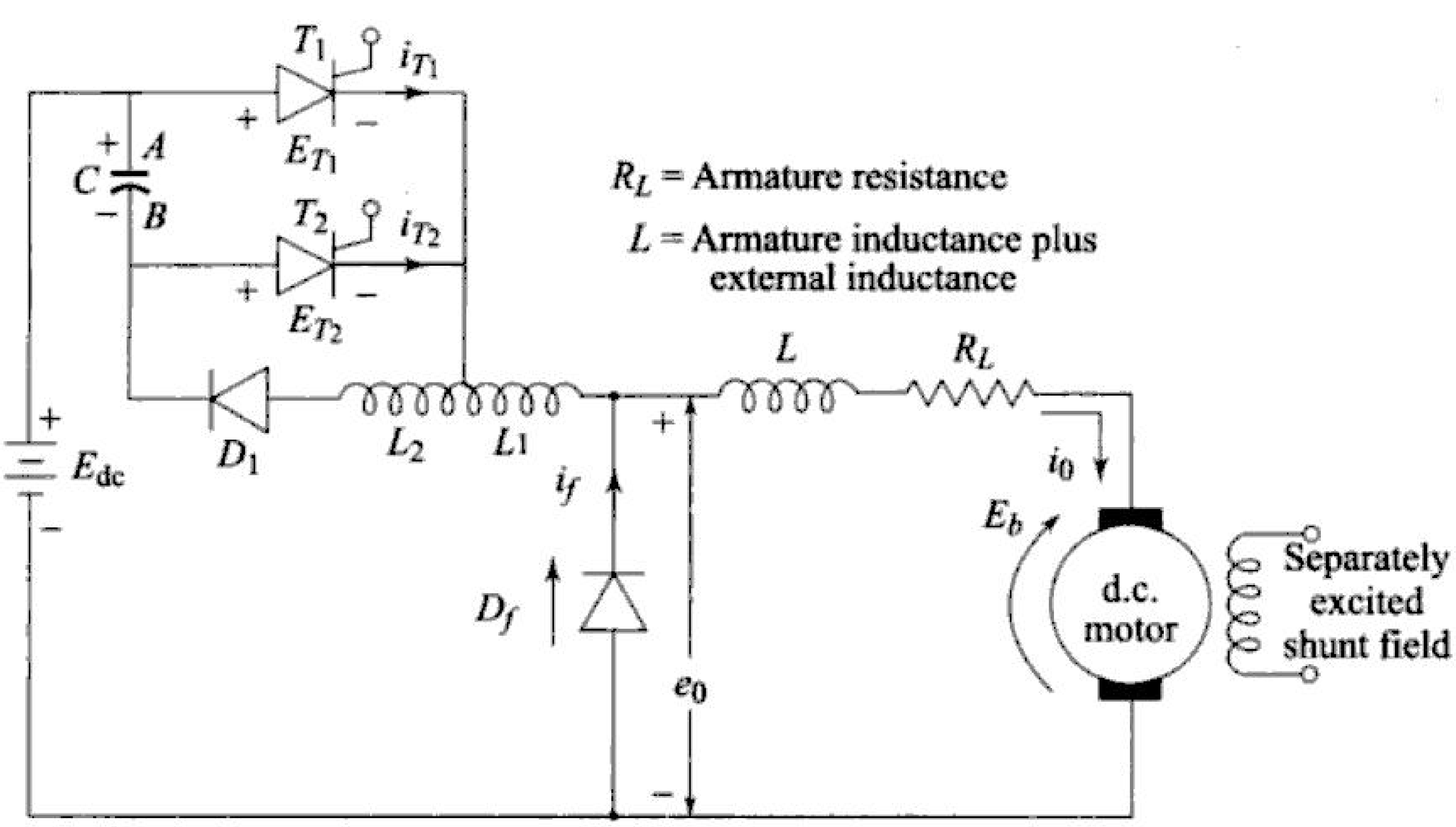


Fig. 8.32 *Freewheeling diode d.c. motor drive using Jones chopper*

Now, at time $t = t_3$, SCR T_2 is triggered. Current flow through the path $C_B - T_2 - T_1 - C_A$. Therefore, discharge of capacitor C reverse-biases SCR T_1 and turns it OFF. The capacitor again charges up with plate A positive and SCR T_2 turns-off because the current through it falls below the holding current value when capacitor C is recharged.

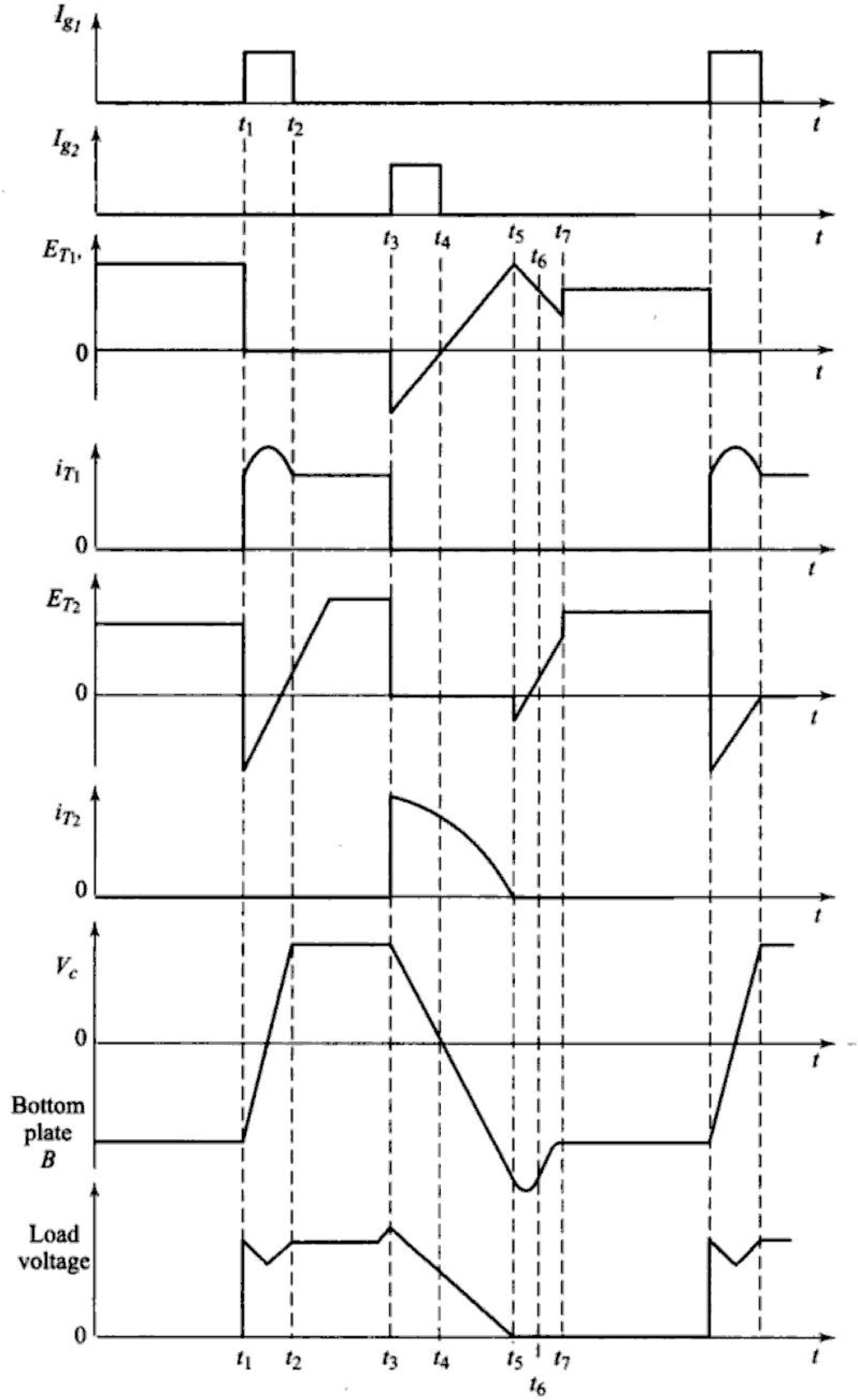


Fig. 8.33 *Jones chopper voltages and current waveforms*

The cycle repeats when SCR T_1 is again triggered. The use of autotransformer insures that whenever current is delivered from dc source to the load, a voltage is induced in L_2 in the correct polarity for changing the commutating capacitor to a voltage higher than E_{dc}. Thus, the autotransformer measurably enhances the reliability of the circuit.

At t_5, the bottom plate (B) of capacitor C reaches a peak value. Since at t_5, the capacitor is charged to a voltage greater than E_{dc}, diode D_1 is again forward biased. Capacitor C now discharges to a value lower than E_{dc}. The time duration t_3 to t_4 is the circuit turn-off time presented to SCR T_1.

Design Considerations : The basic design of the Jones chopper circuit involves the proper selection of commutating capacitor C and autotransformer T.

Initially, maximum load current I_{0m} is flowing through L_1. During turning OFF of SCR T_1, the energy stored in inductance L_1 is being transferred to capacitor C. Thus,

$$\frac{1}{2}L_1 I_{0m}^2 = \frac{1}{2}CV_c^2 \text{ or } V_c^2 / I_{0m}^2 = L_1/C$$

or
$$V_c = I_{0m} \cdot \sqrt{\frac{L_1}{C}} \tag{8.120}$$

During the turn-off time, t_q, the capacitor voltage changes from V_C to 0. Hence,

$$t_q = \frac{V_c \cdot C}{I_{0m}} \tag{8.121}$$

Substituting the value of V_c from Eq. (8.120) into Eq. (8.121), we get

$$t_q = \frac{I_{0m} \cdot \sqrt{\frac{L_1}{C}} \cdot C}{I_{0m}} \text{ or } t_q = \sqrt{L_1}\, C \tag{8.122}$$

Now, dividing Eq. (8.120) by E_{dc} yields:

$$\frac{V_c}{E_{dc}} = \frac{I_{0m}}{E_{dc}}\sqrt{\frac{L_1}{C}} \tag{8.123}$$

Let us define, $g = \dfrac{V_c}{E_{dc}}$ and $R_m = \dfrac{E_{dc}}{I_{0m}}$ then Eq. (8.123) becomes

$$g = \frac{1}{R_m}\sqrt{\frac{L_1}{C}} \tag{8.124}$$

Depending on the values of L_1, C and R_m, the value of g is greater than 1.

The voltage across SCRs T_1 and T_2 is

$$V_c = g \cdot E_{dc} \tag{8.125}$$

Hence, a large value of g would require an increase in the voltage rating of the thyristor in the circuit.

In this type of chopper circuit, only dissipative elements are winding resistance and the forward conducting resistance of the SCRs and diodes. Therefore, this circuit is basically very efficient. The inductance L maintains the load current through diode D_f when SCR T_1 is not conducting. Hence, the motor torque which is proportional to the load current is smooth rather than pulsating. If the inductance in the load circuit is small, the change in the load current is substantial, which would result in substantial torque ripple in the motor load.

SOLVED EXAMPLES

Example 8.20 The Jones chopper of Fig. 8.32 controls the electric car. Compute the value of commutating capacitor C and transformer inductance L_1 and L_2 for the following data:

$$E_{dc} = 60\text{V}, t_q = 20\ \mu\text{s}, I_{0m} = 140\ \text{A}, g = 4$$

Solution: From Eq. (8.124), $g = \dfrac{1}{R_m}\sqrt{\dfrac{L_1}{C}}$

But, $R_m = \dfrac{E_{dc}}{I_{0m}} = \dfrac{60}{140} = 0.43\ \Omega \quad \therefore \sqrt{\dfrac{L_1}{C}} = 4 \times 0.43 = 172$ (a)

Also, from Eq. (8.122), $t_q = \sqrt{L_1 C} \quad \therefore 20 \times 10^{-6} = \sqrt{L_1 C}$ (b)

Dividing Eq. (b) by Eq. (a), we get, $11.63 \times 10^{-6} = C \quad \therefore C = 11.63\ \mu\text{F}$

and $L_1 = 34.4\ \mu\text{H}$

Normally, L_2 is designed to be equal to L_1.

Example 8.21 A d.c. series motor is used in an electric rapid transit system, as shown in Fig. 8.32. The Jones chopper is used as a speed controller for this purpose.

(a) For the following data, compute the inductance, L, required to limit the current swing in the armature under the worst condition to 6 amperes.
Given data :
(i) Motor performance parameters:
n = rated speed in rpm = 1750, HP = horse power rating = 150 HP
R_a = armature circuit resistance in ohm = 0.0099 Ω., E_{ff} = efficiency of motor = 90%
E_a = armature voltage = 1200 V, L = inductance in series with armature
L = (armature inductance + series field inductance + external inductance)
(ii) Chopping period $T = 2500\ \mu$s.

(b) Also calculate the steady-state speed and the current swing in the armature for $\alpha = 0.10$ and $L = 125$ mH.
Assume rated current in the armature for all values of α, and $E_{dc} = 1200$ V, $\alpha = 0.1$

Solution: Average output voltage, $E_0 = \dfrac{T_{on}}{T} \cdot E_{dc} = \alpha E_{dc}$

The voltage across the inductor L is given by $(E_{dc} - \alpha \cdot E_{dc})$

$$\therefore \quad L \cdot \frac{di_a}{dt} = (E_{dc} - \alpha E_{dc}) \text{ or } \frac{di_a}{dt} = \frac{(E_{dc} - \alpha E_{dc})}{L}$$

Here, $dt = T_{on}$ $\therefore$ $di_a = \dfrac{(E_{dc} - \alpha E_{dc})}{L} T_{on}$ (a)

We can write the above equation as

$$di_a = \frac{(E_{dc} - \alpha E_{dc})}{L} \frac{T_{on}}{T} \cdot T = \frac{(E_{dc} - \alpha E_{dc})}{L} \alpha \cdot T \quad \text{(b)}$$

Now, differentiating Eq. (b) w.r.t α,

$$\therefore \quad \frac{di_a}{d\alpha} = \frac{E_{dc}}{L} T - \frac{2\alpha E_{dc}}{L} T$$

For worst case condition, $\dfrac{di_a}{d\alpha} = 0$

$$\therefore \quad 0 = \frac{E_{dc}}{L} T(1 - 2\alpha)$$

$$\therefore \quad (1 - 2\alpha) = 0$$

$\alpha = 0.5$ is the worst condition. Using $\alpha = 0.5$, in Eq. (b),

$$di_a = 6 = \frac{(1200 - 0.5 \times 1200)}{L} \times 0.5 \times 2500 \times 10^{-6}$$

$$\therefore \quad L = 125 \text{ mH}$$

(b) Power input to the motor $= P_{in} = \dfrac{\text{power output}}{\text{efficiency}} = \dfrac{150 \times 746}{0.9} = 124.33$ kW

Therefore, rated current in the armature $I_a = \dfrac{P_{in}}{E_{dc}} = \dfrac{124.33 \times 10^3}{1200} = 103.61$ A

$\therefore$ Armature voltage under rated torque condition is

$$E_{a(rated)} = E_{dc} - I_a \cdot R_a = 1200 - 103.1 \times 0.0099 = 1198.97 \text{ V}$$

For the above armature voltage, the speed is 1750.
For $\alpha = 0.1$, voltage at the armature is given by

$$\alpha \times 1200 - I_a \cdot R_a = 0.1 \times 1200 - 103.61 \times 0.0099 = 118.97 \text{ V.}$$

$\therefore$ Motor speed, $N = \dfrac{118.97}{1198.97} \times 1750 = 173.65$ rpm.

$$\text{Current swing} = \Delta i_a = \frac{(E_{dc} - \alpha E_{dc})}{L} \times \alpha T$$

$$= \left(\frac{1200 - 0.1 \times 1200}{125 \times 10^{-3}} \right) \times 0.1 \times 2500 \times 10^{-6} = 2.16 \text{ A.}$$

Example 8.22 Design the Jones chopper circuit for optimum frequency considerations to meet the following specifications:

Source voltage, $E_{dc} = 200$ V, Load current, $I_0 = 50$ A and $t_q = 200$ µs

Solution:

(i) *Selection of commutating capacitor C.* For obtaining optimum frequency so as to have lesser commutation losses and smaller commutation components, the commutation capacitor C can also be given by the following equation,

$$C \geq \frac{\pi}{2}\frac{t_q}{E_{dc}} I_0 \geq \frac{\pi}{2}\,\frac{200\times 10^{-6}}{200}\times 50 \geq 78.54\ \mu\text{F}.$$

Capacitor voltage rating = safety factor × E_{dc} = 1.5 × 200 = 300 V.

(ii) *Selection of inductance L_1.* From Eq. (8.122), we have the relation

$$t_q = \sqrt{L_1 C}$$

$$\therefore \quad L_1 = \frac{(t_q)^2}{C} = \frac{200\times 200\times 10^{-12}}{78.54\times 10^{-6}} = 0.51$$

$$\therefore \qquad L_1 = L_2 = 0.51\ \text{mH}.$$

(iii) *Selection of SCR T_1 (main SCR)*

$$V_{BO} = \text{safety factor} \times E_{dc} = 1.5 \times 200 = 300\ \text{V}$$

$$I_T = \text{safety current} \times I_0 = 1.5 \times 50 = 75\ \text{A}.$$

(iv) *Selection of auxiliary SCR T_2*

Turn-off time, $\quad t_q \leq \frac{\pi}{2}\sqrt{L_1 C} \leq \frac{\pi}{2}\sqrt{0.51\times 10^{-3}\times 78.54\times 10^{-6}} \leq 315$

or $t_q \cong 250$ µs and $V_{Bo} = 300$ V and $I_T = 75$ A.

(v) *Selection of diode D_l*
PIV rating of diode = V_{BO} of SCR = 300 V and $I_D = I_T = 75$ A.

(vi) SCR *dynamic characteristics*

(a) *Main* SCR T_1, $\dfrac{dV}{dt} = \dfrac{I_{0\max}}{C}$ volts per µs

$$= \frac{50}{78.54\times 10^{-6}} = 0.64 \text{ volts per µs.}$$

Initial $\qquad \dfrac{di}{dt} = \dfrac{E_{RRm}}{L_1}$ amp-per Hz

$$= \frac{\text{safety factor} \times E_{dc}}{L_1} = \frac{1.5\times 200}{0.51\times 10^{-3}} = 0.59\ \text{A/µs}.$$

(b) *Main* SCR T_2, $\dfrac{dV}{dt} = \dfrac{E_{peak}}{\sqrt{L_1 C}}$ volts per µs

$$= \frac{1.5\times 200}{\sqrt{0.51\times 10^{-3}\times 78.54\times 10^{-6}}} = 1.49\ \text{V/µs}.$$

$$\text{Initial } \frac{di}{dt} = \frac{E_{peak}}{L_s} \text{ A}/\mu s$$

Let us assume, L_1 = stray inductance during the discharging loop = 2 μH.

$$\therefore \quad \frac{di}{dt} = \frac{1.5 \times 200}{2\mu H} = 150 \text{ A}/\mu s.$$

8.8 MORGAN CHOPPER

Figure 8.34 shows the power-circuit of Morgan chopper. In this circuit, T_1 is the main thyristor, whereas capacitor C, saturable reactor SR and diode D_1 forms the commutating circuit. The exciting current of the saturable reactor is assumed to be negligible small. When the saturable reactor is saturated, it has very low inductance. The voltage and current waveforms of the Morgan-chopper is shown in Fig. 8.35.

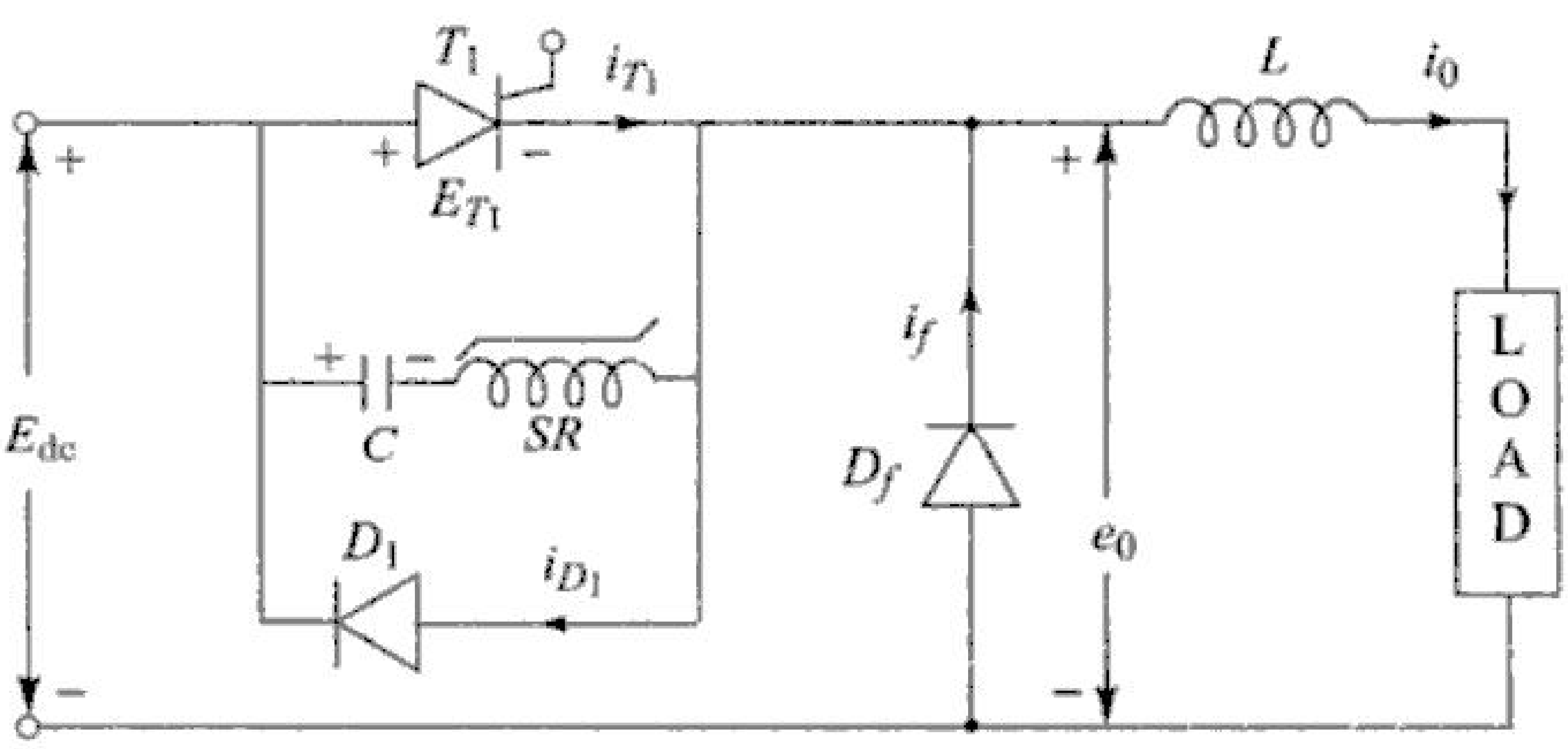


Fig. 8.34 Morgan chopper

When the main SCR T_1 is OFF, capacitor C will charge to the supply voltage E_{dc} with the polarity as shown in Fig. 8.34 and the saturable reactor is placed in the positive saturation condition. The capacitor charging path is $E_{dc+} - C - S_R -$ Load $- E_{dc-}$.

As shown in Fig. 8.35, thyristor T_1 is triggered at time $t = t_1$. When thyristor T_1 is turned-on, the capacitor voltage appears across the saturable reactor and the core flux is driven from the positive saturation towards negative saturation. The capacitor voltage remains essentially constant with the same polarity, till the negative saturation point is reached. This is due to the negligible exciting current of the SR.

When the core flux reaches the negative saturation, the capac·tor discharges through the SCR T_1 and the post-saturation inductance of SR. This forms a resonant circuit with a discharging time of $\pi\sqrt{L_s C}$ seconds, where L_s is the post-saturation inductance of the reactor. Thus, the discharging time of the capacitor is comparatively small and the reversal of the polarity of the capacitor takes place very quickly. After this, the capacitor voltage which is now $-E_{dc}$ is impressed on the saturable reactor in the reverse direction and the core is driven from negative saturation towards positive saturation.

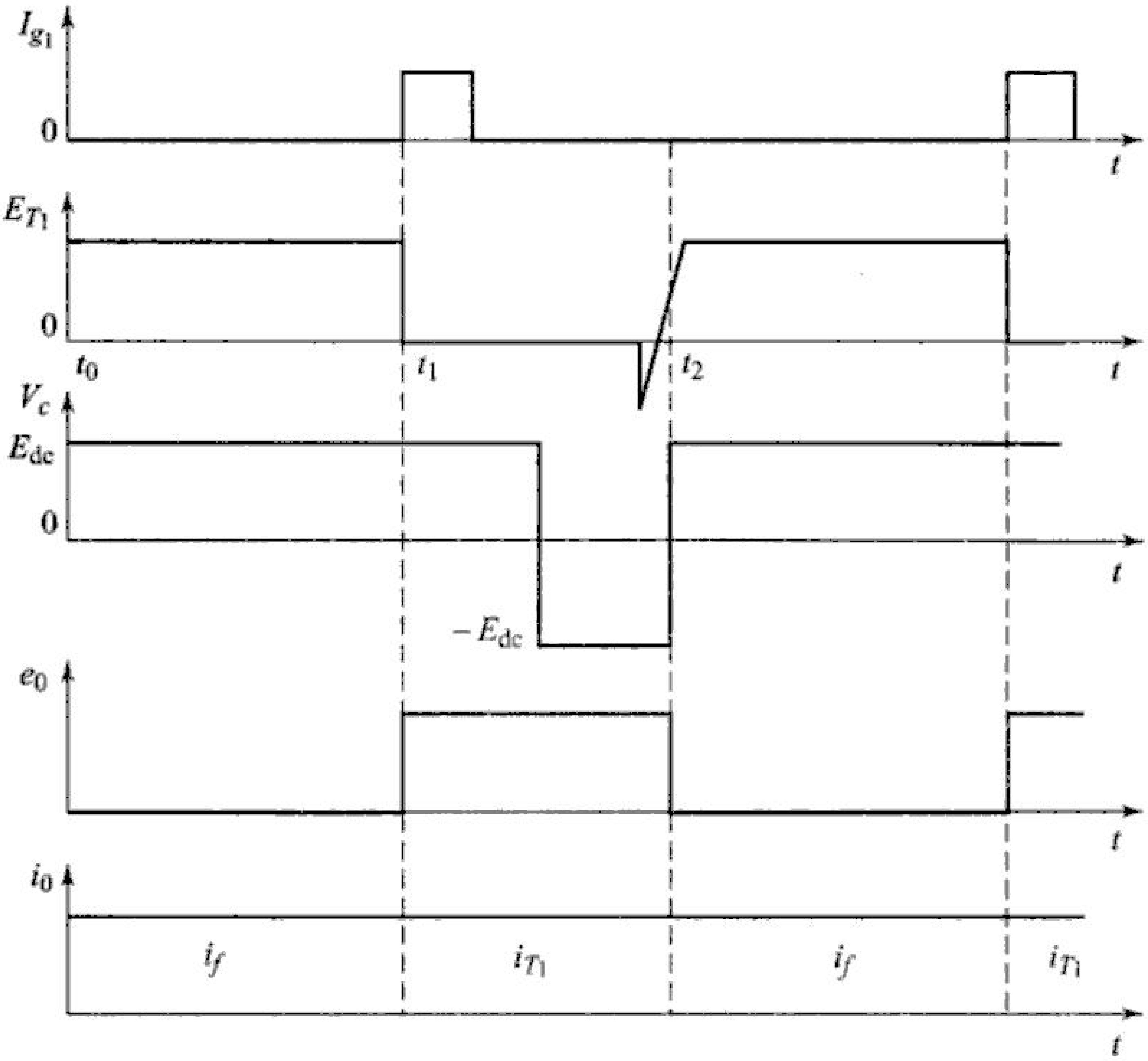


Fig. 8.35 *Morgan chopper voltage and current waveform*

After a fixed interval of time, the core flux reaches the positive saturation after which the capacitor discharges very quickly through SCR T_1 in the reverse direction and the post-saturation inductance as before. The discharge current first passes through SCR T_1, turning it OFF and then through diode D_1.

When SCR T_1 is turned-off the load current flows through the freewheeling diode D_f. Since the volt–time integral to saturate the core is constant, the ON period of SCR T_1 is fixed. The ON period is a function of L_s C and the average output voltage can be altered only by varying the operating frequency. Output voltage is lowered by lowering the frequency and increases by increasing the frequency. The ON period, however, can be controlled by varying the volt time product of the saturable reactor by means of d.c. controlled current through it. Also, the total ON time of SCR T_1 is determined by the time required for the saturable reactor to move from positive saturation to negative saturation and back to positive saturation again. Hence, the use of saturable reactor in place of linear reactor is advantageous in two ways: At the time of turn-off and charging of the capacitor, the inductance (saturated) is low and for on-time, it is high (unsaturated). The circuit cost is low due to the use of only one thyristor.

8.9 A.C. CHOPPERS

The a.c. voltage magnitude can be changed by two methods. The well-known first method is by means of step-up and step-down transformers. In this method, change in voltage depends on the value of transformation ratio of the transformer.

The second method of changing magnitude of an a.c. voltage is by means of a solid-state switch. In this method, the a.c. input voltage is switched ON and OFF periodically by means of a suitable switch. Voltage changing circuits employing semiconductor devices as a static switch, are known as a.c. choppers. Figure 8.36 shows the commonly used single-phase a.c. chopper circuit. In this circuit, SCR T_1 and T_2 are the main SCR whereas, SCR T_3 and T_4 are the auxiliary SCRs. C_1 and C_2 are the commutating capacitors. Diodes D_1 and D_2 provide the charging path for the capacitors.

Thyristors T_1 and T_3 forms the first pair for producing the positive alternation, and T_2 and T_4 constitute the second pair for producing the negative alternation of the input a.c. voltage. Figure 8.37 shows the load-voltage waveforms. For the sake of simplicity, circuit operation is described in various operating modes.

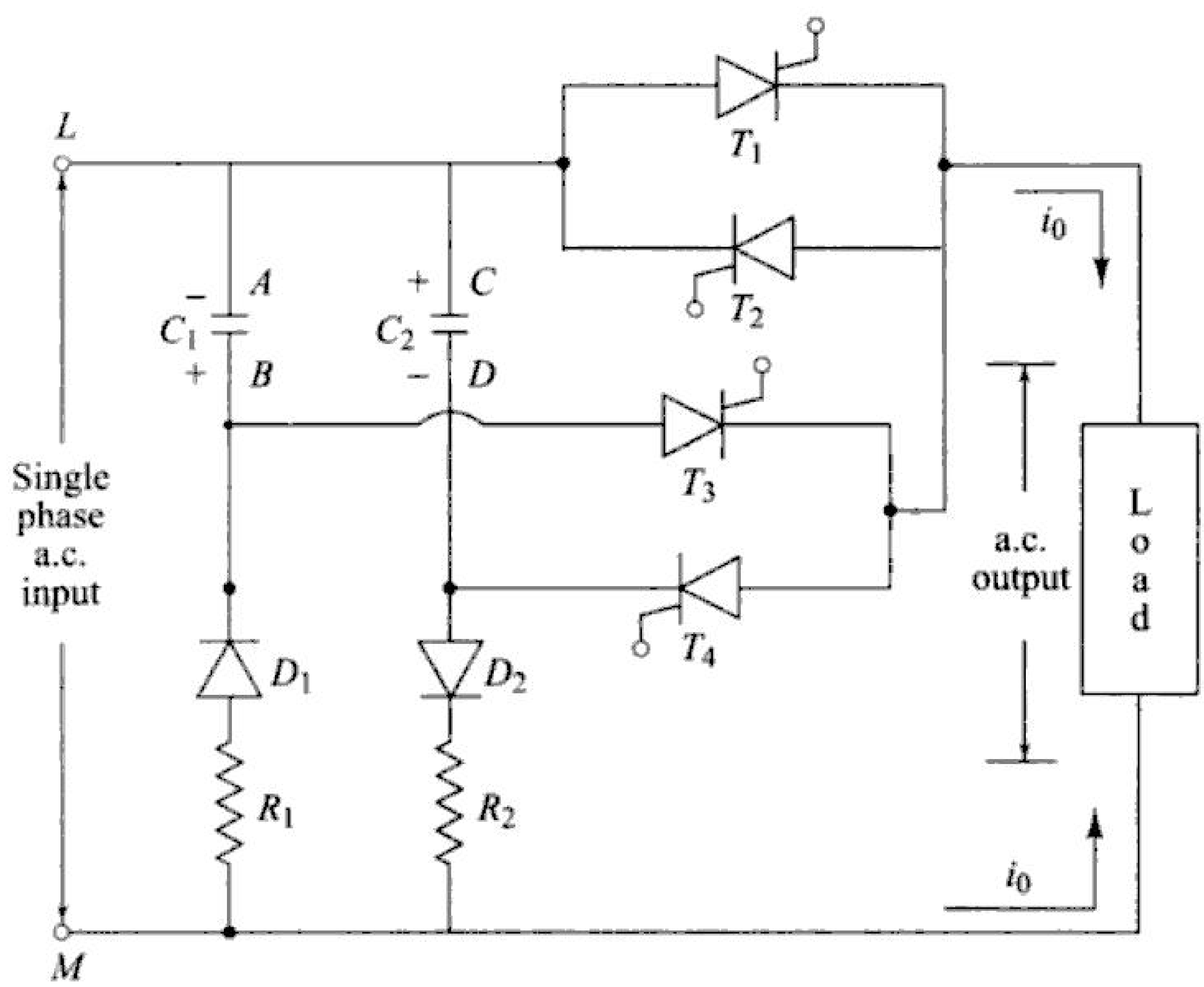


Fig. 8.36 *Single phase a.c. chopper*

(i) Mode 0 operation Initially, during the positive half-cycle of the supply voltage, capacitor C_2 charges through the path $L - C_2 - D_2 - R_2 - M$, with the polarity shown in Fig. 8.36. Similarly, during the negative half-cycle of the supply voltage, capacitor C_1 charges through the path $M - R_1 - D_1 - C_1 - L$, with the polarity shown in Fig. 8.36. The voltage across these capacitors is used for commutation of main SCRs T_1 and T_2.

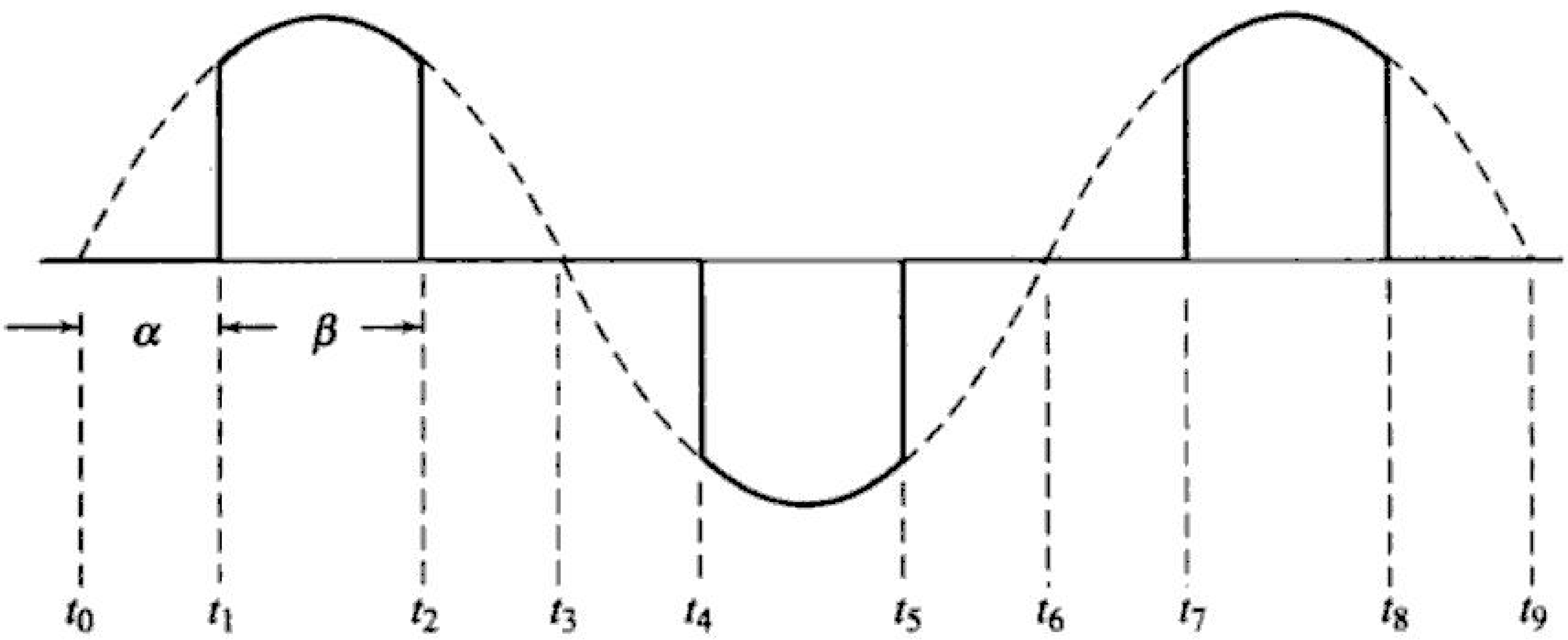


Fig. 8.37 *Load voltage waveform*

(ii) Mode I Operation As shown in Fig. 8.37, during the first positive half-cycle of the supply voltage, thyristor T_1 is triggered at instance t_1 with a firing angle α. The current flows through the path L – SCR T_1 – Load – M. When the instantaneous voltage reaches the instant T_2, auxiliary thyristor T_3 is triggered. As soon as thyristor T_3 is triggered, capacitor C_1 will start discharging through the path $C_B - T_3 - T_1 - C_A$. When the discharging current of capacitor C_1 becomes more than the forward-current of the SCR T_1, SCR T_1 becomes turned-off. The auxiliary SCR T_3 will be automatically turned-off at instant t_3 because of the zero current at this instant. Hence, SCRs T_1 and T_3 forms the first pair for producing the positive alternation of the input a.c. voltage.

(iii) Mode II Operation For the formation of the negative alternation, second pair of thyristors T_2 and T_4 are used. The main SCR T_2 is triggered at the instant t_4, as shown in Fig. 8.37, during the first negative half-cycle of the input voltage. The current flows through the path M – Load – T_2 – L. When the instantaneous voltage reaches the instant t_5, SCR T_4 is triggered. As soon as thyristor T_4 is triggered, capacitor C_2 will start discharging through the path $C_c - T_2 - T_{4(A-K)} - C_D$. When this discharging current is more than the load current, SCR T_2 becomes turned-off. At instant t_6, SCR T_4 is automatically turned-off as the current passing through it becomes zero.

Again at instant t_7, SCR T_1 is triggered to produce the next positive alternation. This is a continuous process and repeated again and again to generate an a.c. voltage across the load. The load power can be changed simply by varying the pulse-width (or conduction angle) β. The main advantage of this type of a.c. chopper is that, whatever the pulse-width β, the fundamental input power factor is always unity. The circuit is generally used for obtaining a regulated a.c. output voltage.

8.10 SOURCE FILTER

A disadvantage of the d.c. to d.c. chopper is that the d.c. supply current is pulsating because of the chopping operation. Therefore, the supply current has harmonics that will produce undesirable effects, such as source voltage fluctuation, signal interference, supply distortion, additional heating and so on. In order to overcome

8.11 MULTIPHASE CHOPPER

A multiphase chopper consists of two or more choppers operating at the same frequency but with a proper phase shift. This type of operation enables the load and power supply to be subjected to an effective frequency which is a multiple of the chopping frequency. As a result, the supply harmonic current is reduced and the ripple amplitude decreases.

The two chopper configuration of Fig. 8.41, is called as two-phase chopper. Similarly, three choppers connected in parallel will constitute a three phase chopper.

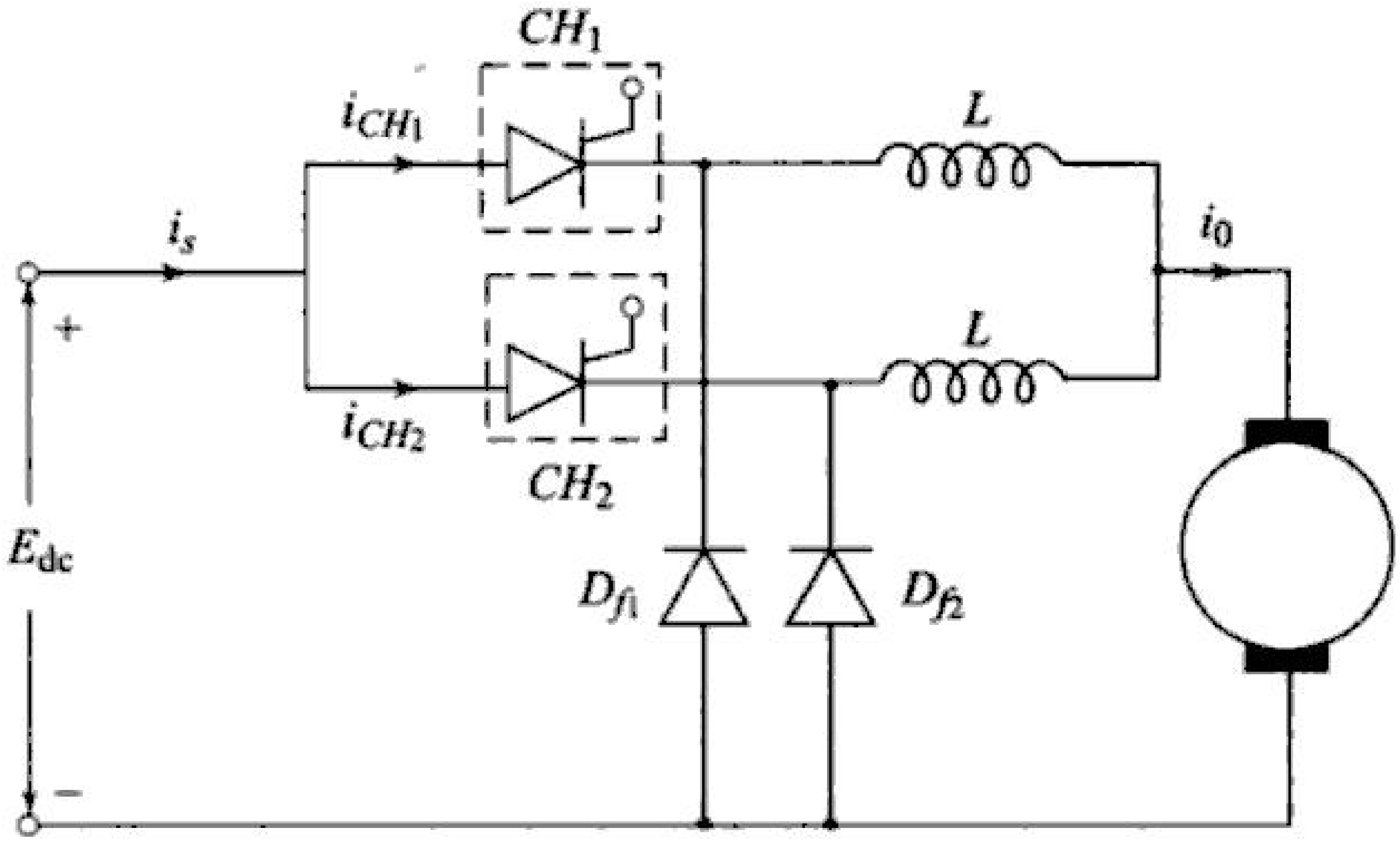


Fig. 8.41 *Two phase chopper*

The main operating modes of the multiphase chopper are
(i) In-phase operating mode and
(ii) Phase shifted operating mode.

In-phase operating mode, all the parallel connected choppers are ON and OFF at the same instant whereas in the phase-shifted operating mode the choppers are ON and OFF at different instants of time. Inductance L in series with each chopper is sufficiently large so that each chopper operates independent of each other.

Figure 8.42(a) shows the input current waveforms for in-phase operation for a duty-cycle of 30%. The load current I_0 be assumed to be ripple free. As shown in the figure, both choppers CH_1 and CH_2 are

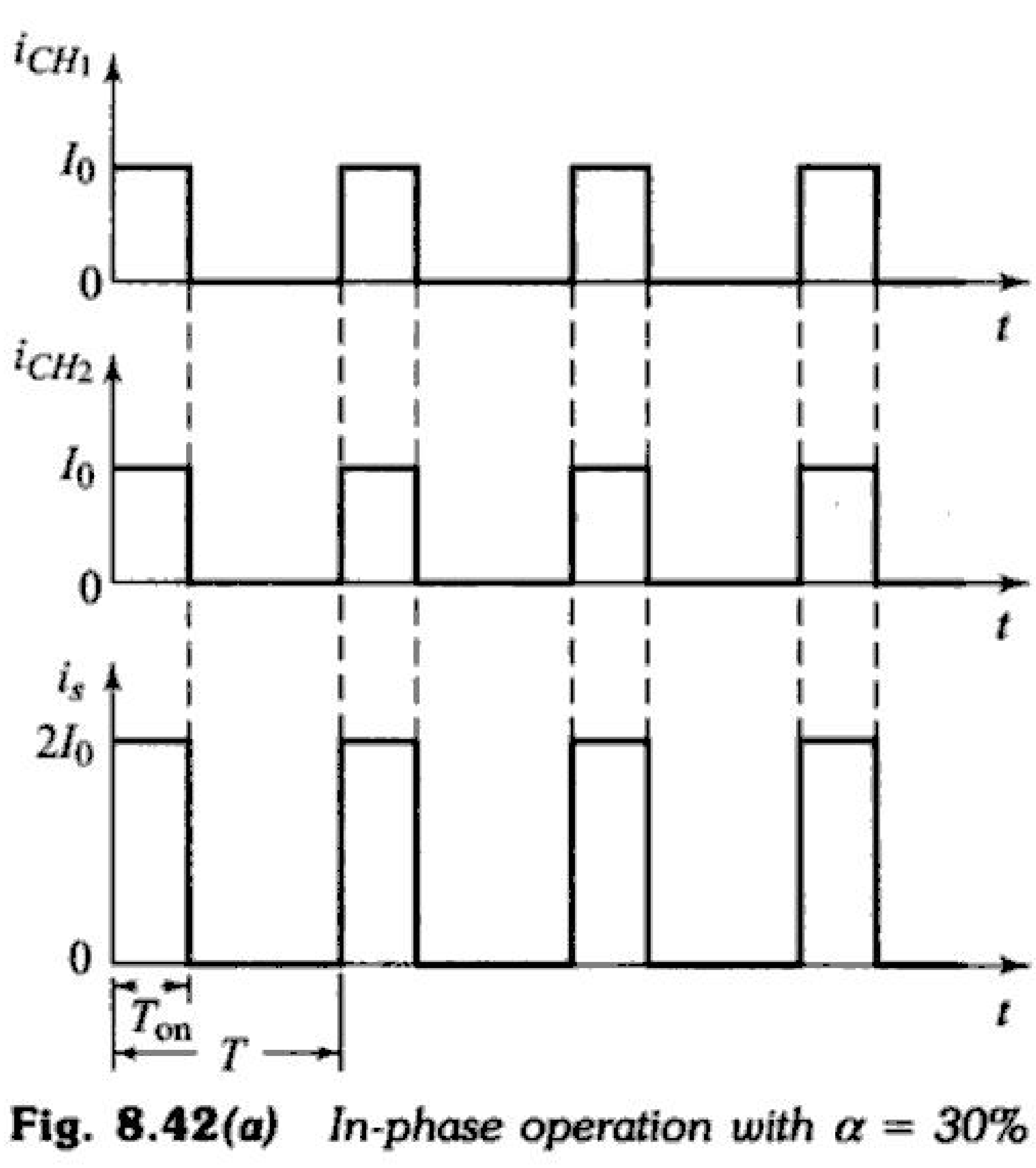


Fig. 8.42(a) *In-phase operation with α = 30%*

containing a pedestal of half the load current as shown in Fig. 8.42(c).

A multiphase chopper is used where load-current requirement is large. The main advantage of the multiphase-chopper over a single chopper is that its input current has reduced ripple amplitude and increased ripple frequency. As a consequence of it, size for filter for a multiphase chopper is reduced.

The main disadvantages of this chopper circuit are–

(i) additional external inductors are required
(ii) need for the additional motor connections
(iii) need for the additional commutating components
(iv) need for additional complexity in the control logic.

8.12 FLYBACK CONVERTERS [SWITCHING REGULATORS]

D.C.–D.C. converters are widely used in regulated switch-mode d.c. power supplies and in d.c. motor drive applications. Often, the input to these converters is an unregulated d.c. voltage, which is obtained by rectifying the line voltage and therefore, it will fluctuate due to changes in the line voltage magnitude. Switch-mode, d.c.-to-d.c. converters are used to convert the unregulated d.c. input into a controlled d.c. output at a desired voltage level.

The following d.c.–d.c. converters are discussed in this section:

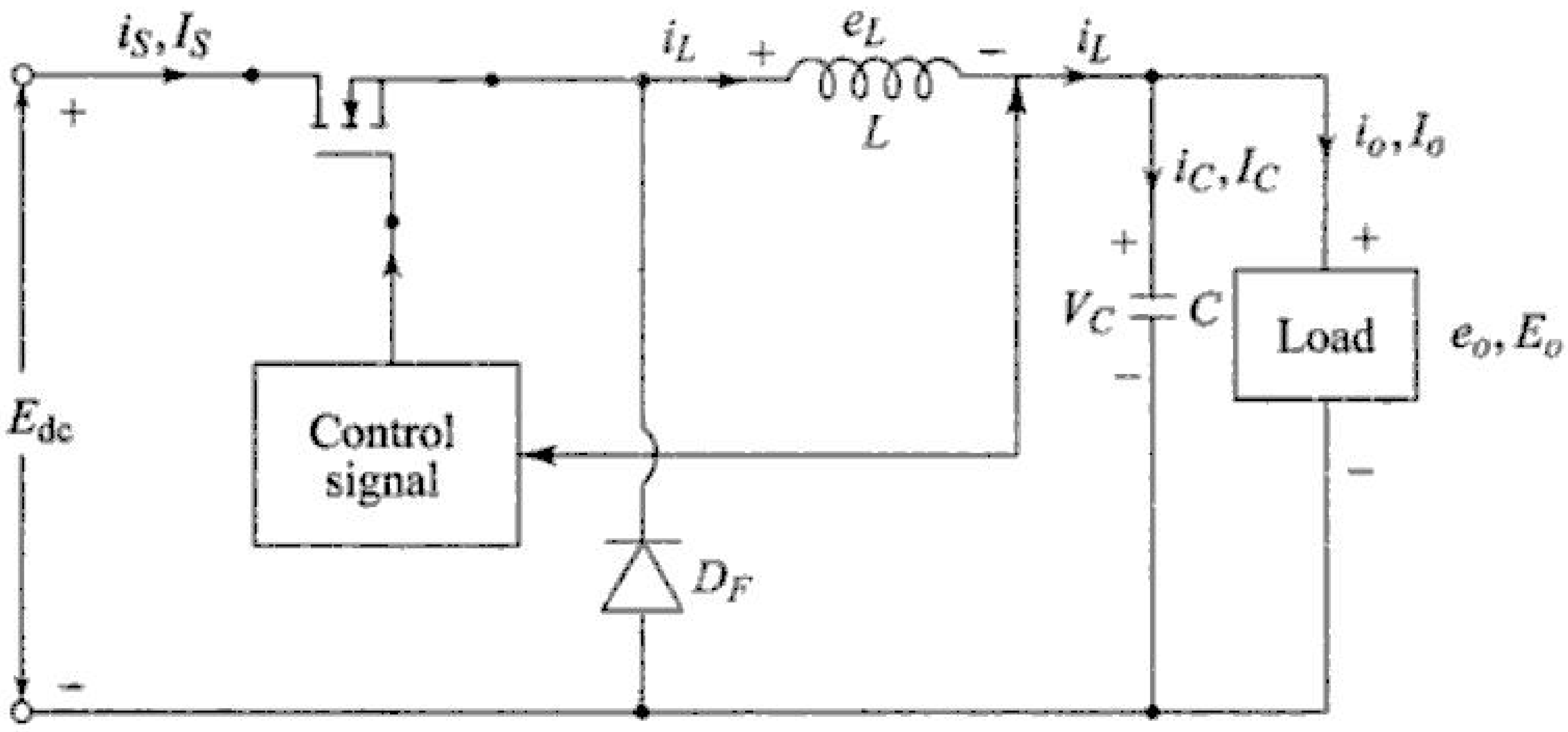
1. Buck (step-down) converter.
2. Boost (step-up) converter.
3. Buck-Boost (step-down/up) converter.
4. Cuk converter.

Of these four converters, only the step-down and step-up are the basic converter topologies. Both the buck-boost and the cuk converters are combinations of the two basic topologies. The name "flyback converter" is descriptive of the inductive energy flyback action typically encountered in this type of converter operation.

8.12.1 Buck (Step-down) Converter

Figure 8.43(a) shows the power diagram of a buck converter using a power MOSFET. As the name implies, a step-down (buck) converter produces a lower average output voltage E_0 than the d.c. input voltage E_{dc}. By varying the duty-ratio T_{on}/T of the switch, the average output voltage can be controlled. The associated voltage and current waveforms for a continuous current flow in the inductor L is shown in Fig. 8.43(b).

As shown in Fig. 8.43(b), device T_1 is switched ON at time $t = 0$. The supply current, which rises, flows through the path filter inductor L, filter capacitor C, and load. Therefore, the inductor stores the energy during the T_{on} period. During the interval when the device is ON, the diode in Fig. 8.43(a) becomes reverse biased and the input provides energy to the load as well as to the inductor. Now, at instant $t = T_{on}$, device T_1 is switched OFF. During the interval when the device is OFF, the inductor current flows through L, C, load, and freewheeling diode D_F and hence diode D_F conducts. The output voltage fluctuations are very much



(a) Power diagram

Fig. 8.43(*a*)

diminished, using a low-pass filter, consisting of an inductor and a capacitor. The corner frequency f_c of this low-pass filter is selected to be much lower than the switching frequency, thus essentially dominating the switching frequency ripple in the output voltage. Depending on the switching frequency, filter inductance, and capacitance the inductor current could be discontinuous.

In general, the voltage across the inductor L is given by

$$e_L = L\frac{di}{dt}$$

In time T_{on}, assuming that the inductor current rises linearly from I_1 to I_2, we can write,

$$\therefore \qquad E_{dc} - E_0 = L\left(\frac{I_2 - I_1}{T_{on}}\right) \tag{8.133}$$

Let us define, the change in current as

$\Delta I = I_2 - I_1$ (i.e. peak-to-peak ripple current of L)

$\therefore$ Equation (8.133) becomes

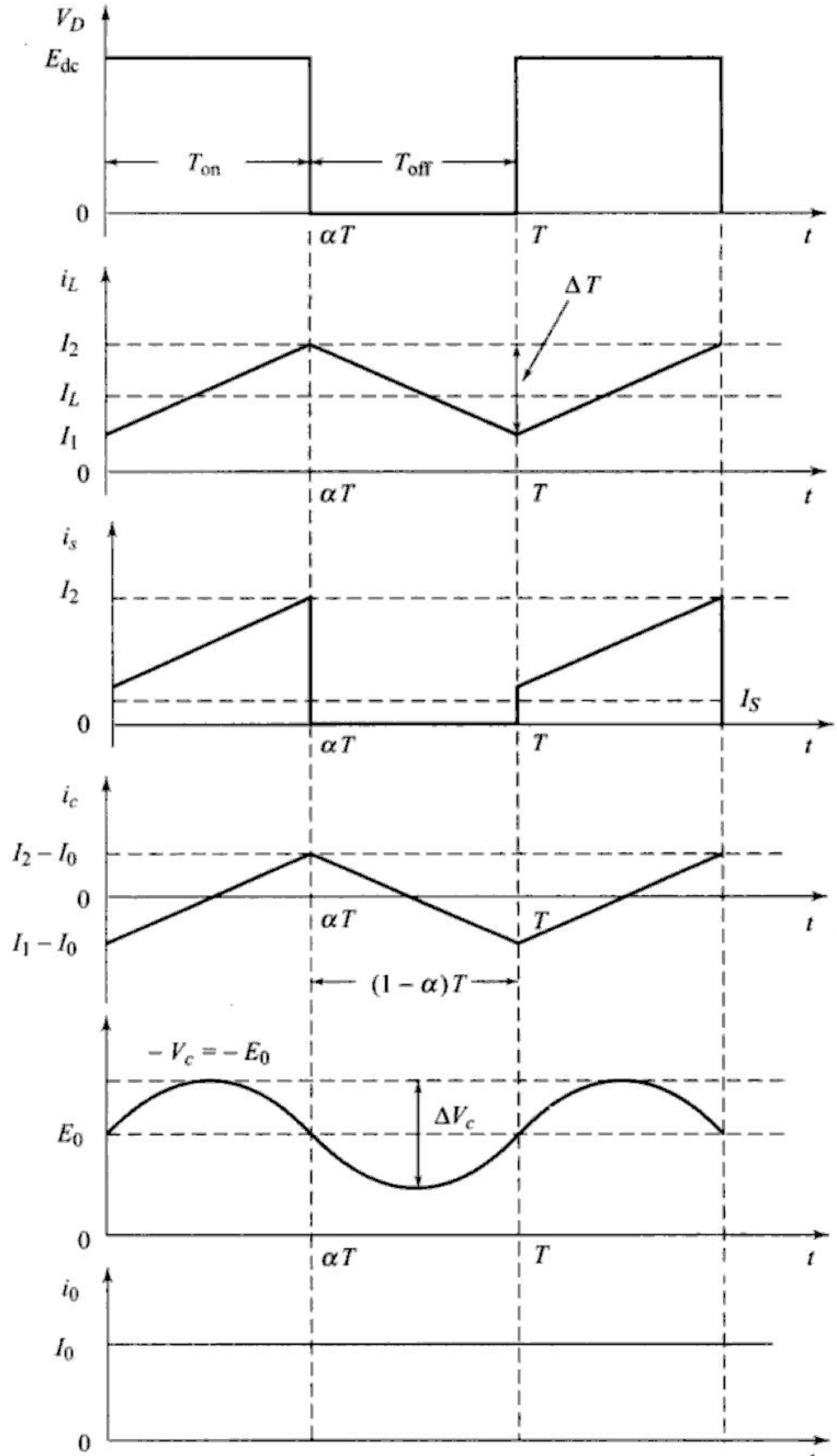
$$E_{dc} - E_0 = \frac{\Delta I \cdot L}{T_{on}} \tag{8.134}$$

or,

$$T_{on} = \frac{\Delta I \cdot L}{E_{dc} - E_0} \tag{8.135}$$

As shown in Fig. 8.43(b), during time T_{off}, inductor current falls linearly from I_2 to I_1,

$$-E_0 = -L\frac{\Delta I}{T_{off}} \tag{8.136}$$



(b) Voltage and current waveform

Fig. 8.43(b) *Buck-chopper with continuous i_L*

We can write the inductor current i_L by applying Kirchhoff's current law as,

$$i_L = i_C + i_O$$

By assuming that the load ripple current Δi_O is very small and therefore, neglected, we can write the above equation as

$$\Delta i_L = \Delta i_C$$

The average capacitor current, which flows into for $T_{on}/2 + T_{off}/2 = T/2$, is

$$I_C = \frac{\Delta I}{4}$$

Now, the capacitor voltage is expressed as

$$V_c = \frac{1}{C}\int i_C \, dt + V_c(t=0)$$

and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C}\int_0^{t/2} \frac{\Delta I}{4} dt$$

$$= \frac{\Delta I \cdot T}{8C} = \frac{\Delta I}{8 f_c} \quad (8.145)$$

Substituting the value of ΔI from Eq. (8.143) or (8.144) in Eq. (8.145) yields

$$\Delta V_c = \frac{E_0 \cdot (E_{dc} - E_0)}{8LCf^2 E_{dc}} \quad (8.146)$$

or

$$\Delta V_c = \frac{E_{dc}\alpha(1-\alpha)}{8LCf^2} \quad (8.147)$$

Since the buck chopper circuit requires only one transistor, it is a simple one and has high efficiency, greater than 90%. The inductor L limits the di/dt of the load-current. This type of chopper circuit provides one polarity of output voltage and unidirectional output current. In case of possible short circuit across the diode path, it requires a protection circuitry. Its main application is in regulated d.c. power supplies and d.c. motor speed control.

SOLVED EXAMPLES

Example 8.23 The buck-converter in Fig. 8.43 has an input voltage of $E_{dc} = 14$ V. The required average output voltage is $E_0 = 6$ V and the peak-to-peak output ripple voltage is 15 mV. The switching frequency is 30 kHz. If the peak-to-peak ripple curent of inductor is limited to 0.6 A. Determine: (a) the duty cycle α, (b) the filter inductance L, and (c) the filter capacitor C.

Solution:

Given: $E_{dc} = 14$ V, $E_0 = 6$ V, $\Delta VC = 15$ mV, $\Delta I = 0.6$ A, $f = 30$ kHz

(a) From Eq. (8.138), duty-cycle α is given by

$$\alpha = \frac{E_0}{E_{dc}} = \frac{6}{14} = 0.4285 = 42.85\%$$

(b) Now, from Eq. (8.143), we can write,

$$L = \frac{E_0(E_{dc} - E_0)}{f \cdot E_{dc} \cdot \Delta I} = \frac{6(14-6)}{30 \times 10^3 \times 14 \times 0.6} = 190.48\ \mu\text{H}$$

(c) From Eq. (8.145), we have

$$C = \frac{\Delta I}{8 \times f \times \Delta V_C} = \frac{0{\cdot}6}{8 \times 30 \times 10^3 \times 15 \times 10^{-3}} = 166.67\ \mu\text{F}.$$

Example 8.24 A buck converter operating at 50 kHz is fed from a 12 V battery and supplies 5 V to load. Neglecting switch and device-losses, determine:

(a) The maximum on-period of MOSFET switch given that battery voltage varies from 13.5 V in fully charged state to 10 V at the end of discharge.
(b) Battery drain current under nominal condition with 10 Amp. load.
(c) The value of choke required to maintain continuous current operation for a ripple current of 500 mA and worst case battery voltage conditions.

Solution:

Given: $E_o = 5$ V, $E_{dc_{max}} = 13.5$, $E_{dc_{min}} = 10$ V, $I_o = 10$ A, $\Delta I = 500$ mA

(a) From Eq. (8.138), $\alpha = \dfrac{E_o}{E_{dc}} \quad \therefore \dfrac{T_{on}}{T} = \dfrac{E_o}{E_{dc}}$

$$\therefore \quad t_{on(max)} = \frac{E_o}{E_{dc_{min}} \cdot f} = \frac{5}{10 \times 50 \times 10^3} = 10\ \mu$$

$\therefore$ Maximum period of conduction for switch = 10 μ sec.

(b) If the switch and device losses are neglected, then output power will be equal to input power, i.e.

$$E_{dc} \cdot I_s = E_0 \cdot I_0 \quad \therefore 12 \times I_s = 5 \times 10 \quad \therefore I_s = 4.16\text{ A}$$

(c) From Eq. 8.143, $L = \dfrac{5(10-5)}{50 \times 10^3 \times 10 \times 500 \times 10^{-3}} = 100\ \mu\text{H}$

8.12.2 Boost (Step-up) Converter

Figure 8.44(a) shows the circuit diagram of a boost chopper using a power MOSFET. As the name implies, the output voltage is always greater than the input voltage. When the power device is ON, the inductor L is connected to the supply E_{dc}, and inductor stores energy during on-period, T_{on}. Hence, diode D_F is reverse biased and isolates the output stage. When the power device is OFF, the output stage receives energy from the inductor as well as from the input. The current which was flowing through the transistor would now flow through L, D_F, C and load. The associated voltage and current waveforms are shown in Fig. 8.44(b).

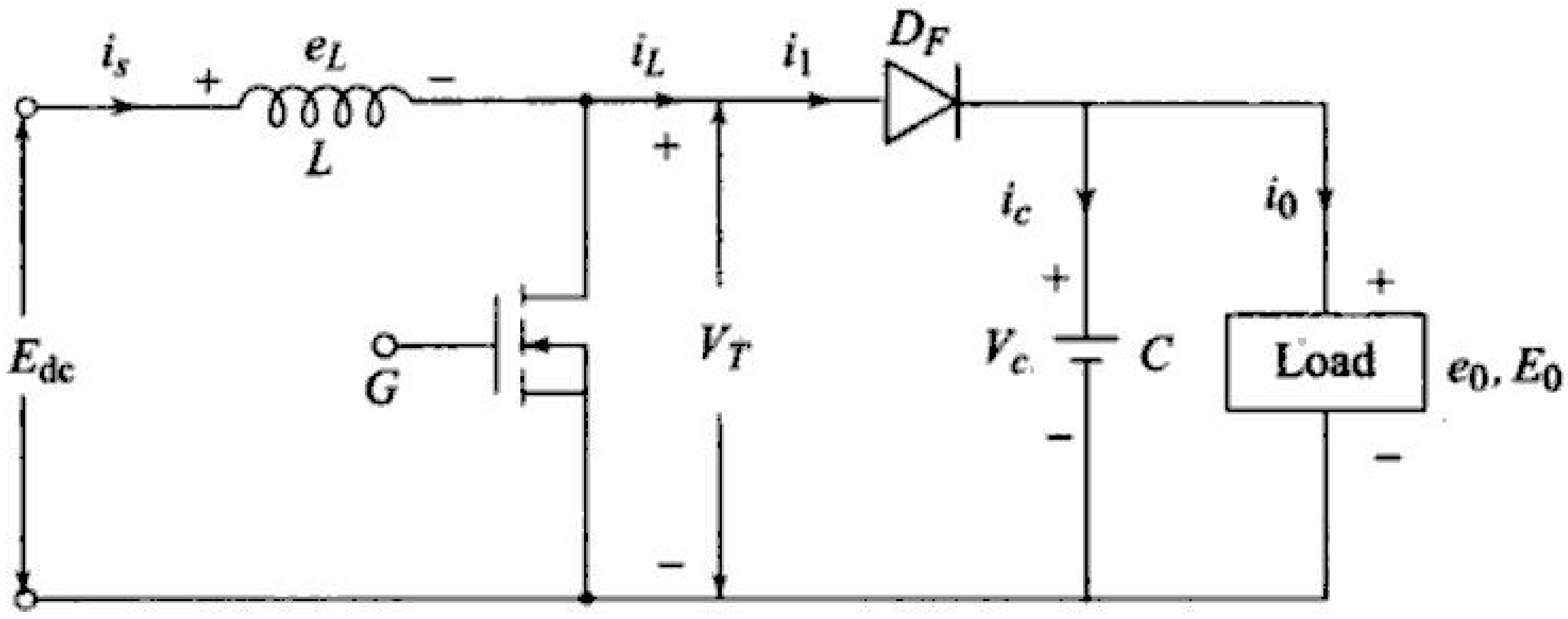


Fig. 8.44(a) *Circuit diagram*

During T_{on}, by assuming that the inductor current rises linearly from I_1 to I_2, we can write,

$$E_{dc} = L\frac{(I_2 - I_1)}{T_{on}} = L\frac{\Delta I}{T_{on}} \tag{8.148}$$

or
$$T_{on} = \frac{\Delta I \cdot L}{E_{dc}} \tag{8.149}$$

During time T_{off}, the inductor current falls linearly from I_2 to I_1, therefore, we can write,

$$E_{dc} - E_0 = -L \cdot \frac{\Delta I}{T_{off}} \tag{8.150}$$

or
$$T_{off} = \frac{\Delta I \cdot L}{E_0 - E_{dc}} \tag{8.151}$$

From Eqs (8.148) and (8.150), the peak-to-peak ripple current of inductor L can be written as,

$$\Delta I = \frac{E_{dc} \cdot T_{on}}{L} = \frac{(E_0 - E_{dc})T_{off}}{L} \tag{8.152(a)}$$

Substituting $T_{on} = \alpha T$ and $T_{off} = (1 - \alpha)T$, yields the average output voltage,

$$E_0 = E_{dc} \cdot \frac{T}{T_{off}} = \frac{E_{dc}}{1-\alpha} \tag{8.152(b)}$$

Assuming a lossless circuit, $P_i = P_o$.

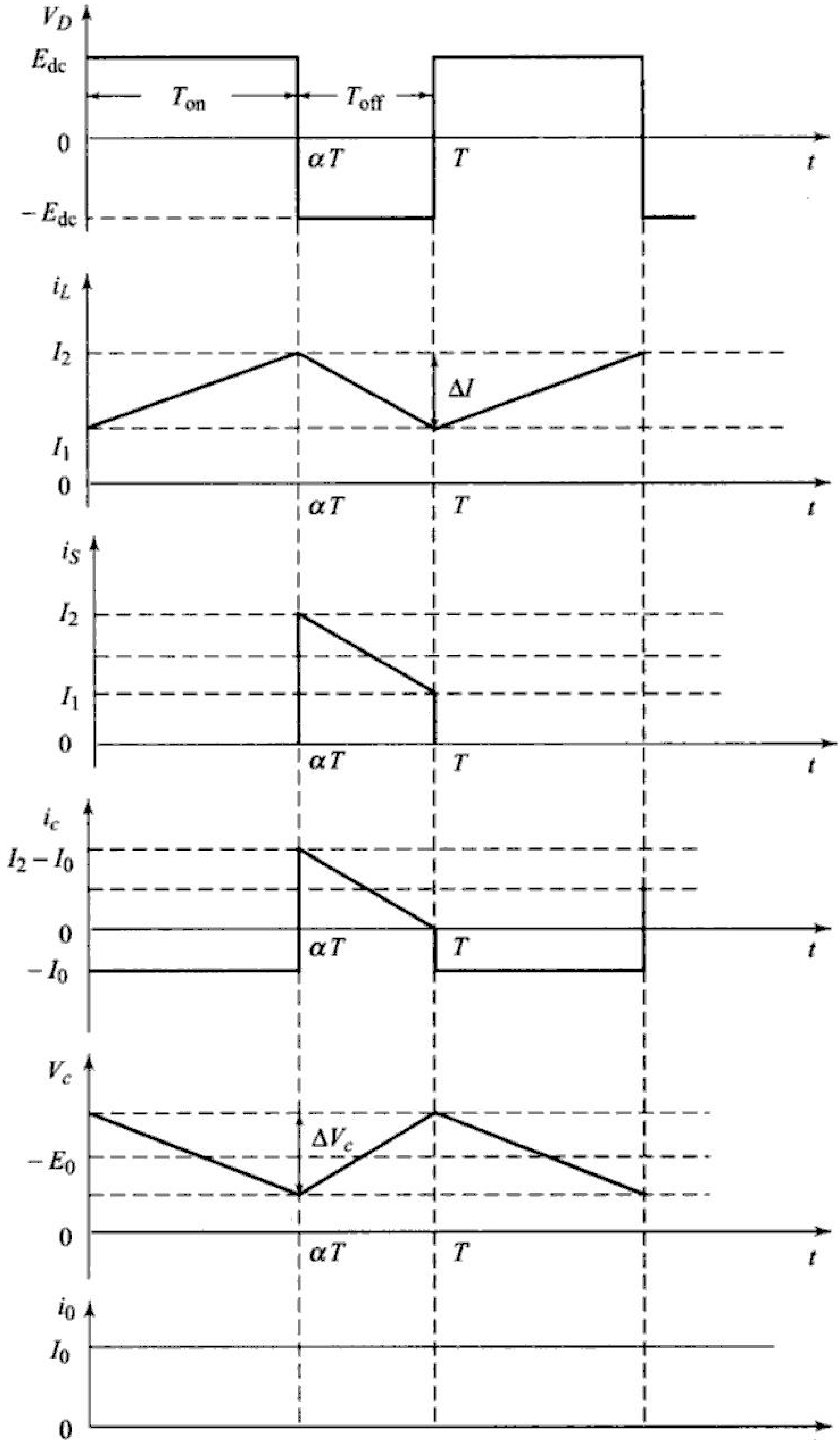
$$\therefore \quad E_{dc} \cdot I_s = E_0\, I_0 = \frac{E_{dc} I_0}{(1-\alpha)}$$

Therefore, the average input current becomes

$$I_s = \frac{I_0}{1-\alpha} \tag{8.153}$$

Now, the switching period T can be obtained as

$$T = \frac{1}{f} = T_{on} + T_{off} = \frac{\Delta I \cdot L}{E_{dc}} + \frac{\Delta I \cdot L}{E_0 - E_{dc}} = \frac{\Delta I \cdot L \cdot E_0}{E_{dc}(E_0 - E_{dc})} \tag{8.154}$$



Voltage and current waveform

Fig 8.45(b) *Buck-boost converter with continuous i_L*

When the power MOSFET is switched OFF, the inductor current tends to decrease and as a result, the polarity of the emf induced in L is reversed as shown in Fig. 8.45(a). Thus, the inductance energy discharges in the load through the path L_+ – Load – D – L_-.

During time T_{on}, by assuming that the inductor current rises linearly from I_1 to I_2, we can write, $E_{dc} = L \cdot \frac{I_2 - I_1}{T_{on}} = L \cdot \frac{\Delta I}{T_{on}}$ (8.161)

or, $$T_{on} = \frac{\Delta IL}{E_{dc}} \quad (8.162)$$

Now, during time T_{off}, the inductor current falls linearly from I_2 to I_1, therefore, we can write

$$E_0 = -L \cdot \frac{\Delta I}{T_{off}} \quad (8.163)$$

or $$T_{off} = \frac{-\Delta I \cdot L}{E_0} \quad (8.164)$$

where the peak-to-peak ripple current of inductor L is given by

$$\Delta I = I_2 - I_1$$

From Eqs (8.161) and (8.163), we can write,

$$\Delta I = \frac{E_{dc} \cdot T_{on}}{L} = \frac{-E_0 \cdot T_{off}}{L}$$

or $$E_0 = -E_{dc} \cdot \frac{T_{on}}{T_{off}} = -E_{dc} \cdot \frac{T_{on}/T}{T_{off}/T} = \frac{-E_{dc} \cdot \alpha}{(T - T_{on})/T}$$

or $$E_0 = -E_{dc} \cdot \frac{\alpha}{(1-\alpha)} \quad (8.165)$$

For a lossless system, in a steady-state,

$$E_{dc} \cdot I_s = -E_0 \cdot I_0 \text{ or } E_{dc}\, I_s = E_{dc} \cdot \frac{\alpha}{1-\alpha} I_0$$

Therefore, the average input current is given by

$$I_s = \frac{\alpha}{1-\alpha} I_0 \quad (8.166)$$

Now, the switching period, T, can be calculated as

$$T = \frac{1}{f} = T_{on} + T_{off}$$

Substituting the values of T_{on} and T_{off} from Eqs (8.162) and (8.164), we get

$$T = \frac{\Delta IL}{E_{dc}} - \frac{\Delta I \cdot L}{E_0} = \frac{\Delta IL(E_0 - E_{dc})}{E_{dc} \cdot E_0} \tag{8.167}$$

From Eq. (8.167), the peak-to-peak ripple current can be written as

$$\Delta I = \frac{E_{dc} \cdot E_0}{f \cdot L \cdot (E_0 - E_{dc})} \tag{8.168}$$

or

$$\Delta I = \frac{E_{dc} \cdot \alpha}{f \cdot L} \tag{8.169}$$

During the period T_{on}, when the device is ON, the filter-capacitor supplies the load current. Therefore, the average discharging current of the capacitor is $I_C = I_0$.

Also, the peak-to-peak ripple voltage of the capacitor is given by

$$\Delta V_C = \frac{1}{C}\int_0^{T_{on}} I_C \mathrm{d}t = \frac{1}{C}\int_0^{T_{on}} I_0 \mathrm{d}t = \frac{I_0 \cdot T_{on}}{C} \tag{8.170}$$

From Eq. (8.165), we can write, $E_0(1 - \alpha) = -E_{dc} \cdot \alpha$, $E_0 = \alpha(E_0 - E_{dc})$

or

$$E_0 = \frac{T_{on}}{T}(E_0 - E_{dc}), \text{ or } T_{on} = \frac{E_0}{(E_0 - E_{dc})f}$$

Substituting the above value of T_{on} in Eq. (8.170), we get

$$\Delta V_C = \frac{I_0 \cdot E_0}{(E_0 - E_{dc})f \cdot C} \tag{8.171}$$

or

$$\Delta V_C = \frac{I_0 \cdot \alpha}{f \cdot C} \tag{8.172}$$

From Eq. (8.165), it becomes clear that the buck-boost converter provides output voltage polarity reversal without a transformer. This type of chopper has a high efficiency. The inductor L limits the $\mathrm{d}i/\mathrm{d}t$ of the fault current when the device is under the fault condition. In this type of converter circuit, the output short circuit protection would be easy to implement.

Example 8.26 Consider the buck-boost converter of Fig. 8.45. The input voltage to this converter is $E_{dc} = 14$ V. The duty cycle $\alpha = 0.6$ and the switching frequency is 25 kHz. The inductance $L = 180$ μH and filter capacitance $C = 220$ μF. The average load current $I_0 = 1.5$ A. Compute:

(a) the average output voltage, E_0;
(b) the peak-to-peak output voltage ripple, ΔV_c;
(c) the peak-to-peak current of inductor, ΔI; and
(d) the peak current of the device I_p.

Solution:

(a) From Eq. (8.165), $E_0 = -\dfrac{14 \times 0.6}{1-0.6} = -21$ V.

(b) From Eq. (8.172), peak-to-peak output ripple voltage is

$$\Delta V_c = \frac{1.5 \times 0.6}{25 \times 10^3 \times 220 \times 10^{-6}} = 0.16 \text{ V.}$$

(c) From Eq. (8.169), the peak-to-peak inductor ripple is

$$\Delta I = \frac{14 \times 0.6}{25 \times 10^3 \times 180 \times 10^{-6}} = 1.87 \text{ A}$$

(d) From Eq. (8.166),

$$I_s = \frac{0.6 \times 1.5}{1-0.6} = 2.25 \text{ A}$$

Now, since the average input current I_s is the average of duration $\alpha \cdot T$, the peak-to-peak current of the MOSFET is given by

$$I_p = \frac{I_s}{\alpha} + \frac{\Delta I}{2} = \frac{2.25}{0.6} + \frac{1.87}{2} = 4.69 \text{ A}$$

Example 8.27 A buck-boost converter is operated from a 24 V battery and supplies an average load current of 2 Amp. Its switching frequency is 50 kHz. Neglecting diode and switch drop, determine

(a) Range of duty-cycle variation required to maintain the output voltage at 15 V, given that the battery voltage ranges from 26 V in the fully charged state to 21 V in the discharged state.

(b) The peak to peak choke ripple current for the nominal supply voltage, given that the choke value is 500 μH.

(c) Average supply current drawn from the battery under nominal condition.

Solution:

(a) From Eq. (8.165),

(i) when $E_{dc} = 26$ V, $\dfrac{E_o}{E_{dc}} = \dfrac{\alpha}{1-\alpha}$

$$\therefore \quad \frac{15}{26} = \frac{\alpha}{1-\alpha} \quad \therefore \alpha = 0.366$$

(ii) When $E_{dc} = 21$ V

$$\therefore \quad \frac{15}{21} = \frac{\alpha}{1-\alpha}, \quad \therefore \alpha = 0.417$$

$\therefore$ Duty cycle varies from 0.366 to 0.417

(b) Nominal supply voltage = 24 V

we have, $\dfrac{E_o}{E_{dc}} = \dfrac{\alpha}{1-\alpha}, \dfrac{15}{24} = \dfrac{\alpha}{1-\alpha}, \quad \therefore \alpha = 0.385$

From (8.169),

$$\Delta I = \frac{24 \times 0.385}{50 \times 10^3 \times 500 \times 10^{-6}} = 0.3696 \text{ A} \quad = \Delta I = 369.6 \text{ mA}$$

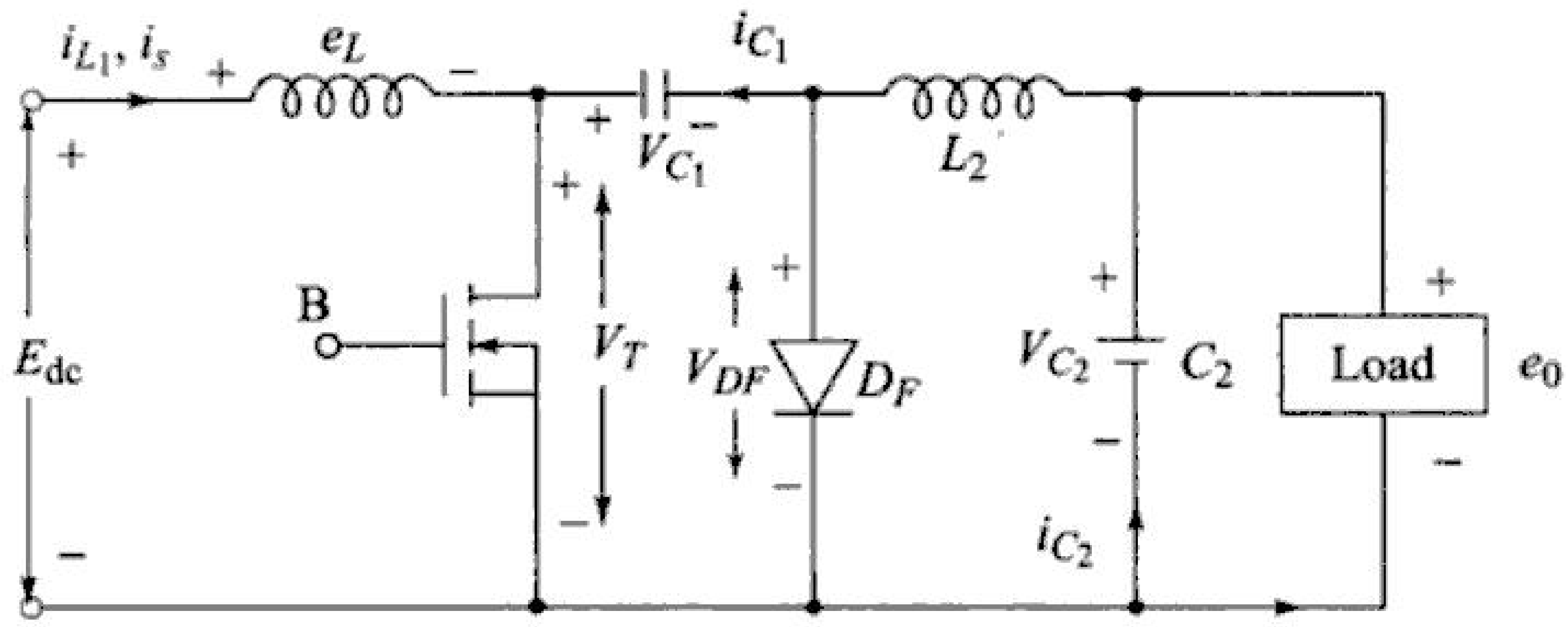
(c) Assuming switch and the device losses to be zero,

∴ Power supplied by the battery = Load power

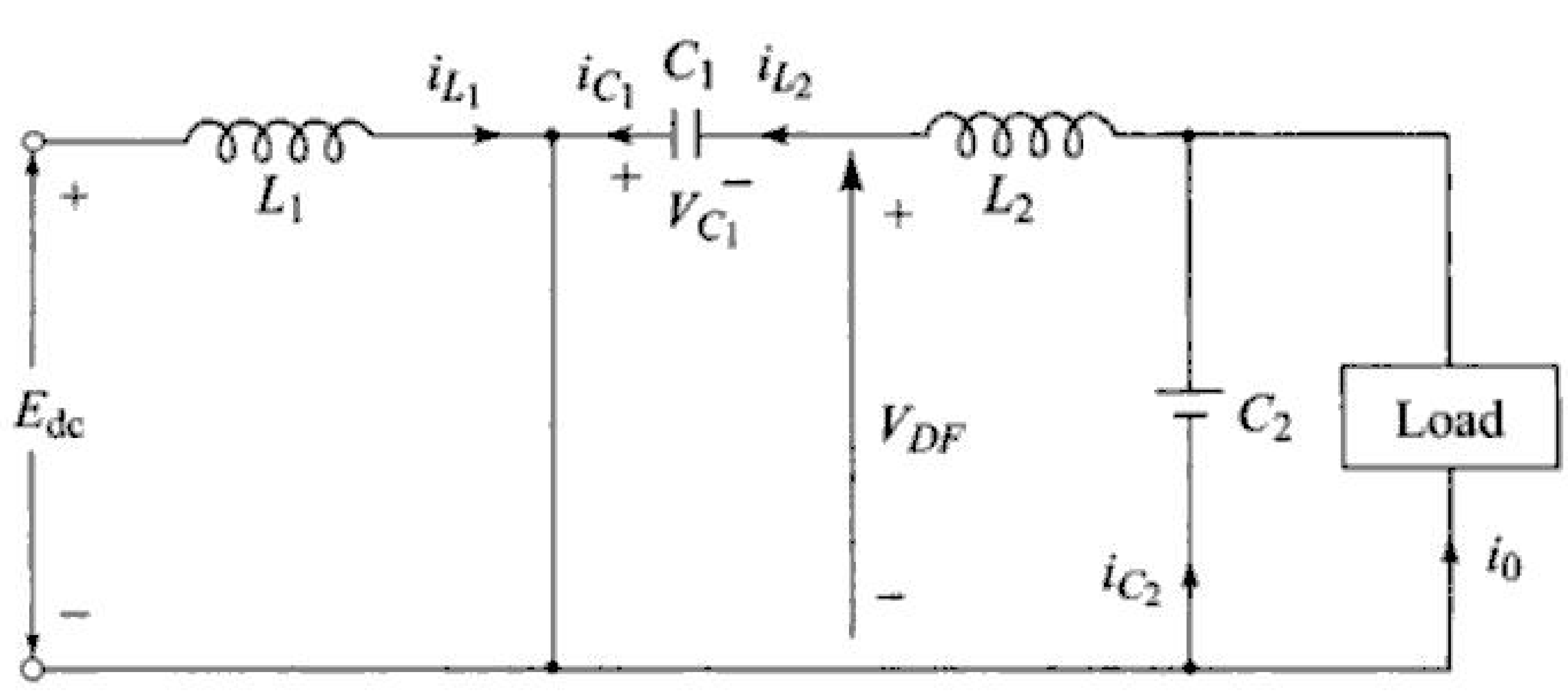
$$24 \times I_s = 15 \times 2, \quad \therefore I_s = 1.25 \text{ Amp.}$$

8.12.4 Cuk Converter

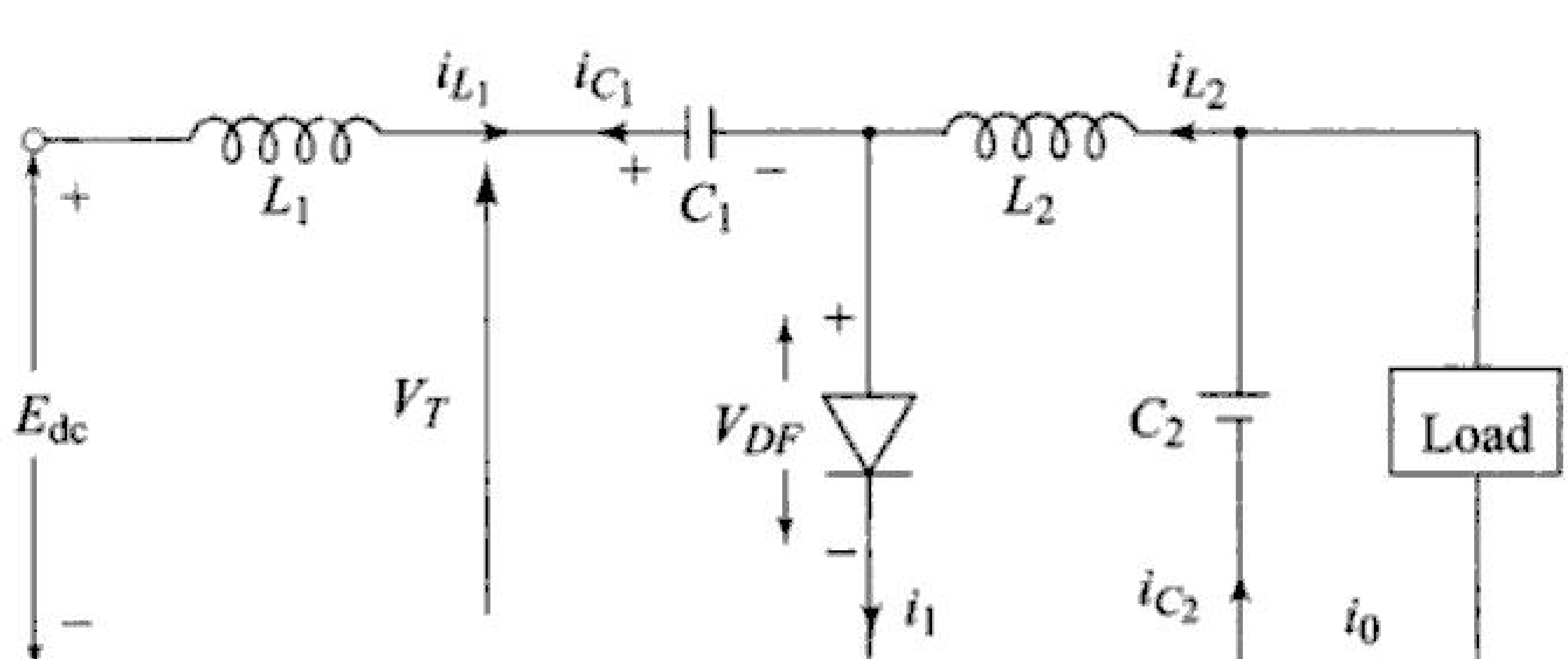
Figure 8.46(a) shows a Cuk converter, after the name of the inventor. The key difference between this converter and the previously discussed converters, from the operation point of view, is that a capacitor, rather than an inductor, is used for



(a) Circuit diagram



(i) Switch-on condition



(ii) Switch-off condition

(b) Equivalent circuits

Fig. 8.46(a) and (b)

energy storage and transfer to accomplish power transformation. From this point of view, the Cuk converter is a capacitive energy flyback converter. In fact, the Cuk converter and the buck-boost converter are electrically duals of each other. The point connected MOSFET-inductor-diode combination is replaced by the dual, serially connected diode-capacitor-MOSFET combination. Similar to the buck-boost converter, the Cuk converter provides an output voltage which is less than or greater than the input voltage but the output voltage polarity is opposite to that of the input voltage.

When the input voltage is applied to the circuit and the MOSFET T_1 is switched-off, the inductor currents i_{L_1} and i_{L_2} flow through the diode D_F. The equivalent circuit is shown in Fig. 8.46(b). Therefore, capacitor C_1 is charged through L_1, D_F and the input supply E_{dc}. Current i_{L_1} decreases, because V_{C_1} is larger that E_{dc}.

Energy stored in inductor L_2 feeds the output. Therefore, current i_{L_2} also decreases.

Now, when the power MOSFET is ON, capacitor voltage V_{C_1} reverse biases the diode D_F and turns it OFF. The inductor currents i_{L_1} and i_{L_2} flow through the device as shown in Fig. 8.46(b). Since $V_{C_1} > E_{dc}$, C_1 discharges through the device, transferring energy to the output and L_2, therefore i_{L_1} increases. The input feeds energy to L_1 causing i_{L_1} to increase. The waveforms for steady-state voltages and currents are shown in Fig. 8.46(c) for a continuous load current.

During time T_{on}, by assuming that the current of inductor L_1 rises linearly from $I_{L_{11}}$ to $I_{L_{12}}$, we can write

$$E_{dc} = L_1 \cdot \frac{I_{L_{12}} - I_{L_{11}}}{T_{on}} = L_1 \cdot \frac{\Delta I_1}{E_{dc}} \tag{8.173}$$

or

$$T_{on} = \frac{\Delta I_1 \cdot L_1}{E_{dc}} \tag{8.174}$$

During time T_{off}, the current of inductor L_1 falls linearly from $I_{L_{12}}$ to $I_{L_{11}}$ due to the charged capacitor C_1.

$$\therefore \quad E_{dc} - V_{C_1} = -L_1 \cdot \frac{\Delta I_1}{T_{off}} \tag{8.175}$$

or

$$T_{off} = \frac{-\Delta I_1 \cdot L_1}{E_{dc} - V_{C_1}} \tag{8.176}$$

where V_C is the average value of capacitor C_1, and

$$\Delta I_1 = I_{L_{12}} - I_{L_{11}}$$

From Eqs (8.173) and (8.175), we can write

$$\Delta I_1 = \frac{E_{dc} \cdot T_{on}}{L_1} = \frac{-(E_{dc} - V_{C_1})}{L_1} T_{off}$$

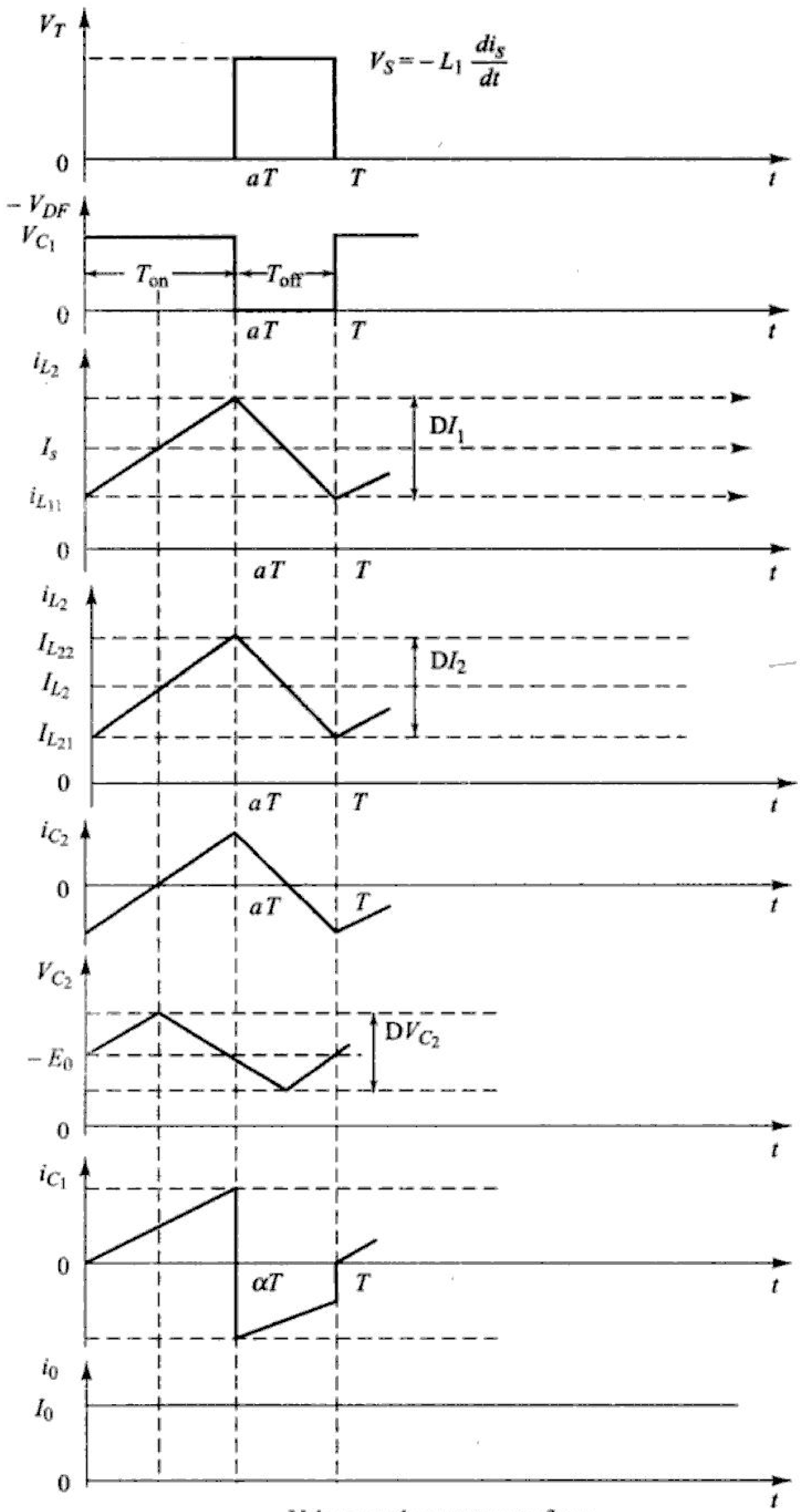
or

$$E_{dc}\, T_{on} = -E_{dc}\, T_{off} + V_{C_1}\, T_{off}$$

$$E_{dc}\,(T_{on} + T_{off}) = V_{C_1} T_{off}$$

or

$$V_{C_1} = \frac{E_{dc} \cdot T}{T_{off}} = \frac{E_{dc}}{1-\alpha} \tag{8.177}$$



Voltage and current waveform

Fig. 8.46(c) *Cuk converter*

Also, during time T_{on}, by assuming that the current of filter inductor L_2 rises linearly from $I_{L_{21}}$ to $I_{L_{22}}$, we get

$$V_{C_1} + E_0 = L_2 \cdot \frac{I_{L_{22}} - I_{L_{21}}}{T_{on}} = L_2 \cdot \frac{\Delta I_2}{T_{on}} \tag{8.178}$$

or
$$T_{on} = \frac{\Delta I_2 \, L_2}{V_{C_1} + E_0} \tag{8.179}$$

Also, during time T_{off}, current of inductor L_2 falls linearly from $I_{L_{22}}$ to $I_{L_{21}}$,

therefore, $E_0 = -L_2 \dfrac{\Delta I_2}{T_{off}}$ (8.180)

or
$$T_{off} = -\frac{\Delta I_2 L_2}{E_0} \tag{8.181}$$

where $\Delta I_2 = I_{L_{22}} - I_{L_{21}}$.

Now, from Eqs (8.178) and (8.180), we can write

$$\Delta I_2 = \frac{(V_{C_1} + E_0)T_{on}}{L_2} - \frac{E_0 \cdot T_{off}}{L_2}$$

$$V_{C_1} T_{on} = -E_0 \, T_{off} - E_0 \, T_{on}$$

$$V_{C_1} = \frac{-E_0 (T_{off} + T_{on})}{T_{on}} = \frac{-E_0}{T_{on}/T} \quad V_{C_1} = \frac{-E_0}{\alpha} \tag{8.182}$$

We can calculate the average output voltage by equating Eqs (8.176) to Eq. (8.182) as,

$$V_{C_1} = \frac{E_{dc}}{1-\alpha} = \frac{-E_0}{\alpha} \quad \text{or} \quad E_0 = \frac{-\alpha \cdot E_{dc}}{1-\alpha} \tag{8.183}$$

For a lossless system, in a steady-state,

$$E_{dc} \, I_s = -E_0 \cdot I_0 = E_{dc} \, I_s = \frac{\alpha \cdot E_{dc}}{1-\alpha} I_0$$

∴ Average input current,

$$I_s = \frac{\alpha \cdot I_0}{1-\alpha} \tag{8.184}$$

Now, the switching period T can be calculated as

$$T = \frac{1}{f} = T_{on} + T_{off}$$

Substituting the value of T_{on} and T_{off} from Eqs (8.174) and (8.176), we get

$$T = \frac{\Delta I_1 \cdot L_1}{E_{dc}} - \frac{-\Delta I_1 \cdot L_1}{E_{dc} - V_{C_1}} = \frac{-\Delta I_1 \cdot L_1 V_{C_1}}{E_{dc}(E_{dc} - V_{C_1})} \tag{8.185}$$

(a) From Eq. (8.183), $E_0 = -\dfrac{0.4 \times 15}{(1-0.4)} = -10$ V

(b) From Eq. (8.184), $I_s = \dfrac{0.4 \times 1.25}{(1-0.4)} = 0.83$ A

(c) From Eq. (8.187), $\Delta I_1 = \dfrac{15 \times 0.4}{25 \times 10^3 \times 250 \times 10^{-6}} = 0.96$ A

(d) From Eq. (8.193), $\Delta V_{C_1} = \dfrac{0.83(1-0.4)}{25 \times 10^3 \times 400 \times 10^{-6}} = 49.8$ mV

(e) From Eq. (8.190), $\Delta I_2 = \dfrac{0.4 \times 15}{25 \times 10^3 \times 380 \times 10^{-6}} = 0.63$ A

(f) From Eq. (8.194), $\Delta V_{C_2} = \dfrac{0.63}{8 \times 25 \times 10^3 \times 220 \times 10^{-6}} = 14.31$ mV

(g) The average voltage across the diode can be obtained from

$$V_{DF} = -\alpha V_{C_1} = -E_0 \cdot \alpha \frac{1}{-\alpha} = E_0$$

For a lossless circuit,

$$I_{L_2} \cdot V_{DF} = E_0 \cdot I_0$$

and the average value of the current in inductor L_2 is

$$I_{L_2} = \frac{I_0 \cdot E_0}{V_{DF}} = I_0 = 1.25 \text{ A}$$

Therefore, the peak current of the device is,

$$I_p = I_s + \frac{\Delta I_1}{2} + I_{L_2} + \frac{\Delta I_2}{2} = 0.83 + \frac{0{\cdot}96}{2} + 1{\cdot}25 + \frac{0{\cdot}63}{2} = 2.88 \text{ A}$$

REVIEW QUESTIONS

8.1 Draw the schematics of step-down and step-up choppers and derive an expression for output voltage in terms of duty-cycle for a step-up and step-down chopper.

8.2 With the circuit diagram and output voltage waveforms, explain the working of Jones chopper.

8.3 With the circuit diagram and output voltage waveform, explain the principle of operation of a chopper.

8.4 Explain the time ratio control and current limit control, and control strategies used for chopper.

8.5 With the help of circuit diagram, explain the working of step-up/step-down chopper.

8.6 Draw the circuit of a two-quadrant chopper and explain its working.

8.7 With the help of voltage and current waveforms, explain the working of first-quadrant chopper. Give the complete time domain analysis of class A chopper.

8.8 Derive the expressions for $I_{0\,max}$ and $I_{0\,min}$ for class A chopper. Also, derive the expression for per unit ripple current.

8.9 Explain the continuous conduction mode and non-continuous conduction mode of class A chopper.

8.10 Derive the expression for average load current for class A chopper.

8.11 With the help of circuit diagram and associated waveforms, explain the principle of working of class C chopper.

8.12 With the help of a circuit diagram, explain the working of class D chopper.

8.13 Give the detailed circuit analysis of class D chopper.

8.14 Derive the expression for output power for class D chopper.

8.15 Draw the schematic of class E chopper and explain the working of the same.

8.16 Give the classification of chopper commutation.

8.17 Describe the voltage commutated chopper with associated voltage and current-waveforms as a function of time.

8.18 Derive the expressions for commutating components L and C for a voltage-commutated chopper. Also, discuss the assumptions made for designing the components.

8.19 With the help of basic power circuit diagram, explain the working of a current commutated chopper. Also, draw the associated waveforms.

8.20 Mention the advantages of Jones chopper circuit over other chopper circuits. Give the application of this chopper.

8.21 Explain in brief how average voltage across the load is made more than d.c. supply voltage using chopper. Derive the expression for the average voltage.

8.22 Draw a schematic diagram of a single-phase a.c. chopper and discuss in brief with output voltage and current waveforms.

8.23 Draw the single SCR chopper circuit for the control of a d.c. series motor. Explain its working with voltage and current waveforms.

8.24 Derive the expression for commuting components L, C and turn-off time t_q for the current commutated chopper circuit.

8.25 Discuss the working of load commutated chopper with associated voltage and current waveforms. Show voltage variation across each pair of SCRs as a function of time.

Derive an expression from which the value of commutating capacitor of this chopper can be calculated.

8.26 Enumerate the merits and demerits of load commutated chopper.

8.27 Describe a Morgan chopper with associated voltage and current waveforms. Enumerate the demerits of Morgan chopper compared to Jones chopper.

8.28 Discuss the design considerations of the source filter.

8.29 What is a multiphase chopper? Bring out clearly, with appropriate waveforms, the difference between the in-phase operation and phase-shifted operation of a multiphase chopper. Also, explain why phase shifted operation is always preferred.

List the merits and demerits of a multiphase choppers.

8.30 Draw and explain the working of any chopper firing circuit.

8.31 With the help of neat circuit diagram and associated waveforms discuss the operation of a Buck converter.

8.32 Derive the expressions for peak-to-peak ripple current of inductor and peak-to-peak ripple voltage of capacitor in terms of circuit components, supply voltage, frequency and duty-ratio, for a Buck converter.

8.33 List the advantages and disadvantages of the Buck chopper.

8.34 Discuss the operation of Boost converter with the help of neat circuit diagram and waveforms.

8.35 For a Boost converter, derive the expressions for peak-to-peak ripple current and ripple voltage in terms of circuit components, frequency, supply voltage and duty ratio.

8.36 List the advantages and disadvantages of the Boost chopper.

8.37 With the help of a neat circuit diagram and associated waveforms, discuss the operation of Buck–Boost converter. List the advantages and disadvantages of this type of converter.

8.38 Derive the expression for peak-to-peak ripple current and ripple voltage in case of Buck–Boost converter.

8.39 Briefly discuss the operation of Cuk converter with the help of a circuit diagram and voltage and current waveforms.

PROBLEMS

8.1 An 80 V battery supplies an *R–L* load through a chopper circuit. The load inductance is 40 mH and resistance is 6 Ω. The load has a freewheeling diode D_f across it. It is required to vary the current between the limits 10 A and 12 A. Calculate the time ratio of the chopper?

$$\left[Ans \quad \frac{T_{\text{on}}}{T_{\text{off}}} = 4.12 \right]$$

8.2 For the ideal type A chopper circuit, with a R-LE_b type load, following operating conditions are given

$E_{\text{dc}} = 220$ V, chopping period $= 1 \times 10^{-3}$ s,

$T_{\text{on}} = 400$ μs, $R = 1.5\ \Omega$, $L = 6$ mH and $E_b = 44$ V.

Compute the following quantities

(i) Check whether the load current is continuous.

(ii) Average output current.

(iii) Maximum and minimum values of steady-state output current.

(iv) RMS values of first, second and third harmonics of load current.

(v) Average value of source current.

(vi) The input power, the power absorbed by the back emf E_b and power loss in the resistor.

(vii) RMS value of output current using the results of (ii) and (iv).

(viii) The RMS value of load current using the resuls of (iv), compute the result with that obtained in part (vii) above

[*Ans* (i) $\alpha' = 0.221$, current is continuous. (ii) 29.33 A (iii) 33.77 A, 24.98 A (iv) 2.496 A, 0.772 A, –0.1716 A. (v) 11.781 A (vi) 2591.82 W, 1290.52 W, 1301.3 W. (vii) 29.45 A (viii) 29.45 A.]

8.3 A chopper circuit is operating on TRC principle at a frequency of 1 kHz on a 220 V d.c. supply. If the load voltage is 180 V, calculate the conducting and blocking period of thyristor in each cycle.

[*Ans* $T_{on} = 0.82$ μs, $T_{off} = 0.18$ μs.]

8.4 A step-up chopper with a pulse width of 150 μs is operating on 220 V d.c. supply. Compute the load voltage if the blocking period of the device is 40 μs.

[*Ans* $E_0 = 14045$ V]

8.5 A d.c. on–off chopper operating at 1 kHz and duty cycle of 10% is supplied from a 200 V source. If the load inductance is 10 mH and resistance 10 Ω. Compute the maximum and minimum circuit in the load.

[*Ans.* $I_{0max} = 2.22$ A, $I_{0min} = 0.22$ A]

8.6 An ideal d.c. chopper operating at a frequency of 600 Hz supplies a load resistance of 5Ω, inductance 1 g mH from a 110 V d.c. source. If the source has zero impedance and the load is shunted by an ideal diode as shown in Fig. 8.6, calculate average load voltage and current at mark/space $\left(\dfrac{T_{on}}{T_{off}}\right)$ ratios of

(i) 1/1 (ii) 5/1 and (iii) 1/3

[*Ans* (i) $E_0 = 55$ V, $I_0 = 11$ A (ii) $E_0 = 91.67$ V, $I_0 = 18.33$ A (iii) $E_0 = 27.5$ V, $I_0 = 5.5$ A.]

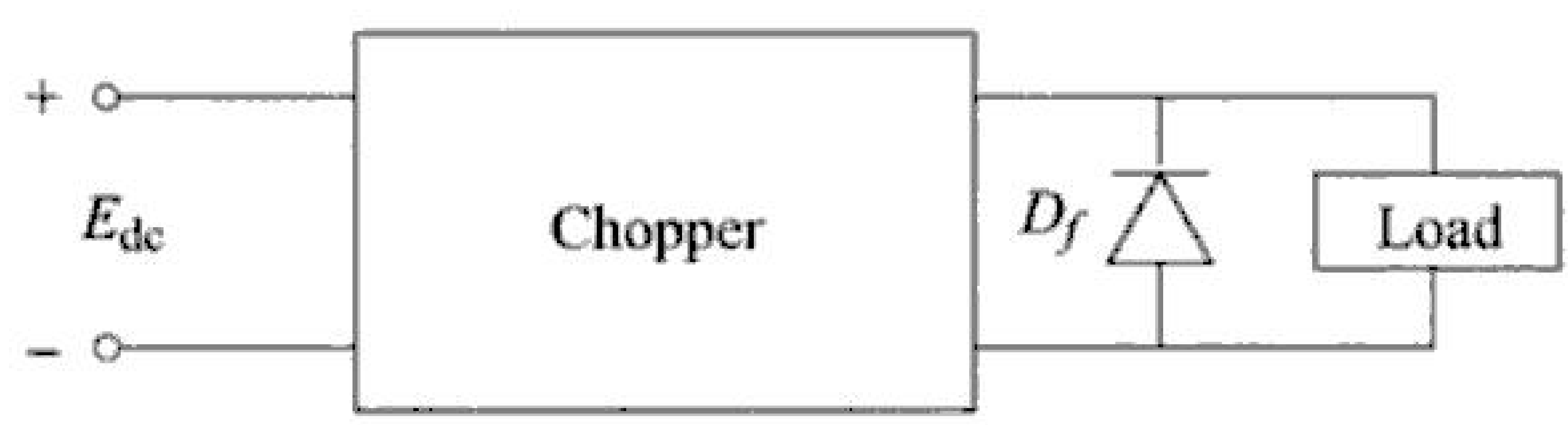


Fig. P.8.6

8.7 A current-commutated chopper controls a battery powered electric car. The battery voltage is 100 V, starting current is 100 A, thyristor turn-off time is 20 μs, chopper frequency is 400 Hz. Compute the values of commutating capacitor and commutating inductor. Assume $\dfrac{I_{cp}}{I_{0m}} = 3$.

[*Ans* $C = 48.74$ μF; $L = 4.4158$ μH.]

8.8 For a current-commutated chopper, peak commutating current is twice the maximum possible load current, the source voltage is 230 V d.c. and main SCR turn-off time is 30 μ sec. For a maximum load current of 200 A, compute

(a) the values of commutating inductor and capacitor
(b) maximum capacitor voltage
(c) the peak commutating current.

[*Ans* (a) $L = 13.178$ μH (b) 345 V (c) 400 A $C = 39.86$ μF.]

8.9 A chopper fed from a 220 V d.c. source is working at a chopping period of 20 ms and is connected to an R–L, Load of $R = 5$ Ω and $L = 40$ mH.

(a) compute the value of α at which the minimum load current will be
(i) 5 A (ii) 10 A (iii) 20 A (iv) 30 A
(b) For the values of duty-cycle obtained in part (a) above, calculate the values of maximum currents and ripple factors.

[*Ans.* (a) 0.328, 0.506, 0.722, 0.862 (b) 26.823 A, 34.405 A, 40.051 A, 42.379 A. ripple factors 1.4313, 0.988, 0.6205, 0.40.]

8.10 A d.c. battery is charged from a constant d.c. source of 220 V through a chopper. The d.c. battery is to be charged from its internal emf of 90 V to 122 V. The battery has internal resistance of 1 Ω. For a constant charging current of 10 A, calculate the range of duty cycle.

[*Ans.* 0.45 to 0.6.]

8.11 The Buck-converter in Fig. 8.43 has an input voltage of E_{dc} = 16 V. The required average output voltage is E_0 = 8 V, and the peak-to-peak output ripple voltage is 10 mV. The switching frequency is 25 kHz. If the peak-to-peak ripple current of inductor is limited to 0.7 A. Determine: (a) duty-cycle α, (b) filter inductance, *L*, and (c) the filter capacitor *C*.

[*Ans* (a) 50%; (b) 228.57 μH; (c) 350 μF.]

8.12 Consider the boost converter of Fig. 8.44. The input voltage to this converter is 8 V. The average output voltage E_0 = 16 V and the average load current I_0 = 0.5 A. The switching frequency is 30 kHz. If L = 160 μH and C = 380 μF. Compute (a) the duty-cycle α; (b) the ripple current of inductor, ΔI; (c) the peak current of inductor, I_2, and (d) the ripple voltage of filter capacitor, ΔV_c.

[*Ans.* (a) 50%; (b) 0.83 A; (c) 1.415 A; (d) 21.93 mv.]

8.13 Consider the buck–bost converter of Fig. 8.45. The input voltage to this converter is E_{dc} = 10 V. The duty cycle α = 0.3 and the switching frequency is 25 kHz. The inductance I = 150 μH and filter-capacitance C = 220 μF. The average load current I_0 = 1.2 A. Determine:

(a) The average output voltage, E_0,
(b) The peak-to®-peak output voltage ripple, ΔV_C,
(c) The peak-to-peak current of inductor, ΔI, and
(d) the peak current of the transistor I_p. [*Ans* (a) – 4.29 V; (b) 65.45 mV; (c) 0.8 A; (d) 2.1 A.]

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Chapter **9**

Inverters

LEARNING OBJECTIVES:

- To describe the need and function of an inverter.
- To consider the operation of single-phase half-bridge and full-bridge transistorised inverters.
- To introduce the performance parameters of inverters.
- To examine the operation of unipolar and bipolar pwm inverters.
- To consider the operation and design of series inverter with different circuit arrangements.
- To examine the operation of a three-phase series inverter.
- To consider the operation of a high frequency series inverter.
- To consider the operation and design considerations of self-commutated inverters.
- To consider the operation and design details of parallel inverter with different circuit arrangements.
- To examine the operation and detailed design aspects of various voltage source bridge inverter circuits.
- To examine the operation of three-phase bridge inverters with different conduction modes.
- To consider the means of controlling a variable frequency inverter output-voltage.
- To introduce various schemes of pulse width modulated inverters.
- To examine the basic techniques of harmonic filtering and to introduce filter types.
- To examine the operation of current source inverters as a means of producing a variable frequency supply.

9.1 INTRODUCTION

The d.c. to a.c. power converters are known as inverters. In other words, an inverter is a circuit which converts a d.c. power into an a.c. power at desired

9.2.1 Thyristor Inverter Classification

The thyristor inverters can be classified in the following categories:

1. According to the method of commutation.
2. According to the connections.

(a) Classification According to the Method of Commutation According to the method of commutation, the SCR inverters can mainly be categorised in two types, viz.

1. Line commutated inverters
2. Forced commutated inverters.

1. Line Commutated Inverters In case of a.c. circuits, a.c. line voltage is available across the device. When the current in the SCR goes through a natural zero, the device is turned-off. This process is known as natural commutation process and the inverters based on this principle are known as line commutated inverters.

2. Forced Commutated Inverters In case of d.c. circuits, since the supply voltage does not go through the zero point, some external source is required to commutate the device. This process is known as the forced commutation process and the inverters based on this principle are called as forced commutated inverters. As the device is to be commutated forcefully, these types of inverters require complicated commutation circuitries. These inverters are further classified as: (i) Auxiliary commutated inverters and (ii) Complementary commutated inverters.

(b) Classifications According to Connections According to the connections of the thyristors and commutating components, the inverters can be classified mainly in three groups. These are:

1. Series inverters.
2. Parallel inverters.
3. Bridge inverters.: Bridge inverters are further classifed as: (i) Half-bridge and (ii) Full-Bridge.

9.3 SINGLE-PHASE HALF-BRIDGE VOLTAGE-SOURCE INVERTERS

Figure 9.1 shows the basic configuration of single-phase half-bridge inverter. Switches S_1 and S_2 are the gate-commutated devices such as power BJTs, MOSFETs, GTO, IGBT, MCT, etc. When closed, these switches conducts and current flows in the direction of arrow. The operation of this inverter for different types of load is explained in the following sections:

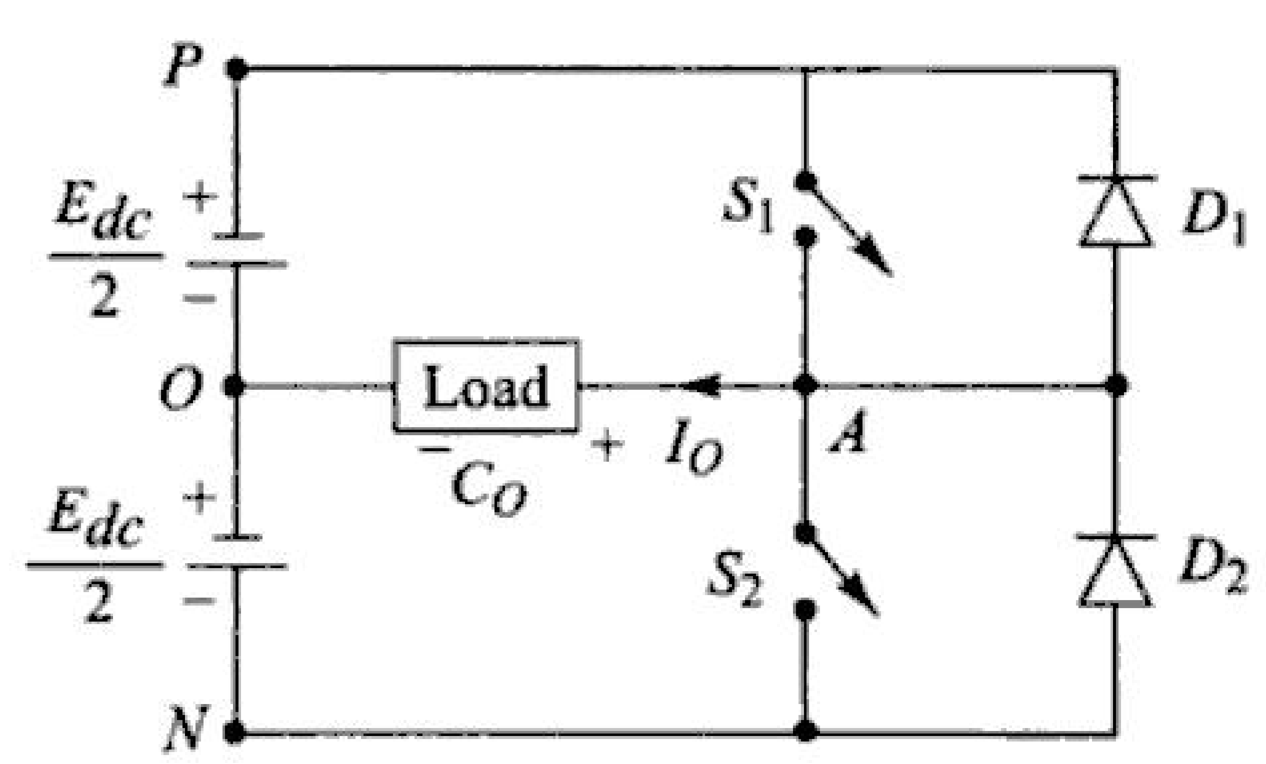

Fig. 9.1 *Half-bridge inverter*

9.3.1 Operation with Resistive Load

The operation of the circuit can be divided into two periods:

(i) Period-I, where switch S_1 is conducting from $0 \le 1 \le T/2$ and

(ii) Period-II, where switch S_2 is conducting from $T/2 \le t \le T$,

where $T = 1/f$ and f is the frequency of the output voltage waveform. Figure 9.2 shows the waveforms for the output voltage and switch currents for a resistive-load.

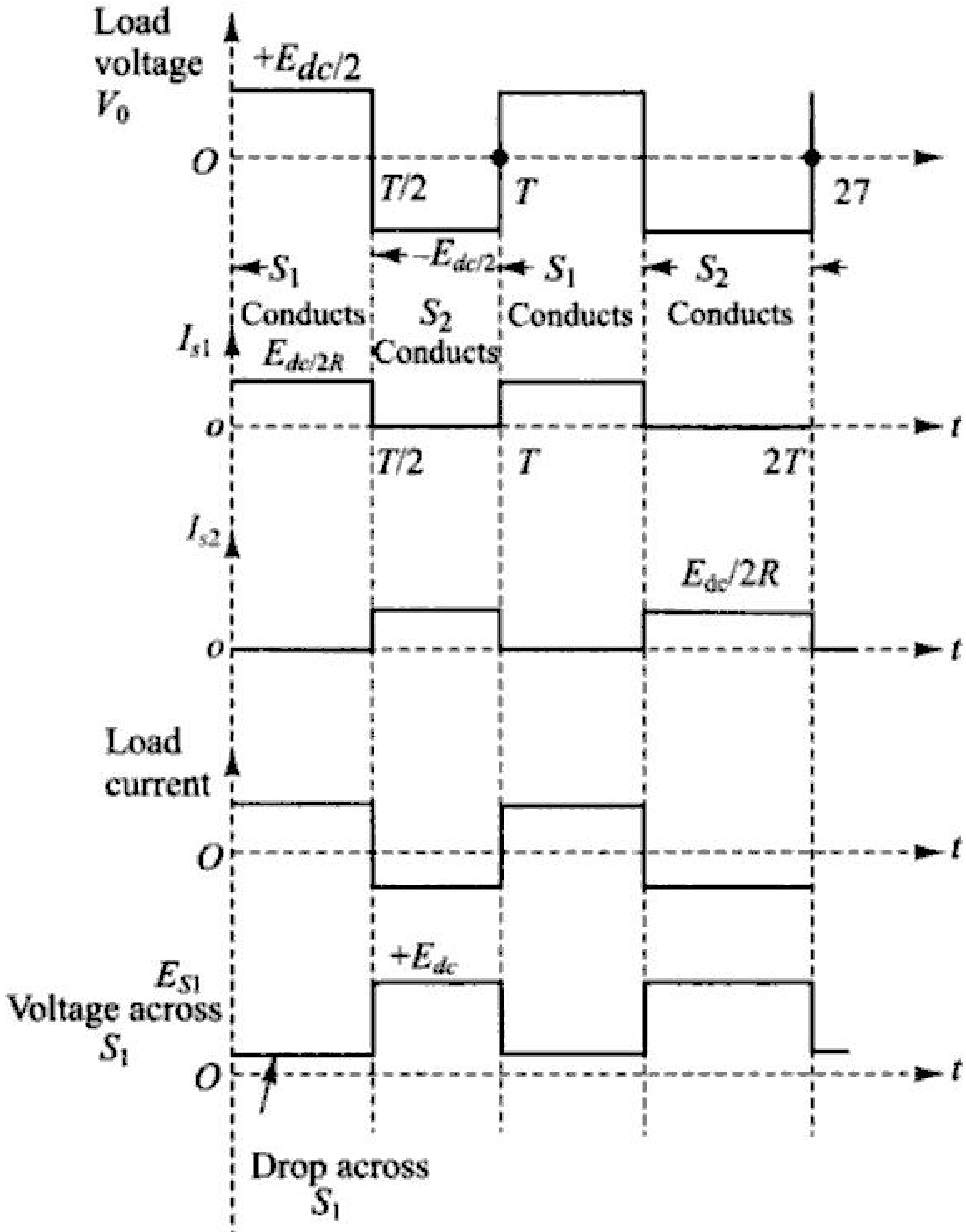

Fig. 9.2 *Voltage and current waveforms*

Switch S_1 is closed for half-time period ($T/2$) of the desired ac output. It connects point p of the dc source to point A and the output voltage e_0 becomes equal to $+E_{dc}/2$.

At $t = T/2$, gating signal is removed from S_1 and it turns-off. For the next half-time period ($T/2 < t < T$), the gating signal is given to S_2. It connects point N of the dc source to point A and the output voltage reverses. Thus, by closing S_1 and S_2 alternately, for half-time periods, a square-wave ac voltage is obtained at the output. With resistive load, waveshape of load current is identical to that of output voltage. Simply by controlling the time periods of the gate-drive signals, the frequency can be varied. Here diodes D_1 and D_2 do not play any role. The voltage across the switch when it is OFF is E_{dc}. Gating circuit should be designed such that switches S_1 and S_2 should not turn-on at the same time.

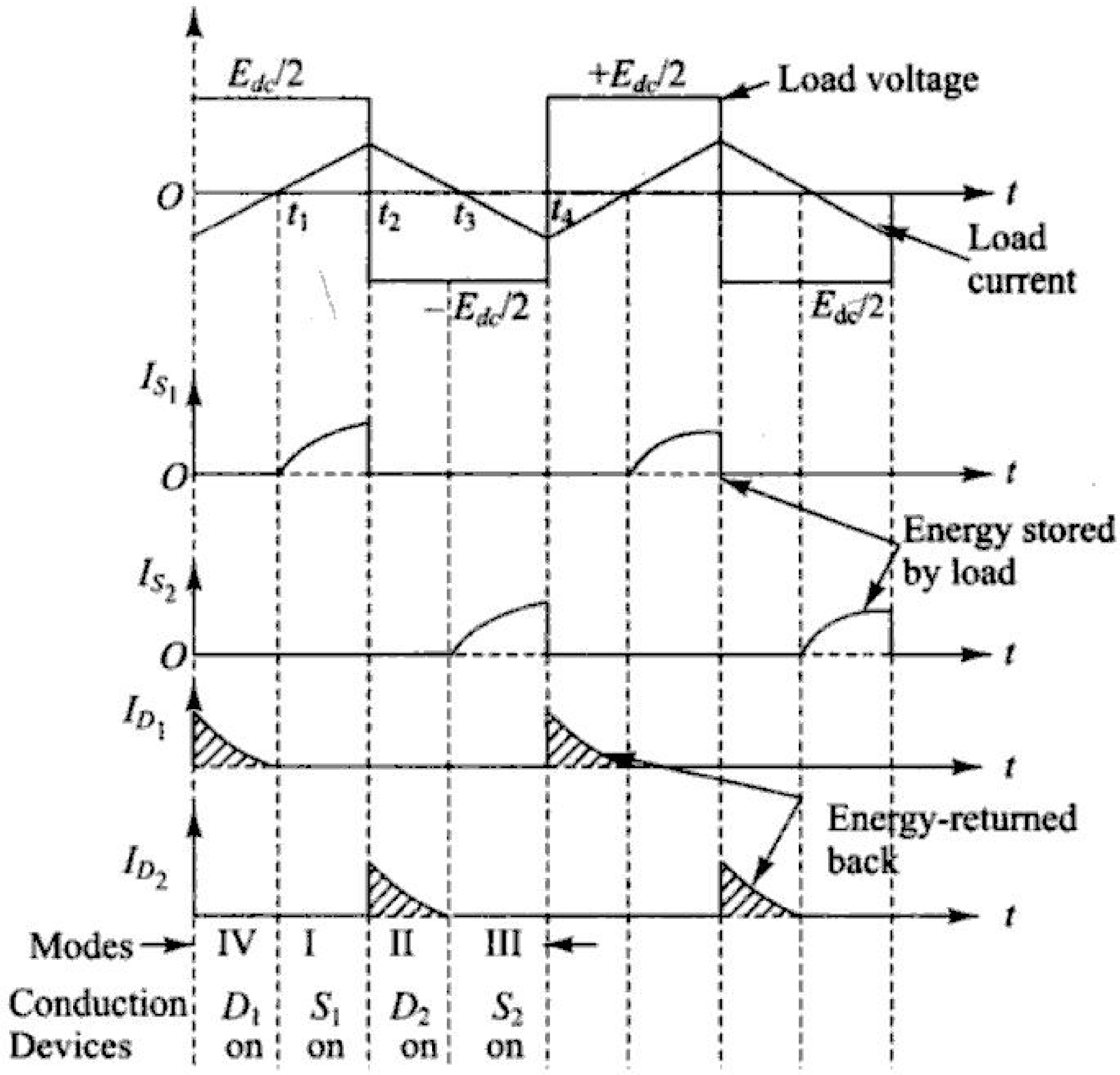

Fig. 9.3 *Voltage and current waveforms with RL load*

instant t_3, S_2 is turned-on. This will produce a negative load voltage $e_0 = -E_{dc}/2$ and a negative load current. Load current reaches a negative peak at the end of this interval (Fig. 9.4(c)].

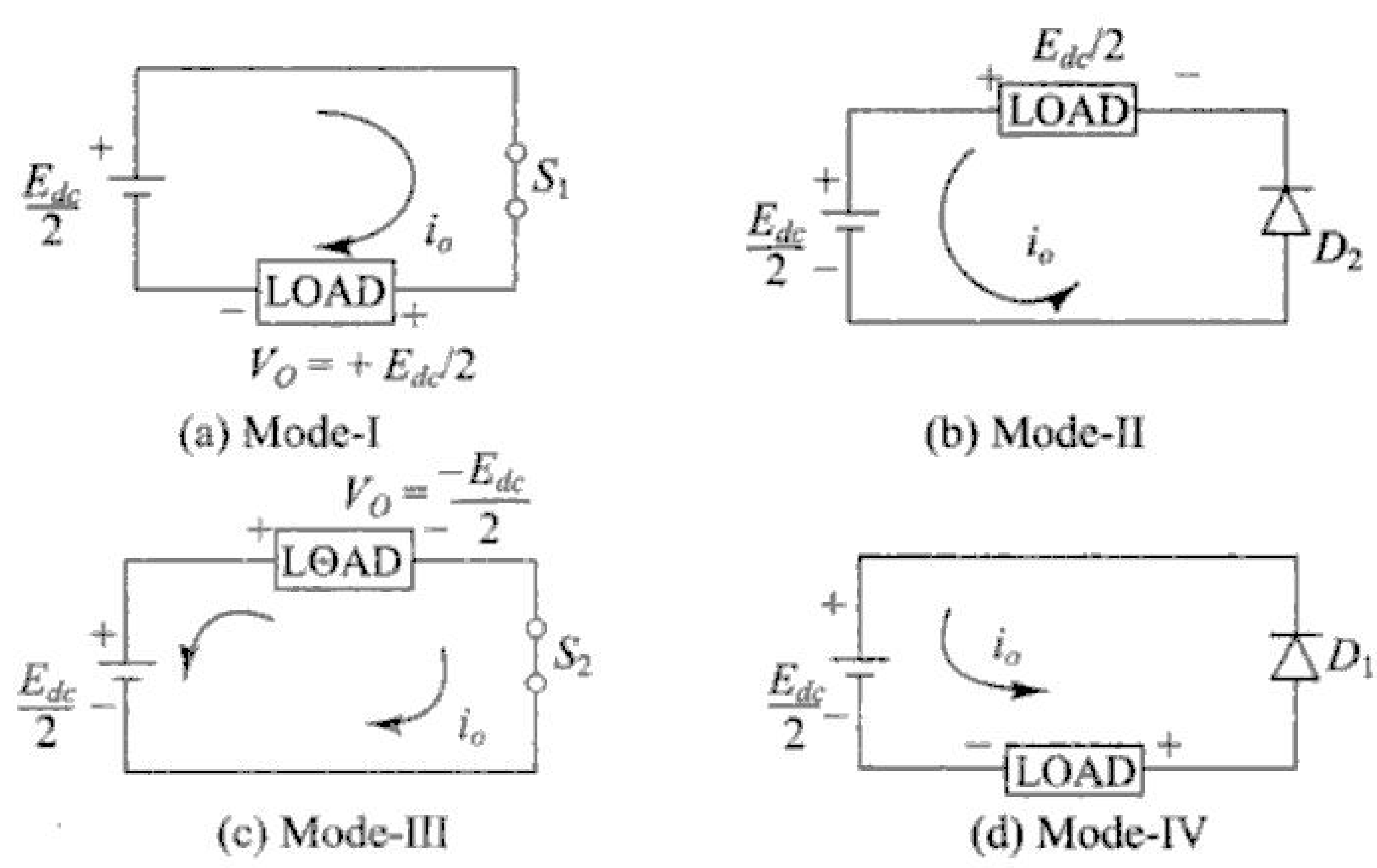

Fig. 9.4 *Operating modes*

Mode IV ($t_0 < t < t_1$): Switch S_2 is turned-off at instant t_4. The self induced voltage in the inductive load will maintain the load current. The load voltage changes its polarity to become positive $E_{dc}/2$, load current remains negative and the stored energy in the load is returned back to the upper half of the dc source (Fig. 9.4(d)).

At t_5, the load current goes to 0 and S_1 can be turned-on again. This cycle of operation repeats.

Circuit-Equations

(i) Instantaneous Current i_0:- With RL load, the equation for instantaneous current i_0 can be obtained from Eq. (9.2), as

$$i_0(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2\,E_{dc}}{n\,\pi\sqrt{R^2 + (n\,\omega L)^2}} \sin(n\omega t - \theta_n) \tag{9.9}$$

Here, $Z_n = \sqrt{R^2 + (n\,\omega L)^2}$ is the impedance offered by the load to the n^{th} harmonic component, $\frac{2\,E_{dc}}{n\,\pi}$ is the peak amplitude of n^{th} harmonic voltage, and

$$\theta_n = \tan^{-1}\left(\frac{n\,\omega L}{R}\right) \tag{9.10}$$

(ii) Fundamental Output Power: The output power at fundamental frequency ($n = 1$) is given by

$$P_{1_{rms}} = E_{1_{rms}} \cdot I_{1_{rms}} \cdot \cos\theta_1 = I^2_{1_{rms}} \cdot R \tag{9.11}$$

where $E_{1_{rms}}$ = RMS value of fundamental output voltage.

$I_{1_{rms}}$ = RMS value of fundamental output current

$\theta_1 = \tan^{-1}(\omega L/R)$

But

$$I_{1_{rms}} = \frac{2\,E_{dc}}{\sqrt{2}\cdot\pi\cdot\sqrt{R^2 + (\omega L)^2}} \tag{9.12}$$

$$P_{1_{rms}} = I^2_{1_{rms}} \cdot R = \left[\frac{2\,E_{dc}}{\pi\cdot\sqrt{2}\,\sqrt{R^2 + (\omega L)^2}}\right]^2 \cdot R \tag{9.13}$$

$$= \left[\frac{4\,E^2_{dc}\cdot R}{2\pi^2\,(R^2 + \omega^2 L^2)}\right] = \left[\frac{2\,E^2_{dc}\cdot R}{\pi^2\,(R^2 + \omega^2 L^2)}\right] \tag{9.14}$$

Importance of fundamental power is that in many applications such as electric motor drives, the output power due to fundamental current is generally the useful power and the power due to harmonic current is dissipated as heat and increases the load dissipation.

9.3.3 Cross Conduction or Shoot through Fault

In the half-bridge inverter circuit, each switch conducts for a period of $T/2$ secs. At any particular instant, one switch is turned-on and the other is turned-off. However, the outgoing switch does not turn-off instantaneously due to its finite turn-off delay. Due to this, both switches (incoming and outgoing) conduct simultaneously for a short-time. This is known as cross-conduction or shoot-through-fault.

When both switches conducts simultaneously, the input dc supply is short-circuited and with this switches get damaged. Cross conduction can be avoided by allowing the outgoing switch to turn-off completely first and then applying the gate-drive to the incoming device. A dead-band or delay is introduced between the trailing-edge of the base-drive of outgoing device and the leading-edge of the base-drive of the incoming device. Therefore, during the dead-band interval, no device receives base-drive. Hence, the dead-band should be longer than the turn-off time of the power-devices used in the inverter circuit.

SOLVED EXAMPLES

Example 9.1 The single-phase half-bridge inverter has a resistive load of 10 Ω and the center-tap dc input voltage is 96 V. Compute:

(i) RMS value of the output voltage.
(ii) Fundamental component of the output voltage waveform.
(iii) First five harmonics of the output-voltage waveform.
(iv) Fundamental power consumed by the load.
(v) RMS power consumed by the load.
(vi) Verify that the rms value determined by harmonic summation method is nearly equal to the value determined by integration method.

Solution:

(i) From Eq. (9.1), $E_{0(\text{rms})} = \dfrac{E_{dc}}{2} = 96$ volts

(ii) From Eq. (9.4), $E_{1(\text{fund})} = \dfrac{\sqrt{2}}{\pi} E_{dc} = 0.9 \times 96 = 86.40$ volts

(iii) From Eq. (9.3), first five harmonics are given by

$$E_{0(3)} = \frac{E_1}{3} = \frac{86.4}{3} = 28.8 \text{ V}, \quad E_{0(5)} = \frac{E_1}{5} = \frac{86.4}{5} = 17.28 \text{ V}$$

$$E_{0(7)} = \frac{E_1}{7} = \frac{86.4}{7} = 12.34 \text{ V}, \quad E_{0(9)} = \frac{E_1}{9} = \frac{86.4}{9} = 9.6 \text{ V}$$

$$E_{0(11)} = \frac{E_1}{11} = \frac{86.4}{11} = 7.85 \text{ V}$$

(iv) Fundamental power, $P_{0(\text{fund})} = \dfrac{E^2_{1(\text{fund})}}{R} = \dfrac{(86.0)^2}{10} = 746.5$ W

(v) RMS power, $P_{0(\text{rms})} = \dfrac{E^2_{0(\text{rms})}}{R} = \dfrac{(96)^2}{10} = 921.6$ W

(vi) RMS value by harmonic summation method is

$$E_{0(\mathrm{rms})} = \sqrt{E_1^2 + E_3^2 + E_5^2 + E_7^2 + E_9^2 + E_{11}^2} = 94.34\text{ V}$$

Thus, the two values are equal. The value obtained by harmonic summation method is always less than that found by direct integration method.

9.4 SINGLE-PHASE FULL-BRIDGE INVERTERS

Figure 9.5 shows the power-diagram of the single-phase bridge inverter. The inverter uses two pairs of controlled switches (S_1S_2 and S_3S_4) and two pairs of diodes (D_1D_2 and D_3D_4). The devices of one pair operate simultaneously. In order to develop a positive voltage ($+E_0$) across the load, switches S_1 and S_2 are turned-on simultaneously whereas to have a negative voltage ($-E_0$) across the load, we need to turn-on the switches S_3 and S_4. Diodes D_1, D_2, D_3 and D_4 are known as the feedback diodes.

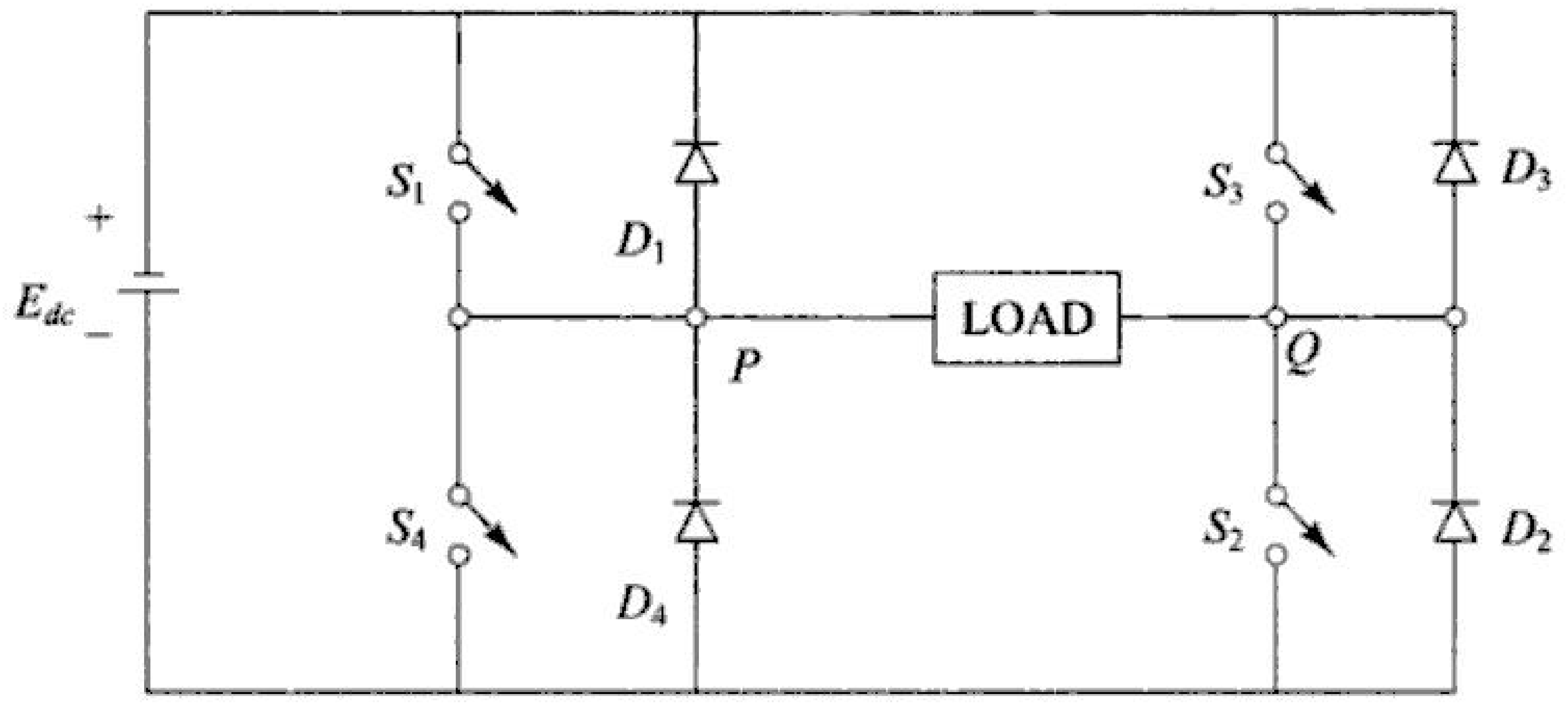

Fig. 9.5 *Single-phase full-bridge inverter*

9.4.1 Operation with Resistive Load

Voltage and current waveforms with resistive-load are shown in Fig. 9.6. The bridge-inverter operates in two-modes in one-cycle of the output.

(i) Mode-I ($0 < t < T/2$): In this mode, switches S_1 and S_2 conducts simultaneously. The load voltage is $+E_{dc}$ and load current flows from P to Q. The equivalent circuit for mode-I is shown in Fig. 9.7(a). At $t = T/2$, S_1 and S_2 are turned-off and S_3 and S_4 are turned-on.

(ii) Mode-II ($T/2 < t < T$): At $t = T/2$, switches S_3 and S_4 are turned-on and S_1 and S_2 are turned-off. The load voltage is $-E_{dc}$ and load current flows from Q to P. The equivalent circuit for mode-II is shown in Fig. 9.7 (b). At $t = T$, S_3 and S_4 are turned-off and S_1 and S_2 are turned-on again.

As the load is resistive, it does not store any energy. Therefore, feedback diodes are not effective here.

(v) Transistor (switch) ratings:

$$V_{CE_0} \geq E_{dc}, I_{T(av)} = \frac{E_{dc}}{2R}$$

$$I_{T(rms)} = \frac{E_{dc}}{\sqrt{2}\,R}, I_{T(peak)} = \frac{E_{dc}}{R} \tag{9.19}$$

SOLVED EXAMPLES

Example 9.2 A single-phase full-bridge inverter is operated from a 48V battery and is supplying power to a pure resistive load of 10 Ω. Determine:

(i) the fundamental output voltage and the first five harmonics.
(ii) RMS value by direct integration method and harmonic summation method.
(iii) Output rms power and output fundamental power.
(iv) Transistor switch ratings.

Solution: *Given:* $E_{dc} = 48$ V, $R = 10$ ohm

(i) From (9.17), $E_{0(fund)} = \dfrac{2\sqrt{2}}{\pi} E_{dc} = \dfrac{2\sqrt{2}}{\pi}(48) = 43.22$ V

Now n^{th} harmonic voltage, $E_{0(n)} = \dfrac{E_{0\,(fund)}}{n}$

$$\therefore \quad E_{0(3)} = \frac{43.22}{3} = 14.40 \text{ V}, \quad E_{0(5)} = \frac{43.22}{5} = 8.64 \text{ V}$$

$$E_{0(7)} = \frac{43.22}{7} = 6.17 \text{ V}, E_{0(9)} = \frac{43.22}{9} = 4.80 \text{ V}, E_{0(11)} = \frac{43.22}{11} = 3.92 \text{ V}$$

(ii) $E_{0(rms)} = E_{dc} = 48$ V also, $E_{0(rms)} = \sqrt{E_1^2 + E_3^2 + E_5^2 + E_7^2 + E_9^2 + E_{11}^2}$

$$= \sqrt{(43.22)^2 + (14.40)^2 + (8.64)^2 + (6.17)^2 + (4.8)^2 + (3.92)^2} = 47.18 \text{ V}$$

Hence, the two values are nearly equal.

(iii) Output rms power, $P_{0rms} = \dfrac{E_{0(rms)}^2}{R} = \dfrac{48^2}{10} = 230.4$ W

Output fundamental power, $P_{0(fund.)} = \dfrac{E_{0(fund)}^2}{R} = 186.624$ W

(iv) Switch (Transistor) Ratings:

$$V_{CE_0} \geq E_{dc} \geq 48 \text{ V}, I_{T(peak)} \geq \frac{E_{dc}}{R} \geq 4.8 \text{ A}$$

$$I_{T(rms)} \geq \frac{E_{dc}}{\sqrt{2} \cdot R} \geq 3.394 \text{ A}, I_{T(avg)} \geq \frac{E_{dc}}{\sqrt{2}\,R} \geq 2.4 \text{ A}$$

is returned back to the source. Load current decreases exponentially and goes to 0 at instant t_3 when all the energy stored in the load is returned back to supply. D_3 and D_4 are turned-off at t_3.

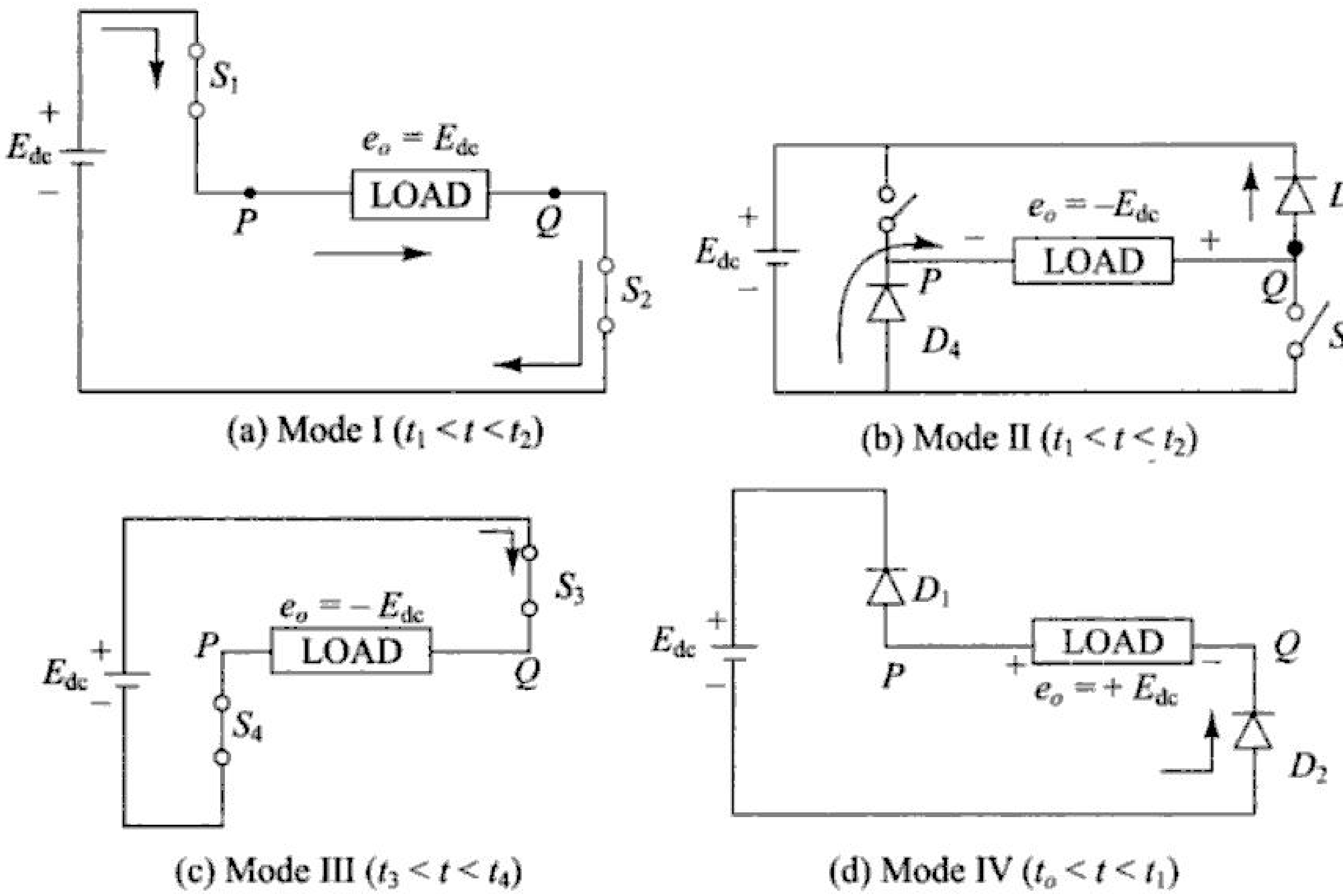

Fig. 9.9 *Equivalent circuits*

(iii) Mode III ($t_3 < t < t_4$): Switches S_3 and S_4 are turned-on simultaneously at instant t_3. Load voltage remains negative ($-E_{dc}$) but the direction of load current will reverse. The current increases exponentially in the other direction and the load again stores the energy.

(iv) Mode IV ($t_0 < t < t_1$): Switches S_3 and S_4 are turned-off at instant t_0 (or t_4). The load inductance tries to maintain the load current in the same direction by inducing the positive-load voltage. This will forward-bias the diodes D_1 and D_2. The load energy is returned back to the input dc supply. The load voltage becomes $e_0 = +E_{dc}$ but the load current remains negative and decreases exponentially towards 0. At t_1 (or t_5), the load current goes to zero and switches S_1 and S_2 can be turned-on again. The conduction period with a very highly inductive load, will be $T/4$ or 90° for all the switches as well as the diodes. The conduction period of switches will increase towards $T/2$ or 180° with increase in the load power-factor.

Circuit Analysis

(i) RMS output voltage can be obtained from

$$E_{0rms} = \left[\frac{2}{T/2}\int_0^{T/2} E^2\,dt\right]^{1/2} \quad \therefore \quad E_{0rms} = E_{dc} \tag{9.20}$$

(ii) The instantaneous output voltage can be expressed in fourier series as

$$e_{0(\omega t)} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4\,E_{dc}}{n\pi} \sin n\omega t \tag{9.21}$$

The output voltage waveform contains only the odd harmonic components, i.e. 3, 5, 7, ... The even order harmonics are automatically cancelled.

(iii) For $n = 1$, Eq. (9.21) gives the rms value of the fundamental component

$$E_{1(rms)} = \frac{4\,E_{dc}}{\sqrt{2}\cdot\pi} = 0.9\,E_{dc} \tag{9.22}$$

(iv) For RL load, the equation for the instantaneous current i_0 can be found using the Equation (9.21), as

$$i_{0(t)} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4\,E_{dc}}{n\pi\sqrt{R^2+(n\,\omega L)^2}} \sin(n\omega t-\theta_n) \tag{9.23}$$

In this equation, $Z_n = \sqrt{R^2+(n\,\omega L)^2}$ is the impedance offered by the load to the n^{th} harmonic component and $\frac{4\,E_{dc}}{n\,\pi}$ is the peak amplitude of n^{th} harmonic voltage, and

$$\theta_n = \tan^{-1}(n\omega L/R) \tag{9.24}$$

Solved Examples

Example 9.3 The full-bridge inverter of Fig. 9.5 has a source voltage $E_{dc} = 220$ V. The inverter supplies an RLC load with $R = 10$ ohm, $L = 10$ mH and $C = 52\ \mu$F. The inverter frequency is 400 Hz. Determine:

(a) the rms load current at fundamental frequency
(b) the rms value of load current
(c) the power output and (d) the average supply current

Solution:

Given: $E_{dc} = 220$ V, $R = 10\ \Omega$, $L = 10$ mH, $C = 52\ \mu$F, $f = 400$ Hz

The inductive reactance of the fundamental voltage

$$X_L = 2\pi f L = 2\times\pi\times 400\times 10\times 10^{-3} = 25.13\ \Omega$$

The capacitive reactance for the fundamental voltage,

$$X_C = \frac{1}{2\pi\, f.c} = \frac{1}{2\pi\times 400\times 52\times 10^{-6}} = 7.7\ \Omega$$

Impedance offered to the n^{th} harmonic-component

$$Z_n = \sqrt{R^2+\left(nX_L-\frac{X_c}{n}\right)^2}$$

It is defined as the ratio of the rms voltage of a particular harmonic component to the rms value of fundamental component.

$$\therefore \qquad \mathrm{HF}_n = \frac{E_{n_{\mathrm{rms}}}}{E_{1_{\mathrm{rms}}}} \tag{9.26}$$

(b) Total Harmonic Distortion (THD) A total harmonic distortion is a measure of closeness in a shape between the output voltage waveform and its fundamental component. It is defined as the ratio of the rms value of its total harmonic component of the output voltage and the rms value of the fundamental component. Mathematically,

$$\mathrm{THD} = \sqrt{\sum_{n=2,3,\ldots}^{\infty} E_{n_{\mathrm{rms}}}^2} \Big/ E_{1_{rms}} \tag{9.27}$$

$$= \sqrt{\frac{E_{0_{\mathrm{rms}}}^2 - E_1^2}{E_1}} \tag{9.28}$$

(c) Distortion Factor (DF) A distortion factor indicates the amount of harmonics that remain in the output voltage waveform, after the waveform has been subjected to second-order attenuation (i.e. divided by n^2). It is defined as

$$\mathrm{DF} = \sqrt{\frac{\sum_{n=2,3,\ldots}^{\infty} \left(\frac{E_{n_{\mathrm{rms}}}}{n^2}\right)^2}{E_{1_{\mathrm{rms}}}}} \tag{9.29}$$

(d) Lowest-Order Harmonics (LOH) The lowest frequency harmonic, with a magnitude greater than or equal to three-per cent of the magnitude of the fundamental component of the output voltage, is known as *lowest-order harmonic.* Higher the frequency of the LOH, lower will be the distortion in the current waveform.

SOLVED EXAMPLES

Example 9.4 A single-phase half-bridge inverter has a resistive load of $R = 3\ \Omega$ and the dc input voltage $E_{\mathrm{dc}} = 24$ Volts. Determine:

(a) IGBT ratings (b) Total harmonic distortion THD
(c) The distortion factor DF
(d) The harmonic factor and the distortion factor of the lowest order harmonic

Solution:

(a) IGBT ratings: (i) Average I_{avg} current $= \dfrac{1}{T}\displaystyle\int_0^{T/2} \dfrac{E_{\mathrm{dc}}}{2R}\, dt = \dfrac{E_{\mathrm{dc}}}{2RT}\,(T/2) = \dfrac{E_{\mathrm{dc}}}{4R}$

$$\therefore \quad \text{Average IGBT current} = \frac{24}{3 \times 4} = 2 \text{ Amp}$$

(ii) IGBT peak current $= I_{peak} = \dfrac{E_{dc}/2}{R} = 4$ Amp

(iii) Peak reverse blocking voltage V_{BR} of each IGBT,

$$V_{BR} = 2 \times \frac{E_{dc}}{2} = 24 \text{ Volts}$$

(b) Total harmonic distortion (THD):

$$\text{THD} = \frac{1}{E_{1rms}} \left[\sum_{n=2,3}^{\infty} E_{n_{rms}}^2 \right]^{1/2}, \quad \therefore \quad E_{1rms} = \frac{2\,E_{dc}}{\sqrt{2}\,\pi} = 10.8 \text{ V}$$

$$\text{RMS harmonic voltage} = \left[\sum_{n=3,5,7}^{\infty} E_{n_{rms}}^2 \right]^{1/2}$$

$$= \sqrt{E_0^2 - E_{1rms}^2} = [12^2 - (10.8)^2]^{1/2} = 5.23 \text{ V}$$

$$\therefore \qquad \text{THD} = \frac{5.23}{10.8} = 0.484 = 48.4\%$$

(c) Distortion Factor DF: $= \dfrac{1}{E_{1rms}} \left[\displaystyle\sum_{n=3,5,7}^{\infty} \left(\frac{E_{n\,rms}}{n^2} \right)^2 \right]^{1/2}$

To determine $\dfrac{E_{n\,rms}}{n^2}$, we have to find E_{nrms},

$$\therefore \quad E_0 = \sum_{n=1,3,5}^{\infty} \frac{2\,E_{dc}}{n\pi} \sin n\omega t = 0, \text{ for } n = 2, 4, 6.$$

$$\therefore \quad E_0 = \frac{2\,E_{dc}}{\pi} \sin \omega t + \frac{2\,E_{dc}}{3\pi} \sin 3\omega t + \frac{2\,E_{dc}}{5\pi} \sin 5\,\omega t + \frac{2\,E_{dc}}{7\pi} \sin 7\,\omega t + \ldots$$

$$E_{3rms} = \frac{2\,E_{dc}}{3\pi\sqrt{2}} = 3.6 \text{ V}, E_{5rms} = \frac{2\,E_{dc}}{5\pi\sqrt{2}} = 2.16 \text{ V}$$

$$E_{7rms} = 1.54 \text{ V}, E_{9rms} = 1.2 \text{ V},$$

$$E_{11rms} = 0.982 \text{ V}, E_{13rms} = 0.83 \text{ V}$$

$$\left[\sum_{n=3,5,7}^{\infty} \left(\frac{E_{n\,rms}^2}{n^2} \right)^2 \right]^{1/2} = \left[\left(\frac{E_3}{3^2} \right)^2 + \left(\frac{E_5}{5^2} \right)^2 + \left(\frac{E_7}{7^2} \right)^2 + \ldots \right]^{1/2}$$

$$= [0.16 + 0.0348 + 2.3 \times 10^{-3} + \ldots]^{1/2} = 0.44 \text{ V}$$

$$\therefore \qquad \text{DF} = \frac{0.44}{10.8} = 0.041 = 4.1\%$$

(d) The lowest harmonic is third harmonic.

$$\therefore \quad \text{HF for the third harmonic} = \text{HF}_3 = \frac{E_{3rms}}{E_{1rms}} = \frac{3.6}{10.8} = 33.33\%$$

(ii) In control schemes of Fig. 9.11, the number of power converters used for the control of inverter output voltage varies from two to three. More power handling converter stages result in more losses and reduced efficiency of the entire scheme.

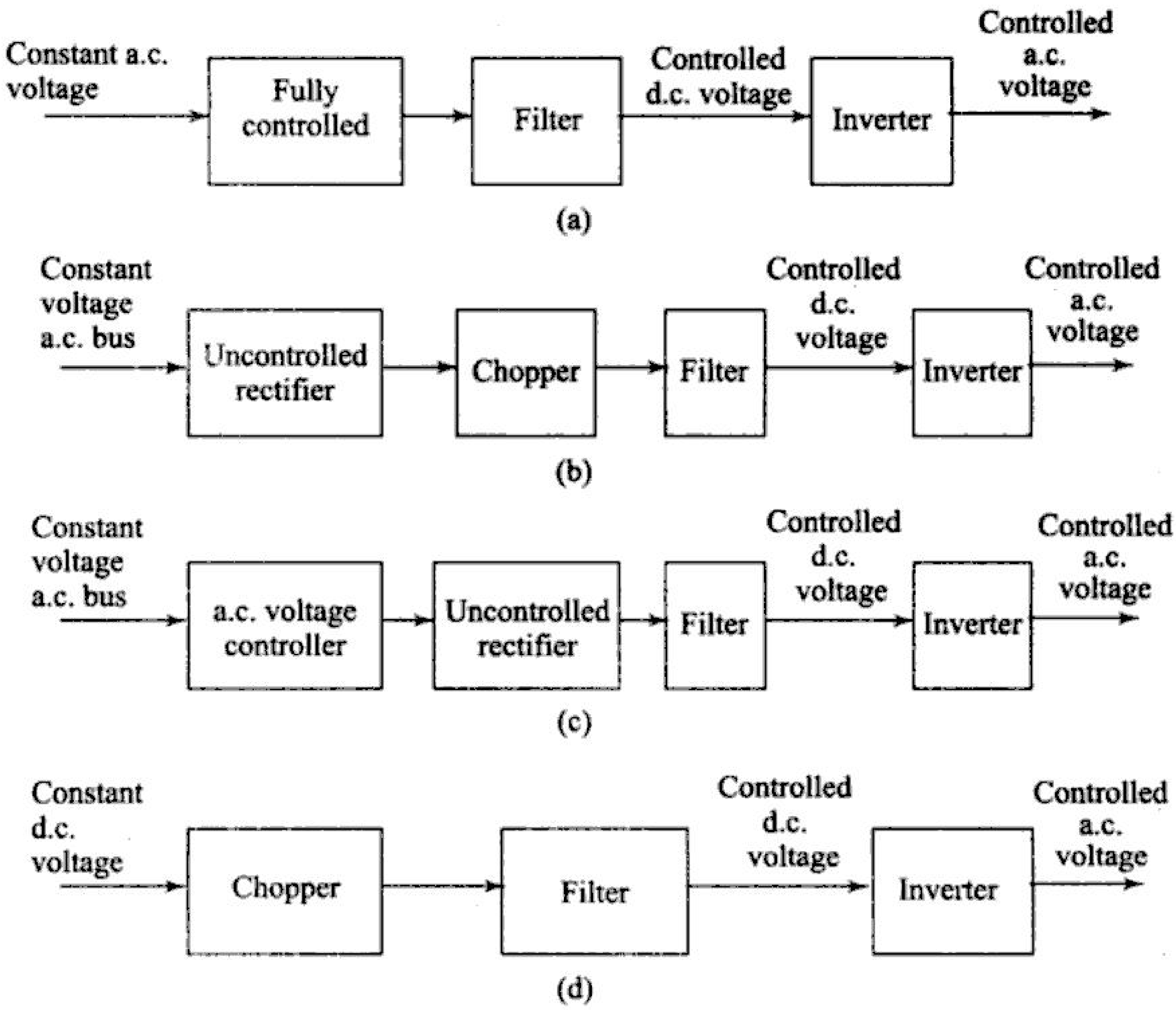

Fig. 9.11 *Voltage control by controlling d.c. input voltage*

(iii) The commutating capacitor voltage decreases as the d.c. input voltage is reduced. This has the effect of reducing the circuit turn-off time for the SCR for a constant load current. Therefore, for a large variation of output voltage for a constant load current, control of d.c. input voltage is not desirable. This limitation can, however, be overcome by a separated fixed d.c. source for charging the commutating capacitor, but this makes the scheme costly and complicated.

9.6.3 Internal Control of Inverter

Inverter output voltage can also be adjusted by exercising a control within the inverter itself. The two possible ways of doing this are:

(a) Series inverter control, and
(b) Pulse-width modulation control.

1. Series Inverter Control This method of voltage control involves the use of two or more inverters in series. Figure 9.12(a) illustrates how the output voltage of two inverters can be summed up with the help of transformers to obtain an adjustable output voltage. In this figure, the inverter output is fed to two transformers whose secondaries are connected in series. Phasor sum of the two voltages E_{L_1}, E_{L_2} gives the resultant voltage E_L as shown in Fig. 9.12(b). The voltage E_L is given by

$$E_L = [E_{L_1}^2 + E_{L_2}^2 + 2\,E_{L_1}\,E_{L_2}\cos\,\theta]^{1/2}$$

It is essential that the frequency of output voltages E_{L_1}, E_{L_2} from the two inverters is the same. When θ is zero, $E_L = E_{L_1} + E_{L_2}$ and for $\theta = \pi$, $E_L = 0$ in case $E_{L_1} = E_{L_2}$. The angle θ can be varied by the firing angle control of two inverters. The series connection of inverters, called multiple inverter control, does not augment the harmonic content even at low output voltage levels.

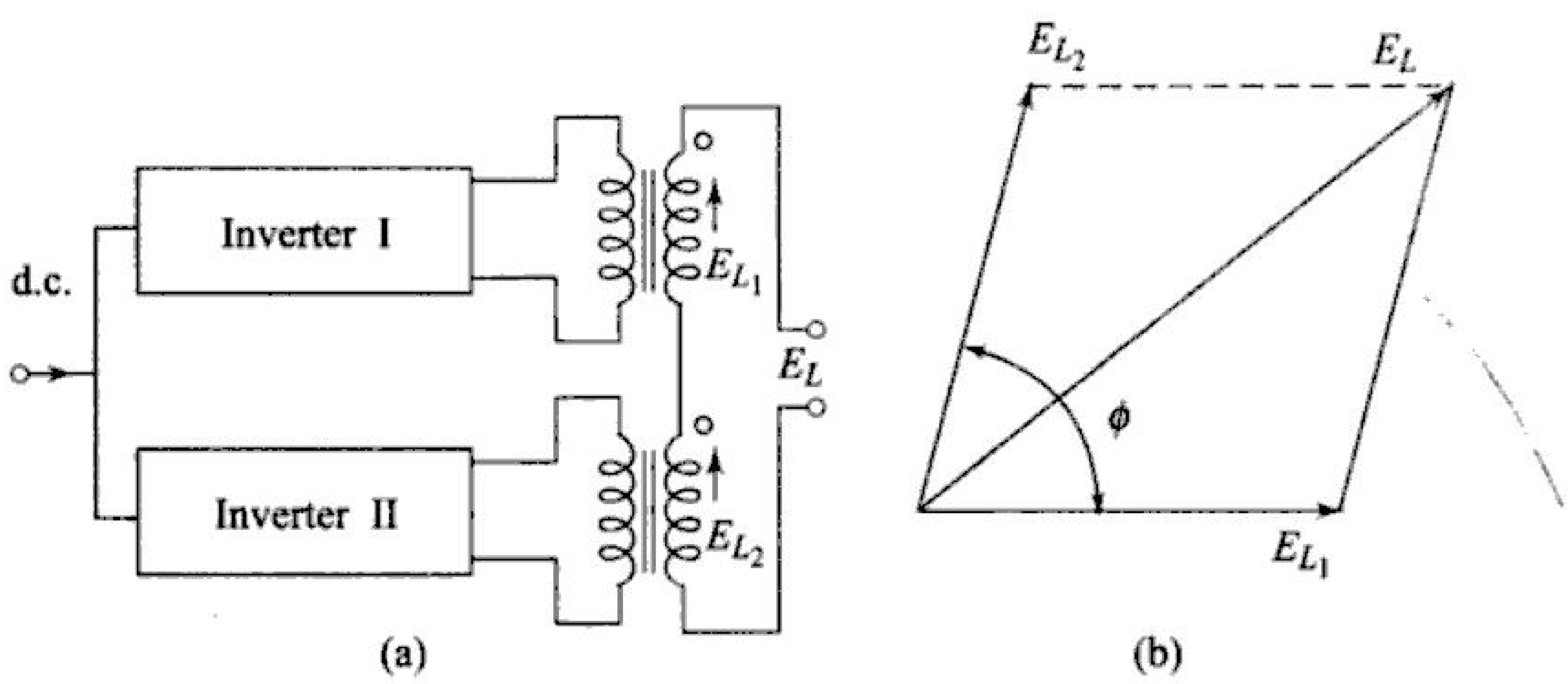

Fig. 9.12 *Internal control of inverters by their series connection*

2. Pulse-width Modulation Control The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters. In this method, a fixed d.c. input voltage is supplied to the inverter and a controlled a.c. output voltage is obtained by adjusting the on-and-off periods of the inverter devices. The PWM control has the following advantages:

(i) The output voltage control can be obtained without any additional components.

(ii) With this type of control, lower order harmonics can be eliminated or minimised along with its output voltage control. The filtering requirements are minimised as higher order harmonics can be filtered easily.

The main drawback of this method is that the SCRs used in this method must have very low turn-on and turn-off times (inverter-grade SCRs), therefore, they are very expensive.

The commonly used PWM control techniques are:

(a) Single-pulse width modulation (SPWM)

(b) Multiple-pulse width modulation (MPWM)

(c) Sinusoidal pulse width modulation (sin PWM)

9.6.3.1 Single-pulse Width Modulation

In single-pulse width modulation control, there is only one pulse per half-cycle and the width of the pulse is varied to control the inverter output voltage. The generation of gating signals and output voltage of single-phase full bridge inverters is shown in Fig. 9.13. As shown in Fig. 9.13, the gating signals are generated by comparing a rectangular reference signal of amplitude, E_R, with a triangular carrier wave of amplitude E_c. The fundamental frequency of output voltage is determined by the frequency of the reference signal. The pulse-width, P, can be varied from 0° to 180° by varying E_R from 0 to E_c. The ratio of E_R to E_c is the control variable and is defined as the ***amplitude modulation index***. The amplitude modulation index, or simply modulation index is

$$M = \frac{E_R}{E_c} \tag{9.30}$$

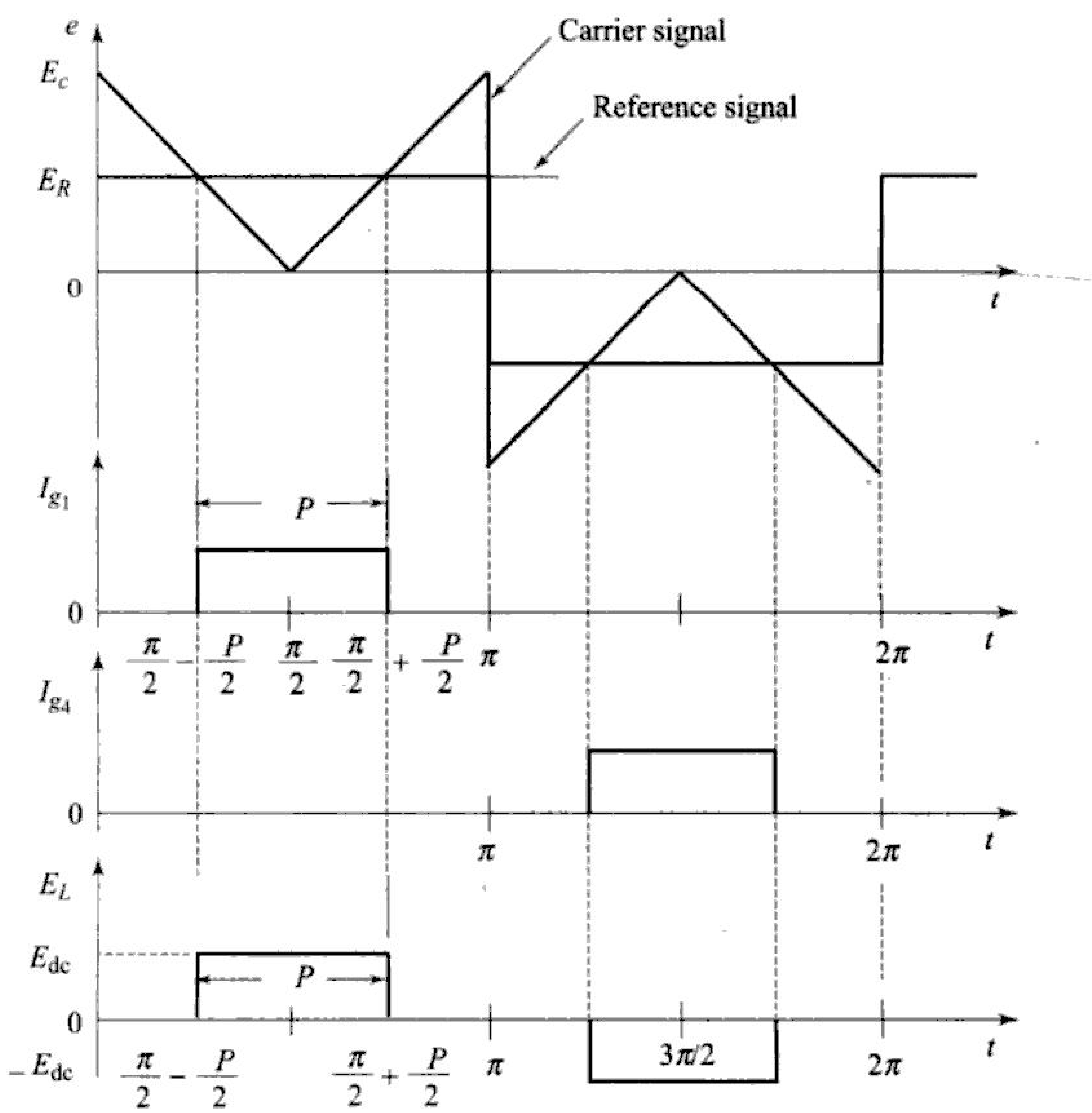

Fig. 9.13 *Single pulse-width modulation*

The following Fourier-series describes the waveform of E_L as

$$E_L = \sum_{n=1,3,5,\ldots}^{\infty} A_n \sin n\omega t + \sum_{n=1,3,5,\ldots}^{\infty} B_n \sin n\omega t \qquad (9.31)$$

where $$A_n = \frac{2}{\pi}\int_0^{\pi} E_{dc} \sin n\omega t \, d(\omega t) = \frac{2}{\pi}\int_{(\pi/2-p)}^{(\pi/2+p)} \sin n\omega t \, d(\omega t).$$

$$= \frac{4E_{dc}}{5\pi} \sin \frac{np}{2}$$

and $$B_n = \frac{2E_{dc}}{\pi}\int_{(\pi/2-p)}^{(\pi/2+p)} \cos n\omega t \, d(\omega t) = 0 \qquad (9.32)$$

Thus, $$E_L = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4E_{dc}}{n\pi} \sin \frac{np}{2} \sin n\omega t \qquad (9.33)$$

When pulse-width P is equal to its maximum value of π radians, then the fundamental component of output voltage E_L, from Eq. (9.33), has the peak value of

$$E_{L1m} = \frac{4E_{dc}}{\pi} \qquad (9.34)$$

The RMS output voltage can be found from

$$E_{Lrms} = \left[\frac{2}{\pi}\int_{(\pi-p)/2}^{(\pi+p)/2} E_{dc}^2 \, d(\omega t)\right]^{1/2} = E_{d.c} \cdot \sqrt{\frac{P}{\pi}} \qquad (9.35)$$

The peak value of the nth harmonic component from Eq. (9.33) is given by

$$E_{Lnm} = \frac{4E_{dc}}{n\pi} \sin \frac{np}{2} \qquad (9.36)$$

From Eqs (9.34) and (9.36), $$\frac{E_{Lnm}}{E_{L1m}} = \frac{\sin \frac{np}{2}}{n} \qquad (9.37)$$

The ratio as given by Eq. (9.37) is plotted in Fig. 9.14 for $n = 1$, $n = 3$, $n = 5$, 7 for different pulse widths. From these curves it may be observed that when the fundamental component is reduced to nearly 0.33, the amplitude of the third harmonic is also 0.33. When fundamental component is reduced to about 0.143, all the three harmonics (3, 5, 7) become almost equal to the fundamental. This shows that in this type of voltage control scheme, as great deal of harmonic content is introduced in the output voltage, particularly at low output voltage levels.

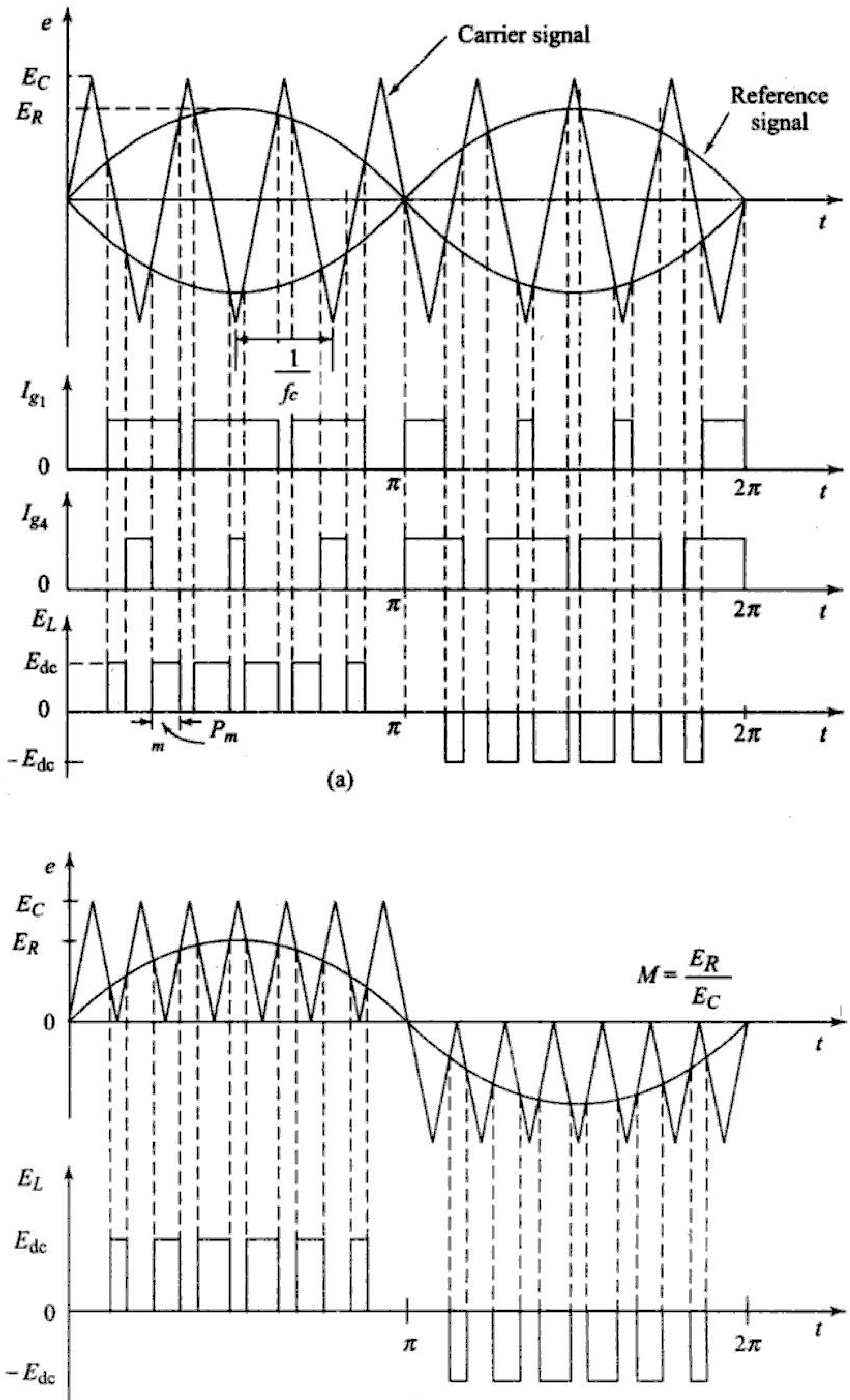

Fig. 9.17 *Sinusoidal pulse-width modulation*

harmonic frequency can be raised, which can then be filtered out easily. For $N_p = 5$, harmonics of the order of 9 and 11 become significant in the output voltage. It may be noted that the highest order of significant harmonic of modulated voltage-wave is centred around the carrier frequency, f_c.

(ii) For modulation index greater than one, lower order harmonics appear since for modulation index greater than one, pulse width is no longer a sinusoidal function of the angular position of the pulse.

9.7 PULSE-WIDTH MODULATED (PWM) INVERTERS

Square-wave inverters suffers from two major drawbacks:

(i) The output voltage of the inverter cannot be controlled for a fixed-source voltage. To achieve voltage control, the inverter must be fed either from a controlled ac-dc or dc-dc converter.

(ii) The output voltage contains appreciable harmonics (low-frequency range). Also, THD is very high.

Due to these drawbacks, square-wave inverter is rarely used in practice. To achieve voltage control within the inverter and to reduce the harmonic contents in the output voltage, PWM inverters are used. In PWM inverters, width of the output pulses are modulated to achieve the voltage control. PWM technique allows:

(i) Variation of output voltage within the inverter by varying the gain of the inverter. This allows the input d.c. voltage to be of fixed amplitude.

(ii) Variation of output frequency either by varying the number of pulses per half cycle of the output or by varying the period for each half-cycle with fixed number of pulses in each half-cycle.

(iii) Simultaneous variation of output voltage and frequency is also possible. So that V/F ratio can be kept constant. This feature is required in induction motor-drives.

(iv) Control of harmonics at the output of the inverter.

9.7.1 Pulse-Width Modulated Half-Bridge Inverters

With a half-bridge inverter, an output voltage of zero is not possible—the output voltage can be only positive or negative. Therefore, the output voltage is allowed to reverse instead of being zero. Figure 9.18 shows a PWM-waveform for a half-bridge inverter. We can control the output voltage by controlling the width 2δ.

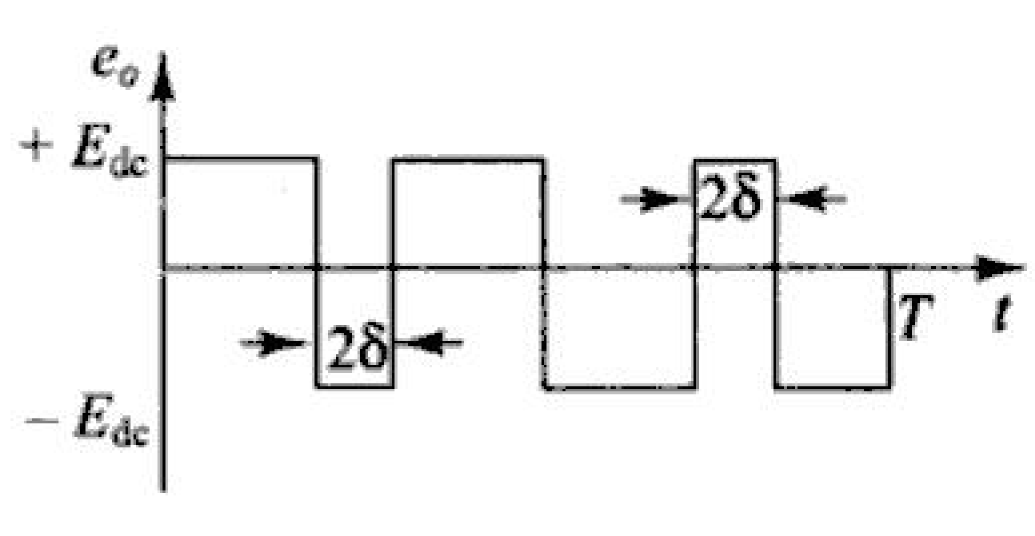

Fig. 9.18 *PWM in half-bridge inverter*

Sinusoidal PWM (Fig. 9.19) is commonly used with half-bridge inverters. A rectified sinusoidal reference signal is compared with a triangular carrier-wave. For the time during which the reference signal is higher than the carrier-wave, the switches are operated to produce positive-going pulses; otherwise, negative-going pulses are produced:

When $E_R > E_C$, S_1 is ON and $e_0 = +E_{dc}$

When $E_R < E_C$, S_2 is ON and $e_0 = -E_{dc}$

Switch conduction is also shown in Fig. 9.19.

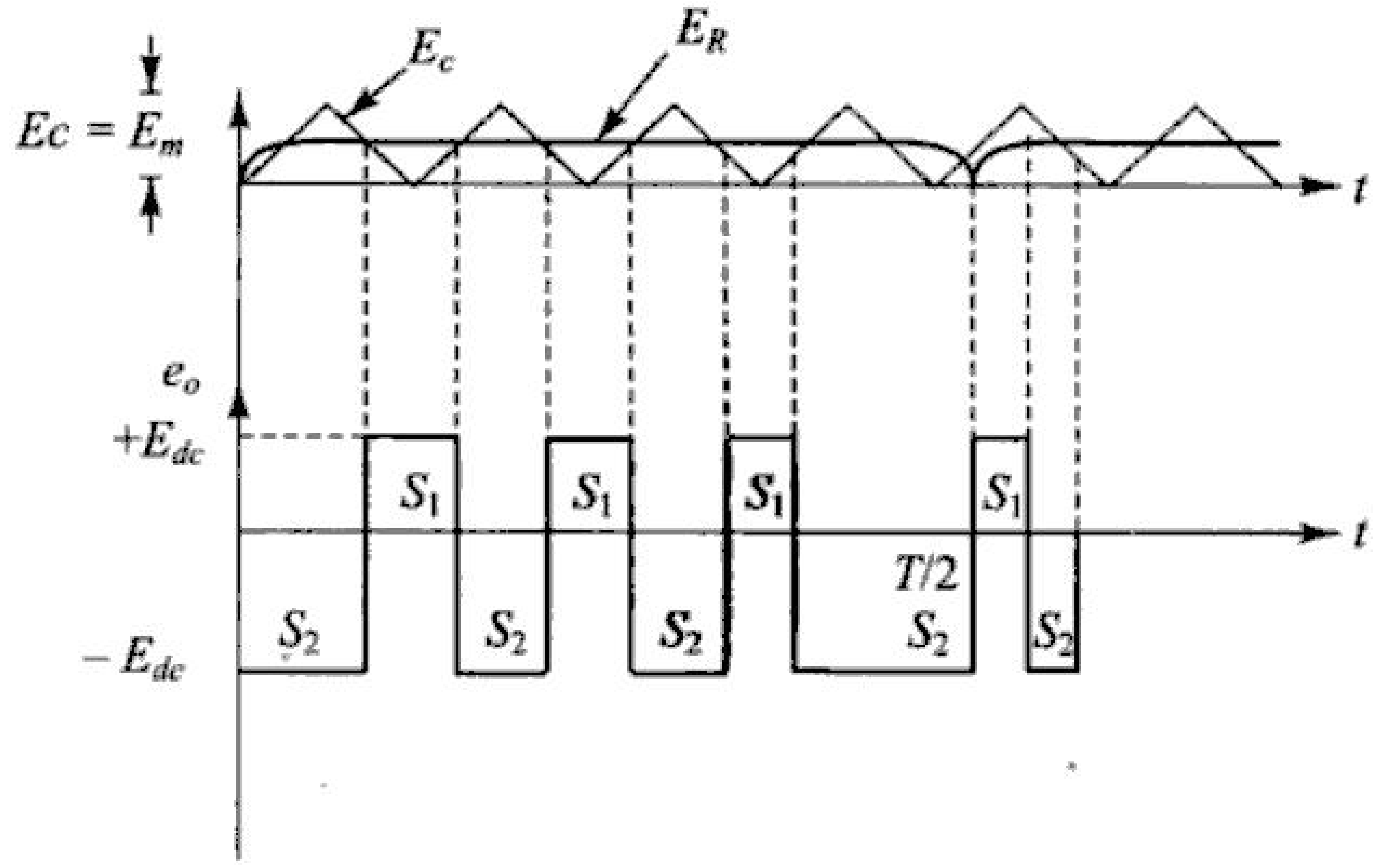

Fig. 9.19 *Sinusoidal PWM (S_1, S_2 are switches in half-bridge inverter)*

Let us define a parameter M_f, *called the carrier frequency ratio as*

$$M_f = \frac{\text{Frequency of the carrier signal.}}{\text{Frequency of the modulating signal}} = \frac{f_c}{f_m} \geq 1 \tag{9.43}$$

Circuit Analysis:-

(i) Fundamental Output Voltage The fundamental output voltage can be very easily found by assuming that the carrier ratio is quite high. Fundamental output voltage is proportional to the instantaneous modulation index and to the peak-value of the output voltage ($E_{dc}/2$).

$$\therefore \quad E_{0(\text{fund.})} = \begin{array}{c}\text{Instantaneous}\\\text{modulation}\\\text{index}\end{array} \times \begin{array}{c}\text{Peak value of}\\\text{output voltage}\end{array}$$

$$= \frac{E_m \sin w_m t}{E_c} \frac{E_{dc}}{2} = \frac{E_m}{E_c} \frac{E_{dc}}{2} \sin w_m t$$

but
$$M = \frac{E_m}{E_c}$$

$$\therefore \quad E_{0(\text{fund.})} = M \cdot \frac{E_{dc}}{2} \cdot \sin w_m t,\ M \leq 1 \tag{9.44}$$

But,
$$E_{0(\text{fund.})} = M \cdot \frac{E_{dc}}{2\sqrt{2}} \tag{9.45}$$

$$\therefore \quad E_{0(\text{fund.})} = \sqrt{2}\ E_{0(\text{fund.})} \cdot \sin (w_m t) \tag{9.46}$$

(v) Harmonics at the Output The carrier ratio as defined earlier is given by

$$M_F = f_c/f_m = 2 \cdot p$$

where p is the number of pulses per half-cycle. The harmonic frequencies present at the output can be expressed as

$$f_n = k_1 \cdot f_c + k_2 \cdot f_m$$

where f_n = frequency of the n^{th} harmonic

$$\therefore \qquad \frac{f_n}{f_m} = k_1 \cdot \frac{f_c}{f_n} + k_2$$

The order of the harmonic 'n' can be written as

$$n = \frac{f_n}{f_m} = k_1 \cdot m_f + k_2 \tag{9.58}$$

The carrier ratio is usually chosen as odd number. The waveform then will have a quarter-wave symmetry and only odd harmonics are present. This is one of the requirements of a PWM signal. Now only odd harmonics are present hence if k_1 is odd then k_2 is even and vice versa. Therefore, the harmonic present at the output are

$$\left.\begin{aligned} n &= M_f, M_{f\pm 2}, M_{f\pm 4}, M_{f\pm 6}, \ldots \\ n &= 2M_{f\pm 1}, 2M_{f\pm 3}, 2M_{f\pm 5}, \ldots \\ n &= 3M_f, 3M_{f\pm 2}, 3M_{f\pm 4}, 3M_{f\pm 6} \ldots \end{aligned}\right\} \tag{9.59}$$

Frequency spectrum of the PWM signal is shown in Fig. 9.20. The sidebands can be clearly seen. The centre frequencies are M_f, $2M_f$, $3M_f$, ... The amplitude

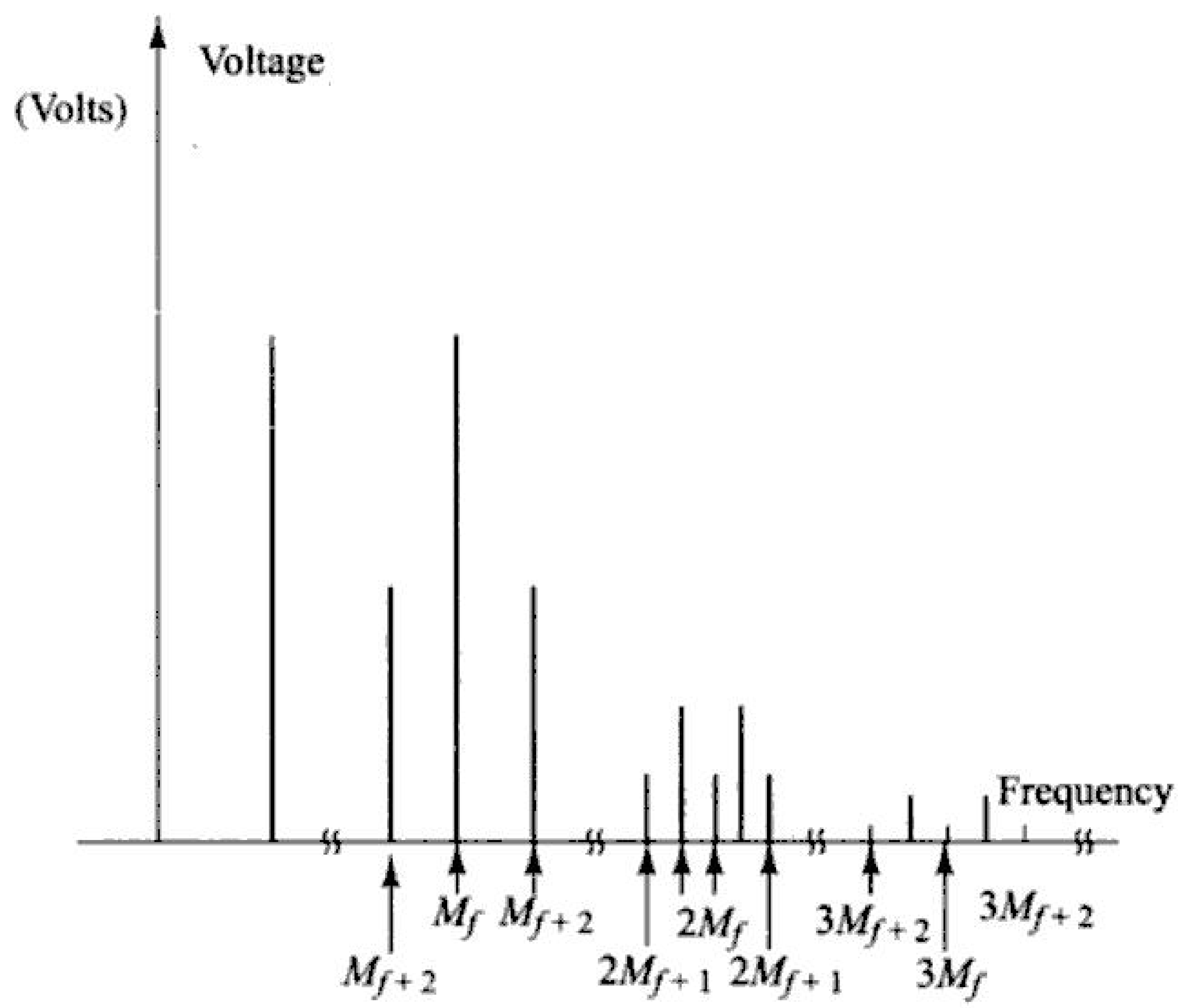

Fig. 9.20 *Frequency-spectrum for bipolar sinusoidal PWM-output in half-bridge-inverter*

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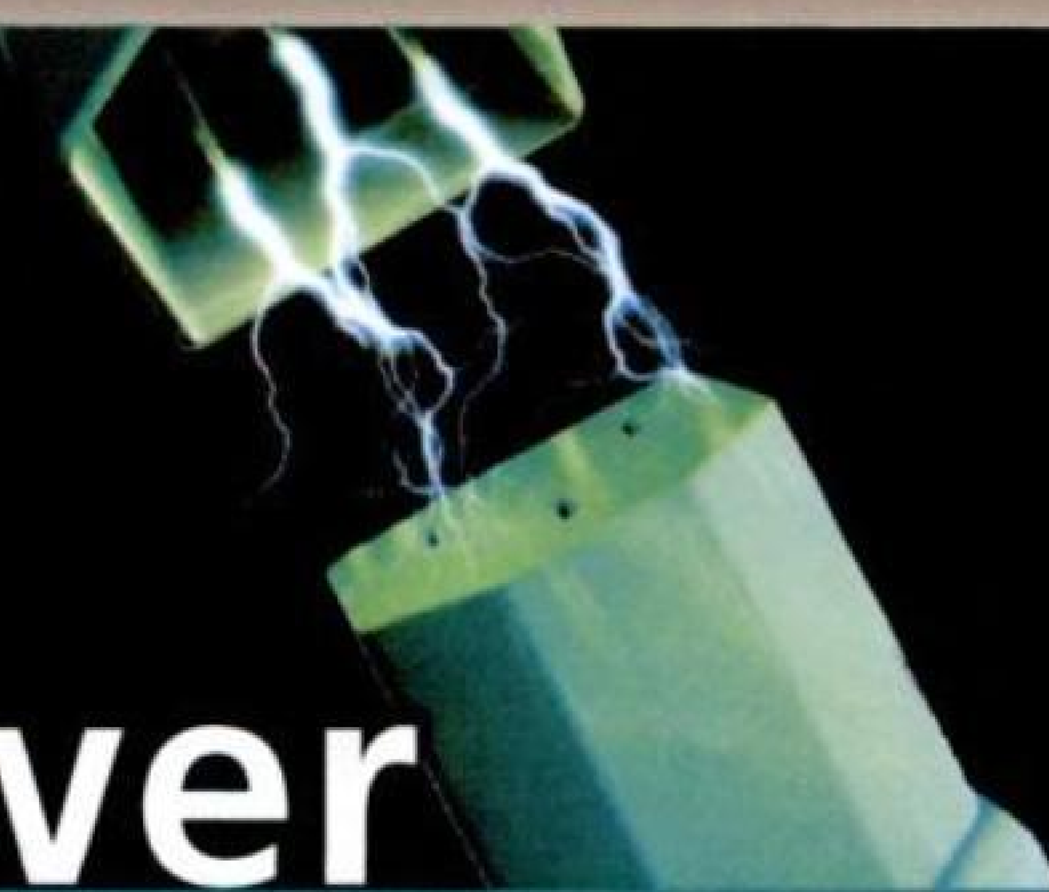

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