# LeonardoSpectrum Release Notes

Software Release v2002a

March 2002



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# LeonardoSpectrum Release v2002a

Product Enhancements New Technologies Fixed Bugs Unix O/S Patch Details Known Problems

# **Product Enhancements**

## Altera LogicLock Methodology is Now Supported

LogicLock incremental design is a new methodology available exclusively to Quartus II users. Using the LogicLock methodology, each module in a design is implemented independently. LeonardoSpectrum supports this methodology by allowing you to assign a LOGICLOCK attribute to one or more modules using the Module PowerTab of the Constraints FlowTab. This attribute is passed to Quartus II through a Tcl file that tells Quartus II to implement the module in a particular area of the chip.

# **Xilinx Support**

- Virtex-II and Virtex-II Pro MULT18X18S pipeline multiplier support has been added
  - Virtex-II devices have synchronous multiplier cells (MULT 18X18S) with built-in register banks for the outputs. These cells are useful for implementing very fast pipelined multipliers. With this release, LeonardoSpectrum uses this cell to build pipeline multipliers with a large number of stages. For pipeline designs with less than two stages, the regular MULT18X18 cell is used which is generally more efficient for this type of design.
- Virtex-II SRL dynamic mode is now supported
- Virtex-II RAM inferencing has been improved

# **New Technologies**

The following devices are now supported.

# **New Actel Devices**

#### **ProASIC**PLUS

LeonardoSpectrum now supports Actel's newest technology ProASICPLUS. The library name is listed as PA in the Actel technology list.

## **Other Devices Supported**

RT54SX Family			
Default Speed Gra	Default Speed Grade: -1		
Speed Grades sup	Speed Grades supported: -1, STD		
	New Devices Supported		
RT54SX72	CQFP208, CQFP256		

RT54SXS Family			
Default Speed Grade: -1			
Speed Grades supp	Speed Grades supported: -1, STD		
New Devices Supported			
RT54SX72S	CQFP208, CQFP256		

### **New Altera Devices**

#### **Stratix Device Support**

The new Stratix architecture features eight times more RAM bits as well as dedicated DSP functionality, on-chip termination resistors and advanced system clock management features. LeonardoSpectrum now supports the following Stratix devices.

Stratix Devices	
EP1S10	F780C
EP1S20	F780C
EP1S25	F780C, F1020C
EP1S30	B956C, F1020C
EP1S40	B956C, F1020C, F1508C
EP1S60	B956C, F1020C, F1508C
EP1S80	B956C, F1508C

Stratix Speed Grades	
Default Speed Grade: 5	
Speed Grades supported: 5, 6, 7	

Stratix Wire Load	
stratix_default	stratix_bc
stratix_wc	stratix_megalab_default

## **New Lattice Devices**

MACH Devices

	MACH Devices
MACH4A	M4A3: 384/160, 512/160, 512/192, 512/256
Packages	44PLcc 44TQFP 48TQFP 100TQFP 144TQFP 208PQFP

- ispMACH 5000MX CPLD
- ispGDX2 Crossbar Switch

# **New QuickLogic Devices**

	<b>Eclipse Devices Supported</b>	
QL6250	PT280 PS484 PB516 PS672	
QL6325	PT280 PS484 PB516 PS672	
QL6500	PT280 PS484 PB516 PS672	
QL6500	PT280 PS484 PB516 PS672	
QL6600	PT280 PS484 PB516 PS672	
Process	Typical Case (default), Best Case, Worst Case	

QuickDSP	
Devices Supported	
QL7100	PT280 PS484 PB516 PS672
QL7120	PT280 PS484 PB516 PS672
QL7160	PT280 PS484 PB516 PS672
QL7180	PT280 PS484 PB516 PS672
Process	Typical Case (default), Best Case, Worst Case

	QuickPCI	
Default Spee	d Grade: -1	
Speed Grade	s supported: 0, -1, -2, -3, -4	
Devices Supported		
QL5030	PF144 CF208 PQ208 PB256 PB456 BG484	
QL5130	PF144 CF208 PQ208 PB256 PB456 BG484	
QL5032	PF144 CF208 PQ208 PB256 PB456 BG484	
QL5232	PF144 CF208 PQ208 PB256 PB456 BG484	
QL5064	PF144 CF208 PQ208 PB256 PB456 BG484	
Process	Typical Case (default), Best Case, Worst Case	

QuickRAM		
Default Speed	Default Speed Grade: -1	
Speed Grades	supported: 0, -1, -2, -3, -4	
Devices Supported		
QL4009	CF208 PB256 PB456 PF100 PF144 PQ208 PQ240	
QL4016	CF208 PB256 PB456 PF100 PF144 PQ208 PQ240	
QL4036	CF208 PB256 PB456 PF100 PF144 PQ208 PQ240	
QL4058	CF208 PB256 PB456 PF100 PF144 PQ208 PQ240	
QL4090	CF208 PB256 PB456 PF100 PF144 PQ208 PQ240	
Process	Typical Case (default), Best Case, Worst Case	

# **New Xilinx SPARTAN-IIE Devices Supported**

Spartan-IIE Devices Supported		
Internal Library N	Internal Library Name: xis2e	
2s50e	ft256, pq208, tq144	
2s100e	ft256, fg456, pq208, tq144	
2s150e	ft256, fg456, pq208	
2s200e	fg256, fg456, pq208	
2s300e	fg256, fg456, pq208	

Spartan-IIE Speed Grades	
Default Speed Grade: -7	
Speed Grades supported: -6, -7	

Spartan-IIE Wire Load Tables		
xis2e50-6_wc	xis2e50-7_wc	
xis2e100-6_wc	xis2e100-7_wc	
xis2e150-6_wc	xis2e150-7_wc	
xis2e100-6_wc	xis2e100-7_wc	
xis2e200-6_wc	xis2e200-7_wc	
xis2e300-6_wc	xis2e300-7_wc	

# **New Xilinx VIRTEX-II Pro Devices Supported**

VIRTEX-II Pro Devices Supported		
Internal Library Name: xcv2p		
2VP2	fg256, fg456	
2VP4	fg256, fg456	
2VP7	fg456, bg575	
2VP20	bg575, ff1152	
2VP50	ff1152	

VIRTEX-II Pro Speed Grades		
Default Speed Grade: -7		
Speed Grades supported: -6, -7		

VIRTEX-II Pro Wire Load Tables		
xcv2p-2-7_wc	xcv2p-2-6_wc	
xcv2p-4-7_wc	xcv2p-4-6_wc	
xcv2p-7-7_wc	xcv2p-76_wc	
xcv2p-20-7_wc	xcv2p-20-6_wc	
xcv2p-50-7_wc	xcv2p-50-6_wc	

#### **New CoolRunner-II Devices**

CoolRunner-II		
Default Speed Gra	nde: -7	
Speed Grades supported: -4, -5, -7, -10		
Devices Supported		
X2C32	PC44, VQ44, CP56	
X2C64	PC44, VQ44, CP56, VQ100, CP132	
X2C128	VQ100, CP132, TQ144, FT256	
X2C256	VQ100, CP132, TQ144, VQ100, FT256	

# **Fixed Bugs**

**DR296844** LeonardoSpectrum places a buf on the wrong wire when an inout port is joined to a net with another port.

**DR297760** LeonardoSpectrum failed to issue a warning or an error when it found a missing or repeated port in the HDL source.

**DR300196** LeonardoSpectrum abnormally terminates while synthesizing a customer design.

**DR301435** Spectrum incorrectly reports that a design won't fit in a Xilinx Coolrunner device.

**DR301484** Unable to change process (speed) variable from the LeonardoSpectrum GUI

**DR302148** LeonardoSpectrum incorrectly reports an error when parsing an else'0' clause without a space.

**DR302346** LeonardoSpectrum generates misleading messages while inferring a counter.

**DR302347** LeonardoSpectrum abnormally terminates while synthesizing a customer design.

**DR303026** LeonardoSpectrum output causes an error in Max+Plus II.

**DR303456** Optimization for Altera technology producing overly complicated logic.

**DR303551** Not possible to read a constraint file from the Input FlowTab.

**DR303554** In a Xilinx CoolRunner design, macrocells are in-correctly used instead of gates.

**DR303630** LeonardoSpectrum uses incorrect speed grade nomenclature for Altera Mercury.

**DR304128** Parameter which is not a constant causes LeonardoSpectrum to abnormally terminate.

**DR304178** exclude\_gates variable has no effect on the APEX20 Family.

**DR304678** Design appears to compile correctly but can't be read into LeonardoSpectrum.

**DR304963** do\_ip command does not do boundary optimization.

**DR304976** STARTUP\_VIRTEX2 block gets optimized away.

**DR305276** LeonardoSpectrum accepts bad port assignments on customer design

**DR305648** Insertion of a BUFG in a special case circuit creates an illegal logic structure.

**DR305721** LeonardoSpectrum error tracing mechanism fails if the source line number is greater than 16 bits.

**DR305848** Constraint file is lost after a READ command is executed.

**DR305984** Actel PRO ASIC flow abnormally terminates on demo design.

**DR306021** Wrong logic produced due to inverted clock for CoreGen BlockRAM.

**DR306445** (**DR310128**) LeonardoSpectrum fails to complete boundary optimization on customer design.

**DR306768** Customer design causes LeonardoSpectrum to terminate prematurely.

**DR307208** Unable to modify Editor preferences.

**DR307244** Verilog file created by HDL Designer causes LeonardoSpectrum to crash.

**DR307961** Internal signal clock buffer cells exceed Actel 42MX library limit.

**DR308008** LeonardoSpectrum with the Actel A500k technology selected abnormally terminates while writing EDIF.

**DR309018** LeonardoSpectrum GUI crashes when writing EDIF for Actel A500K.

**DR309597** VHDL file with the same functionality but different coding style produces different sized circuits.

**DR309597** Request to add Altera LogicLock support to the LeonardoSpectrum GUI.

**DR310113** LeonardoSpectrum generates an incorrect multiple-drivers error message on a customer design.

**DR310131 (DR310297)** LeonardoSpectrum incorrectly optimizes the neq operator in a customer design.

**DR310619** LeonardoSpectrum incorrectly infers RAM in customer's Virtex-E design.

**DR311656** LeonardoSpectrum incorrectly maps the output ports of a RAM16X1D cell on Solaris.

**DR312749** LeonardoSpectrum abnormally terminates on a custom ASIC library with no INV cell.

**DR315362** LeonardoSpectrum produces clock enable logic that is too complex.

# **Unix O/S Patch Details**

Starting with Release 2001.1d, LeonardoSpectrum supports MainWin 3.4 software running on the Solaris 7/8 and HP-UX 10.20/11.00 operating systems. MainWin 3.4 requires certain patches in order to run properly. You may install operating system patches before or after you install LeonardoSpectrum. The paragraphs that follow outline the required patches for each operating system.

#### **Sun Microsystems Patches**

#### **Detecting the Graphics Card**

On Solaris systems, a patch is sometimes required that is specific for the installed graphics card. Use the instructions that follow to determine which graphics card is installed on your system.

To verify that an FFB accelerator is installed on the system (Creator 3D), enter

```
% dmesg | grep ffb
```

The output should be:

```
SUNW,ffb0 at root: UPA 0xle 0x0
SUNW,ffb0 is /SUNW,ffb@le,0
stdout is (/SUNW,ffb@le,0) major (53) minor (0)
```

To verify that an AFB accelerator is installed on the system (Elite 3D), enter

```
% dmesg | grep afb
```

#### The output should be:

```
SUNW,afb0 at root: UPA 0xle 0x0 SUNW,afb0 is /SUNW,afb@le,0
```

stdout is major <79> minor <0>

#### To detect graphics cards (alternate method), enter

% ls /dev/fbs/\*

You can tell which graphic card is present by the output from the command; refer to Table 0-1.

Table 0-1. Detecting a Graphics Card

Output	Graphics Card	
/dev/fbs/m640	PGX graphics card	
/dev/fbs/afb*	Elite3D graphics card	
/dev/fbs/ffb*	Creator/Creator3D graphics card	
/dev/fbs/gfxp*	PGX32 (Raptor GFX) graphics card	
/dev/fbs/cgsix*	GX graphics card	
/dev/fbs/leo*	ZX graphics card	
/dev/fbs/sx*	SX graphics card	
/dev/fbs/tcx*	TCX graphics card	

#### **Solaris 8 Patches**

The following tables describe the required patches for Solaris 8 operating systems. Patches are available for download at the following Sun web site: http://sunsolve.sun.com

Table 0-2. Patches for All Solaris 8 systems

Patch	Description	Notes
108434-01	Shared library fix for C++ runtime.	Shared library fix for C++ runtime.

#### **Solaris 7 Patches**

The following tables describe the required patches for Solaris 7 operating systems. Patches are available for download at the following Sun web site: http://sunsolve.sun.com

Table 0-3. Patches for All Solaris 7 systems

Patch	Description	Notes
106300-07	Sun OS 5.7 Shared library patch for C++.	Required for Mentor Graphics D.2 environment.
106327-06	Sun OS 5.7 Shared library patch for C++.	Required for Mentor Graphics D.2 environment.
106725-02		Required for Mentor Graphics D.2 environment.
106748-04		Required for Mentor Graphics D.2 environment.
107200-11		Required for Mentor Graphics D.2 environment.
12/8/99 Recommended Patch Cluster		Required for Mentor Graphics D.2 environment.

Table 0-4. Configuration-Specific Patches for Solaris 7 systems

Patch	Description	Notes
107851-11 (or later)	Patch for PGX32 (Raptor GFX) graphics card	PGX32 2.1 graphics patch
106146-16 (or later)	M64 graphics card	For PGX (M64 graphics card)
106145-17 (or later)	Creator 7 FFB graphics card	Patch for Creator graphics card
106144-21 (or later)	Elite3D graphics card	For Elite3D AFB graphics patch
106147-06 (or later)	Supplemental patch for Elite 3D and Creator graphics cards	VIS/XIL graphics patch

106148-12	Required supplemental patch for	XF8 graphics patch
(or later)	Elite 3D and Creator graphics	
	cards	

#### HP-UX 10.20 and HP-UX 11.00 Patches

The following patches are required on the HP-UX 10.20 and HP-UX 11.00 operating system to allow LeonardoSpectrum with MainWin 3.4 to run appropriately.

Patches are available on the following HP WEB sites:

```
http://us-support.external.hp.com
http://europe-support.external.hp.com
```

Table 0-5. Patches for All HP-UX 10.20 systems

Patch	Description	Notes
PHSS_19739	s700_800 10.20 HP DCE/9000 1.5 cumulative patch	Fixes problems with threads.
PHCO_19434	s700_800 10.20 csh(1) cumulative patch	Fixes crash of csh exit of Mainwin.
PHSS_17872	HP aC++ runtime libraries (ACC A.01.21)	
PHSS_17159	s700_800 10.20 Xserver cumulative patch	Fixes X server crach with multiple-rectangle

Table 0-6. Patches for All HP-UX 11.00 systems

Patch	Description	Notes
PHSS_19866	s700_800 11.00 X/Motif2.1 Dev Kit Mar99 Periodic Patch	X patch.
PHSS_17327	s700_800 11.00 ld(1) and linker tools cumulative patch	Linker patch.

## **Known Problems**

### **Internet Explorer 5.0 is Required for Windows NT**

If you plan to run the LeonardoSpectrum GUI on the Windows NT Operating System, you must install Internet Explorer 5.0 or higher.

## **Opening Files on Windows 2000**

The LeonardoSpectrum Open Files dialog box opens starting with the current working directory. On Windows 2000, the Open Files dialog box may open on the directory where the last file was opened, even if that file was opened by another application. The Windows 2000 operating system has been identified as the source of the problem and a bug report has been submitted to Microsoft.

# **Designs with Long Chains of Arithmetic Operators May Experience Long Run Times**

If your design contains a long chain of arithmetic operators, you may experience a long optimization run time. The workaround to this problem is to turn off Optimization Pass 4.