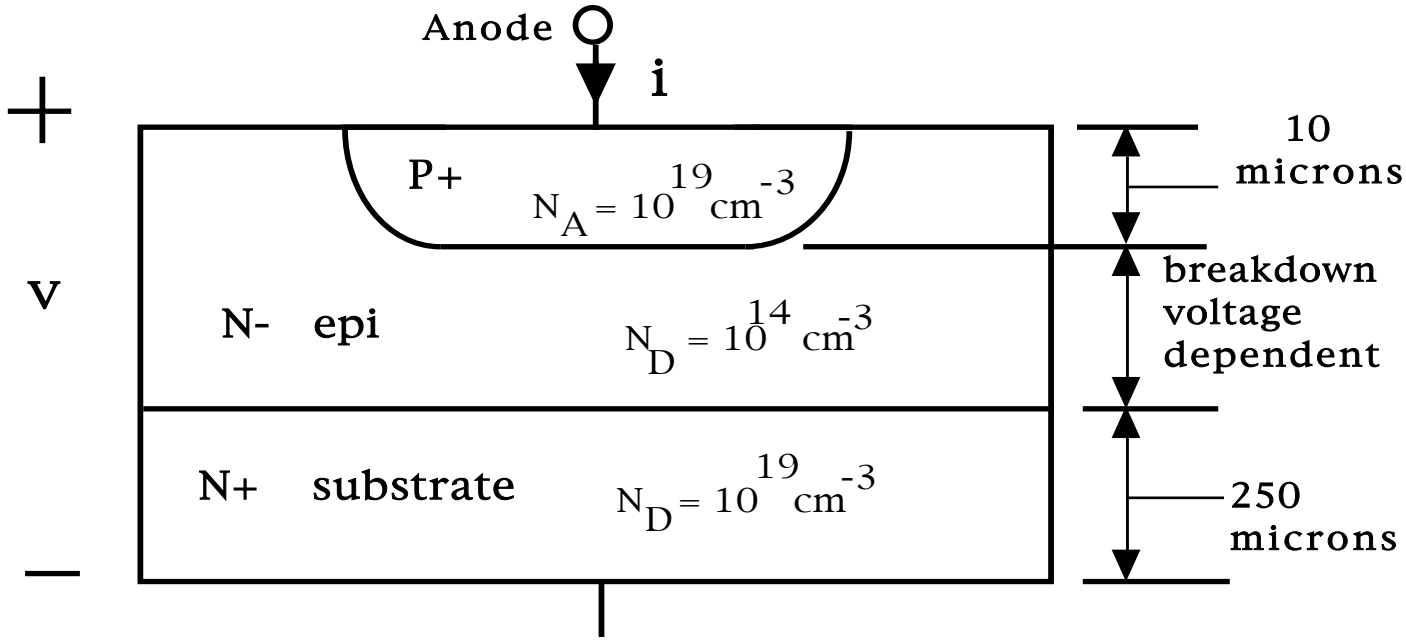
Lecture Notes

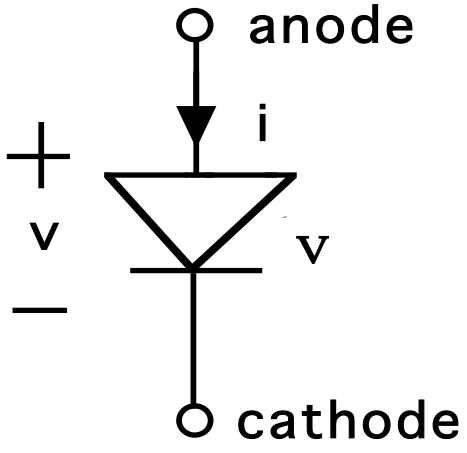
Diodes for Power Electronic Applications

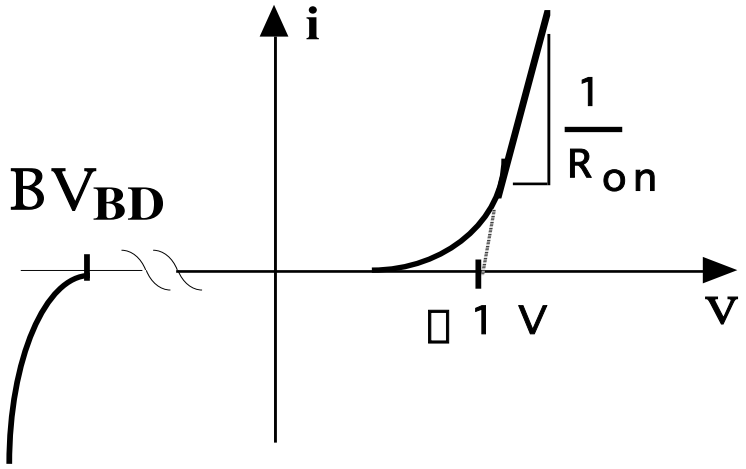
OUTLINE

- PN junction power diode construction
- Breakdown voltage considerations
- On-state losses
- Switching characteristics
- Schottky diodes
- Modeling diode behavior with PSPICE

Basic Structure of Power Semiconductor Diodes

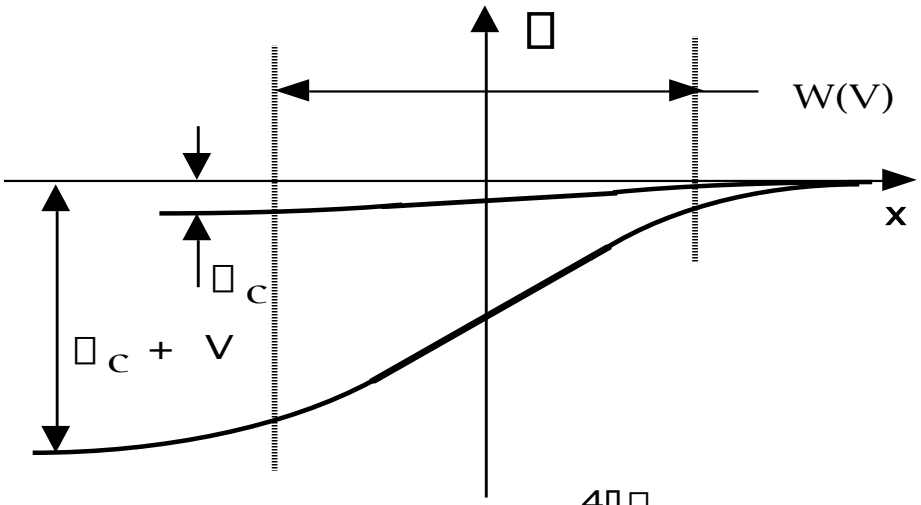






Breakdown Voltage Estimate - Step Junction

- Non-punch-through diode. Drift region length $W_d > W(BV_{BD})$ = length of space charge region at breakdown.
- $W(V) = W_o\sqrt{1+V/\phi_c}$
- $W_o = \sqrt{\dfrac{2\varepsilon\phi_c(N_a+N_d)}{qN_aN_d}}$



- $E_{max} = \dfrac{2\phi_c}{W_o}\sqrt{1+V/\phi_c}$
- Power diode at reverse breakdown: $N_a \gg N_d$; $E = E_{BD}$; $V = BV_{BD} \gg \phi_c$
- $W^2(BV_{BD}) = \dfrac{W_o^2 BV_{BD}}{\phi_c}$; $W_o^2 = \dfrac{2\varepsilon\phi_c}{qN_d}$
- $(E_{max})^2 = (E_{BD})^2 = \dfrac{4\phi_c}{W_o^2}BV_{BD}$
- Solve for $W(BV_{BD})$ and BV_{BD} to obtain (put in Si values)

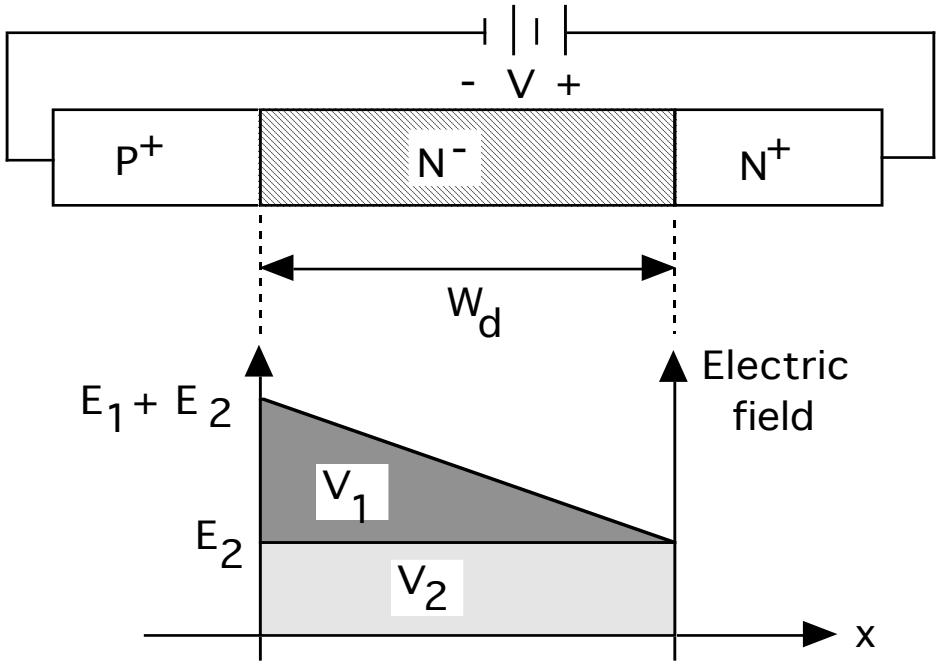
$$BV_{BD} = \frac{\varepsilon E_{BD}^2}{2qN_d} = \frac{1.3\times10^{17}}{N_d} \text{ ; [V]}$$

$$W(BV_{BD}) = \frac{2BV_{BD}}{E_{BD}} = 10^{-5}\,BV_{BD} \text{ ; [}\mu\text{m]}$$

- Conclusions
  1. Large BV_{BD} (10^3 V) requires $N_d < 10^{15}$ cm^{-3}
  2. Large BV_{BD} (10^3 V) requires N^- drift region > 100 μm

Breakdown Voltage - Punch-Through Step Junction

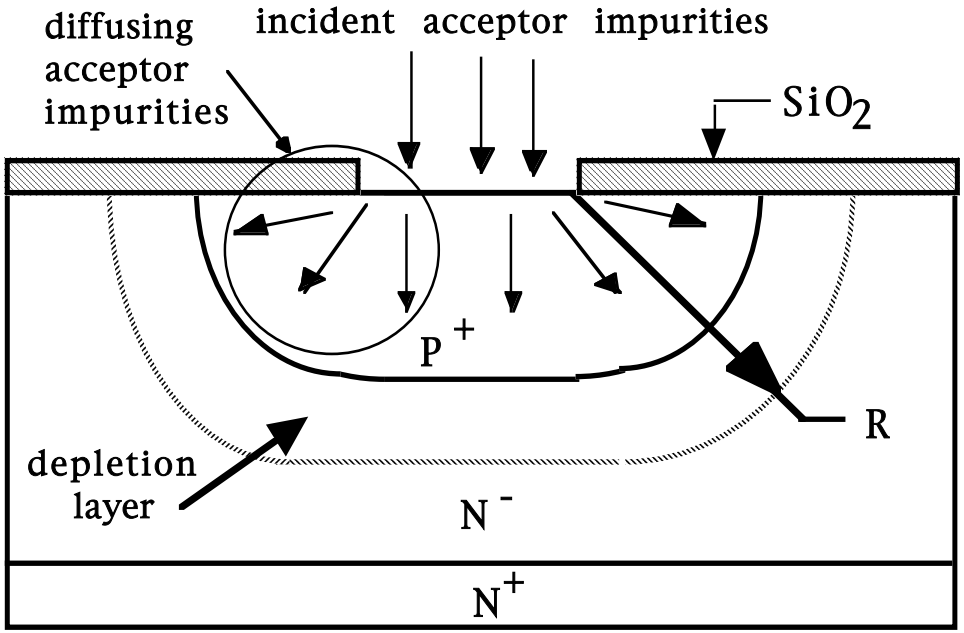
- Punch-through step junction - $W(BV_{BD}) > W_d$



- $E_1 = \frac{qN_dW_d}{\varepsilon}$; $V_1 = \frac{qN_dW_d^2}{2\varepsilon}$
- $V_2 = E_2 W_d$

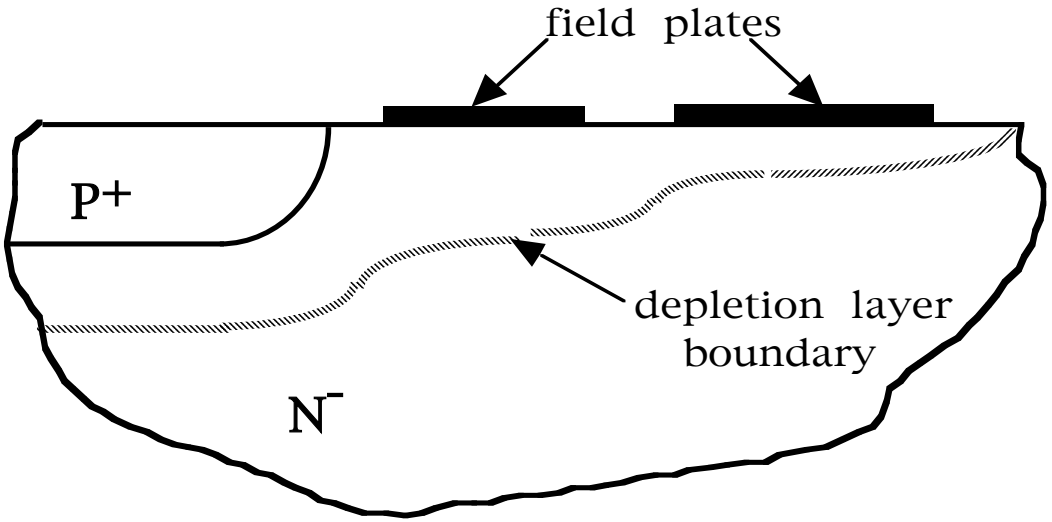
- At breakdown:
  - $V_1 + V_2 = BV_{BD}$
  - $E_1 + E_2 = E_{BD}$
- $BV_{BD} = E_{BD} W_d - \frac{qN_dW_d^2}{2\varepsilon}$
- If $N_d << \frac{\varepsilon(EBD)^2}{2q(BV_{BD})}$ (required value of N_d for non-punch-thru diode), then
  - $BV_{BD} \approx E_{BD} W_d$ and
  - W_d(Punch-thru) $\approx 0.5\ W_d$(non-punch-thru)

Effect of Space Charge Layer Curvature

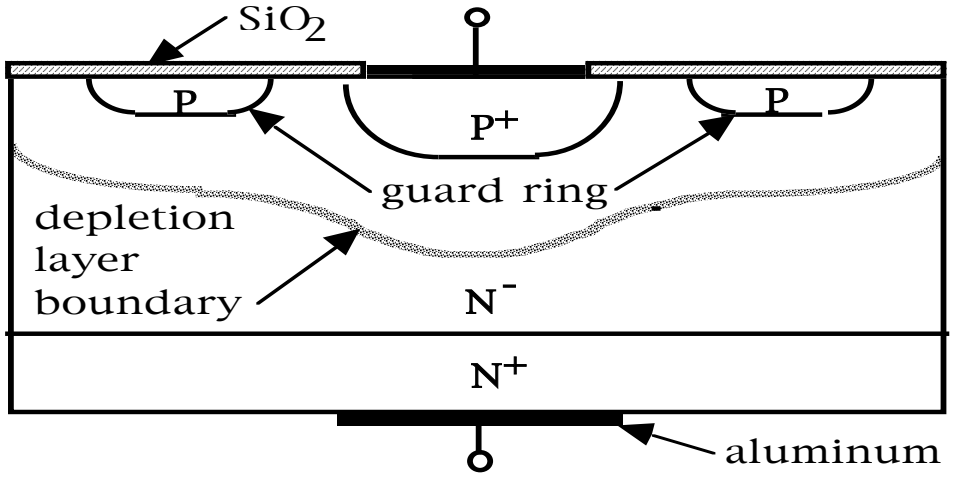


- Impurities diffuse as fast laterally as vertically
- Curvature develops in junction boundary and in depletion layer.
- If radius of curvature is comparable to depletion layer thickness, electric field becomes spatially nonuniform.
- Spatially nonuniform electric field reduces breakdown voltage.
- $R > 6\ W(BV_{BD})$ in order to limit breakdown voltage reduction to 10% or less.
- Not feasible to keep R large if BV_{BD} is to be large (> 1000 V).

Control of Space Charge Layer Boundary Contour

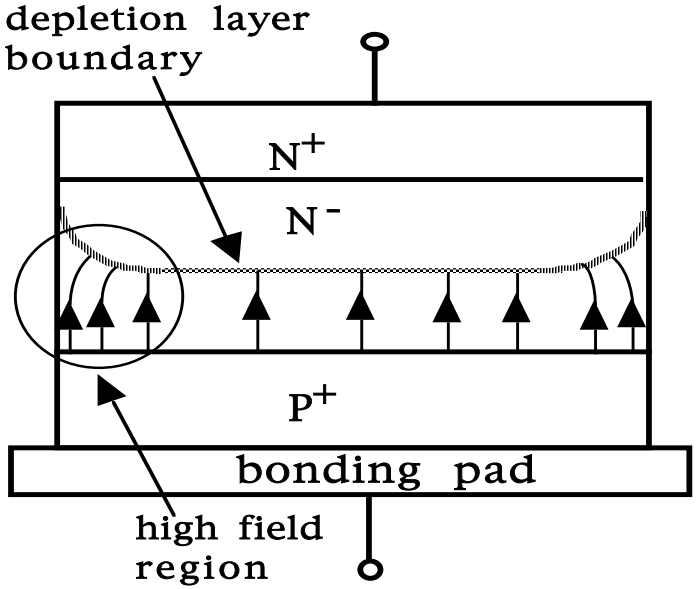


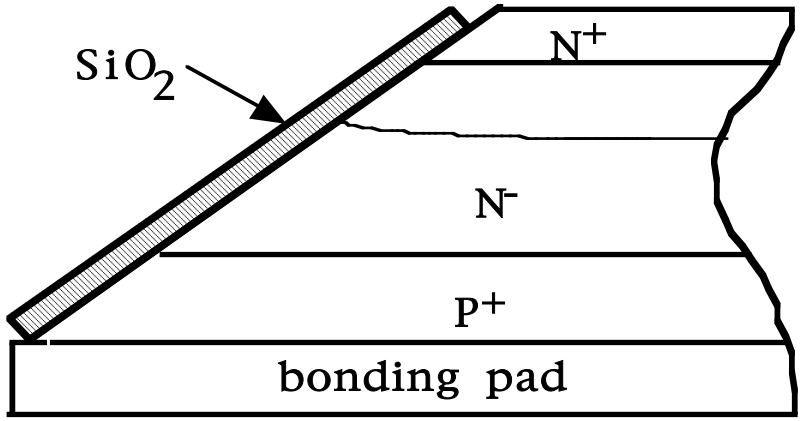
- Electrically isolated conductors (field plates) act as equipotential surfaces.
- Correct placement can force depletion layer boundary to have larger radius of curvature and t;hus minimize field crowding.



- Electrically isolated p-regions (guard rings)has depletion regions which interact with depletion region of main pn junction.
- Correct placement of guard rings can result in composite depletion region boundary having large radius of curvature and thus minimize field crowding.

Surface Contouring to Minimize Field Crowding

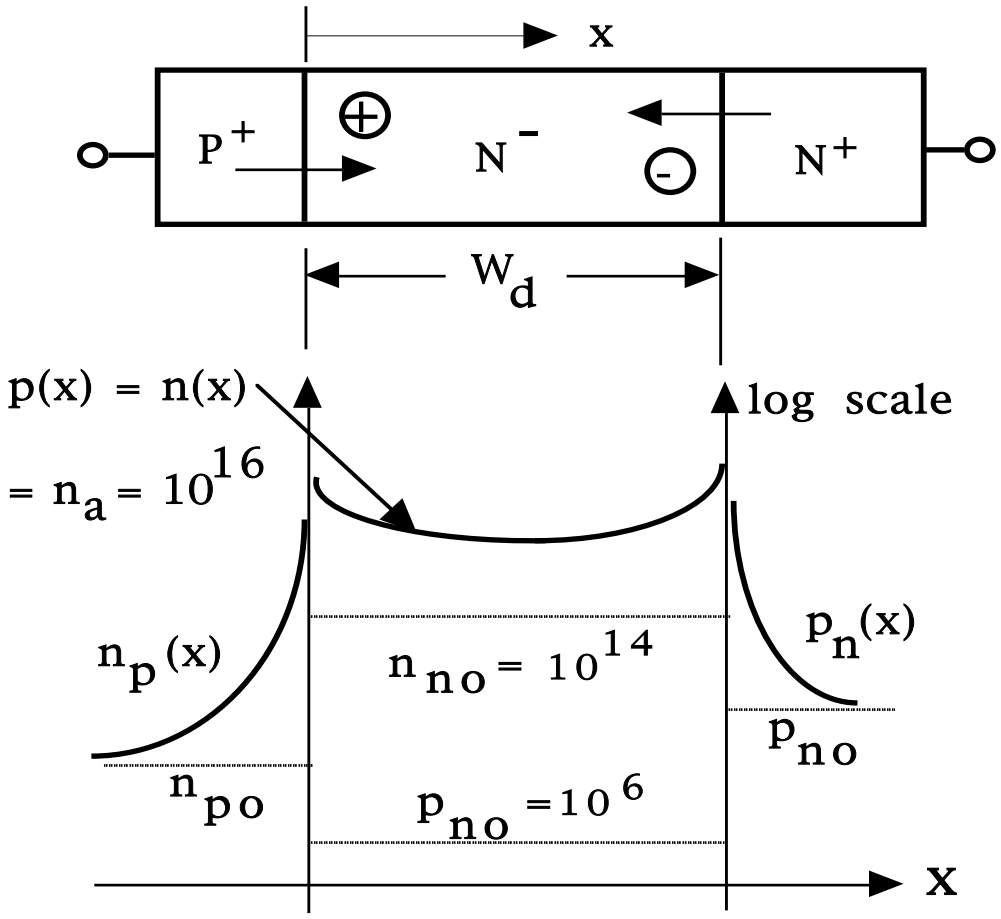




- Large area diodes have depletion layers that contact Si surface.
- Difference in dielectric constant of Si and air causes field crowding at surface.
- Electric fields fringing out into air attract impurities to surface that can lower breakdown voltage.

- Proper contouring of surface can mimimize depletion layer curvature and thus field crowding.
- Use of a passivation layer like SiO_2 can also help minimize field crowding and also contain fringing fields and thus prevent attraction of impurities to surface.

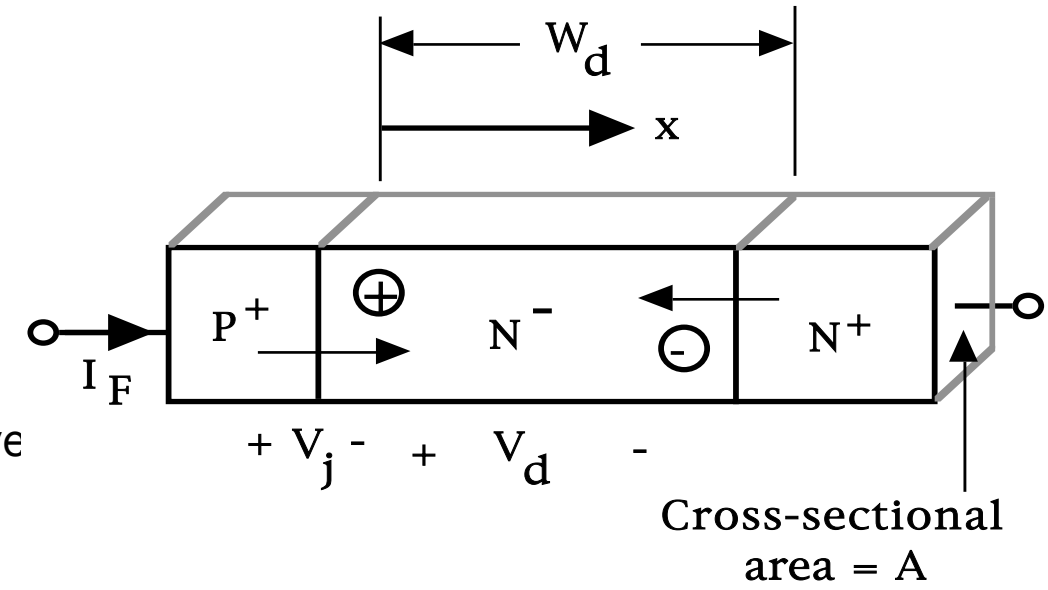
Conductivity Modulation of Drift Region



- Forward bias injects holes into drift region from P^+ layer. Electrons attracted into drift region from N^+ layer. So-called double injection.
- If $W_d \leq$ high level diffusion length L_a , carrier distributions quite flat with $p(x) \approx n(x) \approx n_a$.
- For $n_a >>$ drift region doping N_d, the resistance of the drift region will be quite small. So-called conductivity modulation.
- On-state losses greatly reduced below those estimated on basis of drift region low-level (N_d) ohmic conductivity.

Drift Region On-State Voltage Estimate

- $I_F = \frac{Q_F}{\tau} = \frac{q \cdot A \cdot W_d \cdot n_a}{\tau}$; Current needed to maintain stored charge Q_F.
- $I_F = \frac{q \cdot [\mu_n + \mu_p] \cdot n_a \cdot A \cdot V_d}{W_d}$; Ohm's Law ($J = \sigma E$)
- $V_d = \frac{W_d^2}{\tau \cdot [\mu_n + \mu_p] \cdot \sigma}$; Equate above two equations and solve for V_d
- Conclusion: long lifetime τ minimizes V_d.



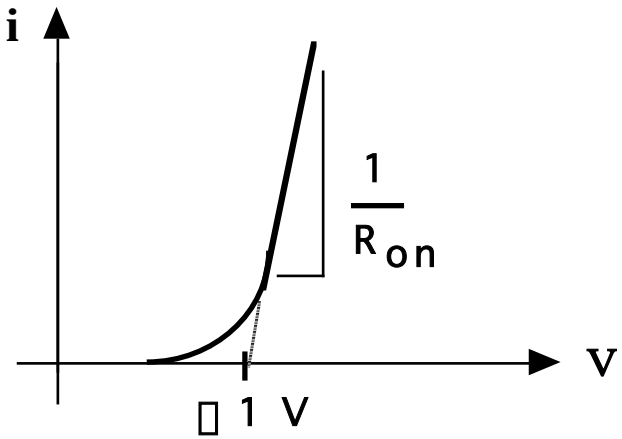
Diode On-State Voltage at Large Forward Currents

- $\mu_n + \mu_p = \dfrac{\mu_o}{1 + \dfrac{n_a}{n_b}}$; $n_b \approx 10^{17}\ cm^{-3}$.
  - Mobility reduction due to increased carrier-carrier scattering at large n_a.

- $I_F = \dfrac{q \cdot n_a \cdot A \cdot V_d}{W_d} \dfrac{\mu_o}{1 + \dfrac{n_a}{n_b}}$; Ohms Law

  with density-dependent mobility.

- Invert Ohm's Law equation to find V_d as function I_F assuming $n_a >> n_b$.

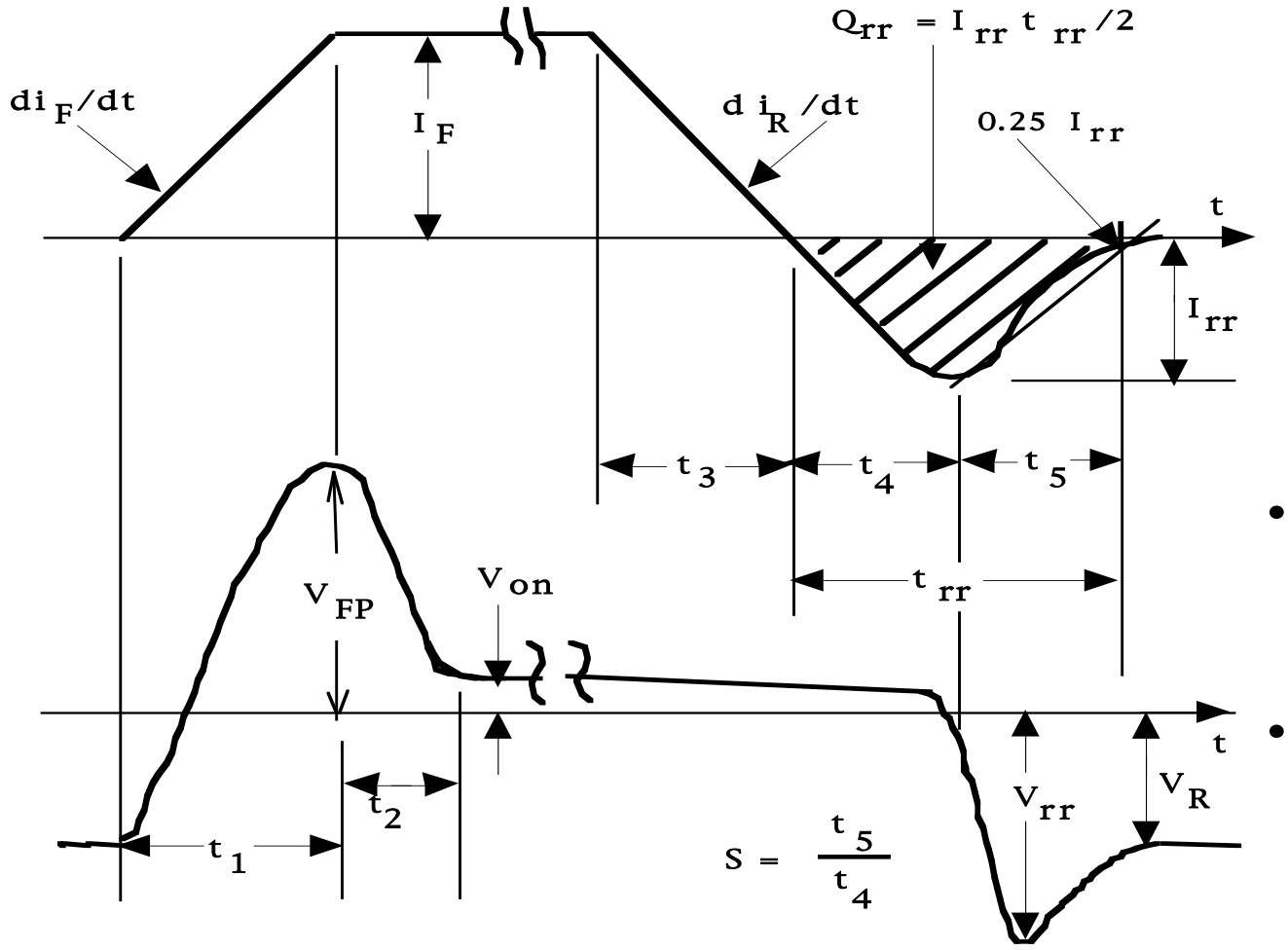


- $V_d = \dfrac{I_f \cdot W_d}{q \cdot \mu_o \cdot n_b \cdot A}$

- $V_d = I_F R_{on}$

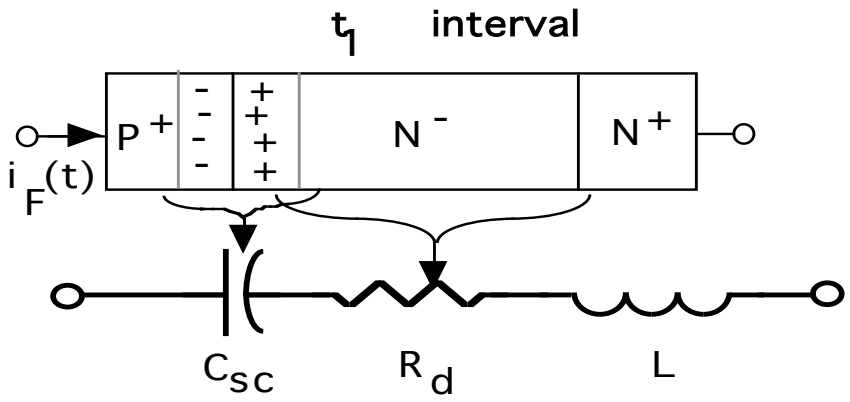
- $V = V_j + V_d$

Diode Switching Waveforms in Power Circuits



- $\frac{di_F}{dt}$ and $\frac{di_R}{dt}$ determined by external circuit.
- Inductances or power semiconductor devices.

Diode Internal Behavior During Turn-on

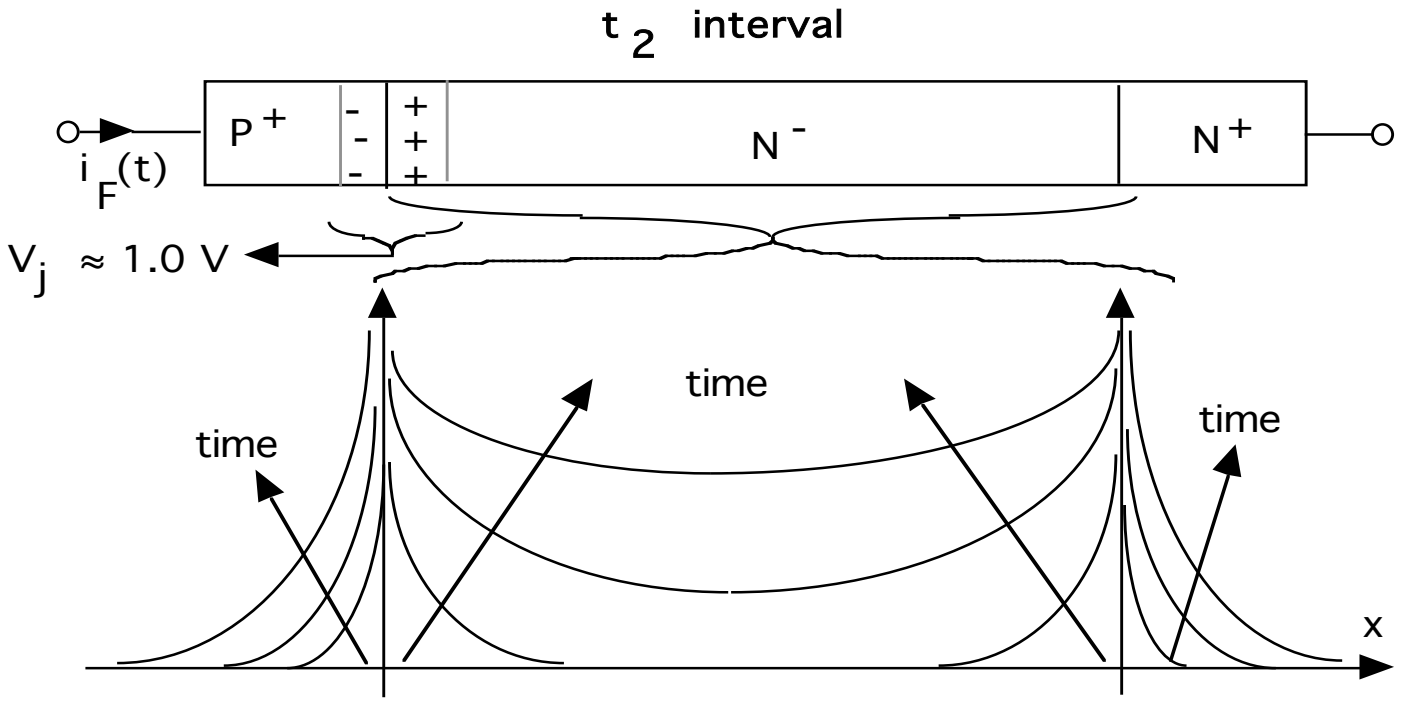


$$C_{sc}(V) = \frac{\varepsilon A}{W(V)}$$

$$R_d = \frac{W_d}{q \mu_n N_d A}$$

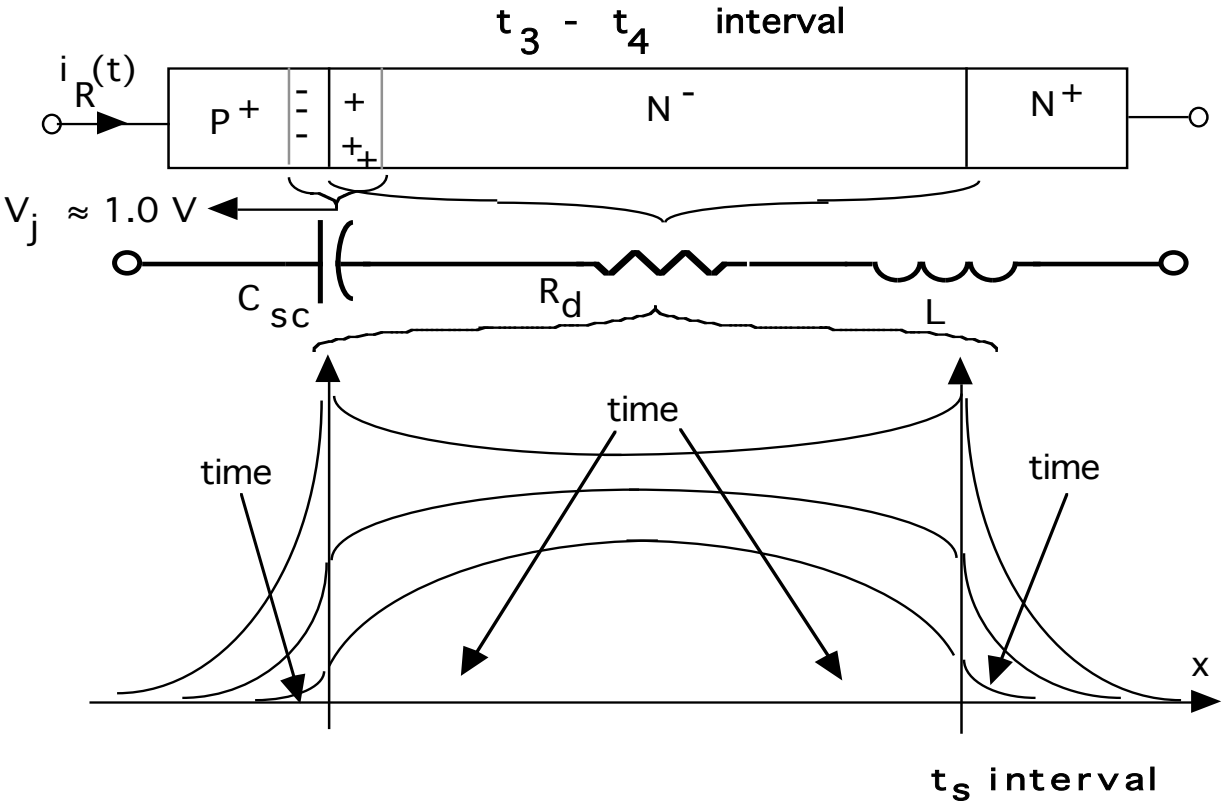
$$V_{FP} \approx I_F R_d + L\frac{di_F}{dt}$$

L = stray or wiring inductance



- Injection of excess carriers into drift region greatly reduces R_d.

Diode Internal Behavior During Turn-off



- R_d increases as excess carriers are removed via recombination and carrier sweep-out (negative current).
- $V_r = I_{rr}R_d + L\frac{di_R}{dt}$

- Insufficient excess carriers remain to support I_{rr}, so P^+N^- junction becomes reverse-biased and current decreases to zero.
- Voltage drops from V_{rr} to V_R as current decreases to zero. Negative current integrated over its time duration removes a total charge Q_{rr}.

Factors Effecting Reverse Recovery Time

- $I_{rr} = \frac{di_R}{dt} t_4 = \frac{di_R}{dt} \frac{t_{rr}}{(S+1)}$; Defined on switching waveform diagram

- $Q_{rr} = \frac{I_{rr} \cdot t_{rr}}{2} = \frac{di_R}{dt} \frac{t_{rr}^2}{2(S+1)}$; Defined on waveform diagram

- Inverting Q_{rr} equation to solve for t_{rr} yields

$$t_{rr} = \sqrt{\frac{2Q_{rr}(S+1)}{\frac{di_R}{dt}}} \text{ and } I_{rr} = \sqrt{\frac{2Q_{rr}\frac{di_R}{dt}}{(S+1)}}$$

- If stored charge removed mostly by sweep-out $Q_{rr} \approx Q_F \approx I_F \cdot$

- Using this in eqs. for I_{rr} and t_{rr} and assuming $S + 1 \approx 1$ gives

$$t_{rr} = \sqrt{\frac{2 \cdot I_F \cdot}{\frac{di_R}{dt}}} \text{ and}$$

$$I_{rr} = \sqrt{2 \cdot I_F \cdot \cdot \frac{di_R}{dt}}$$

Carrier Lifetime-Breakdown Voltage Tradeoffs

- Low on-state losses require

$$L = \sqrt{D\tau} = \sqrt{\frac{kT}{q[\mu_n + \mu_p]}\tau}$$

$$L = W_d \geq W(V) = 10^{-5} BV_{BD}$$

- Solving for the lifetime yields

$$\tau = \frac{W_d^2}{(kT/q)[\mu_n+\mu_p]} = 4x10^{-12}\ (BV_{BD})^2$$

- Substituting for τ in I_{rr} and t_{rr} equations gives
  - $t_{rr} = 2.8x10^{-6}\ BV_{BD} \sqrt{\frac{I_F}{(di_R/dt)}}$
  - $I_{rr} = 2.8x10^{-6}\ BV_{BD} \sqrt{I_F \frac{di_R}{dt}}$

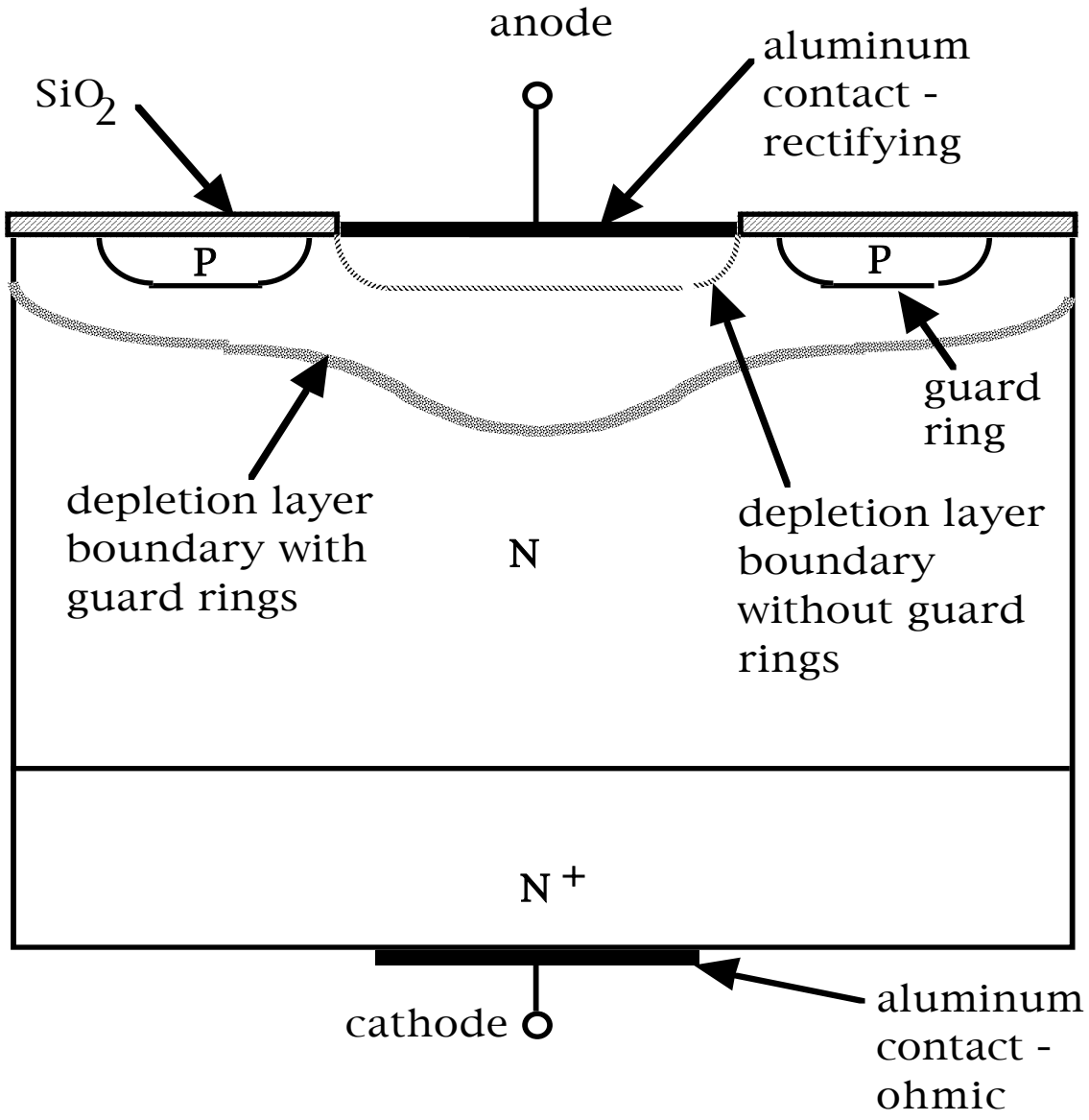
Conclusions

1. Higher breakdown voltages require larger lifetimes if low on-state losses are to be maintained.
2. High breakdown voltage devices slower than low breakdown voltage devices.
3. Turn-off times shortened by large $\frac{di_R}{dt}$ but I_{rr} is increased.

Schottky Diodes

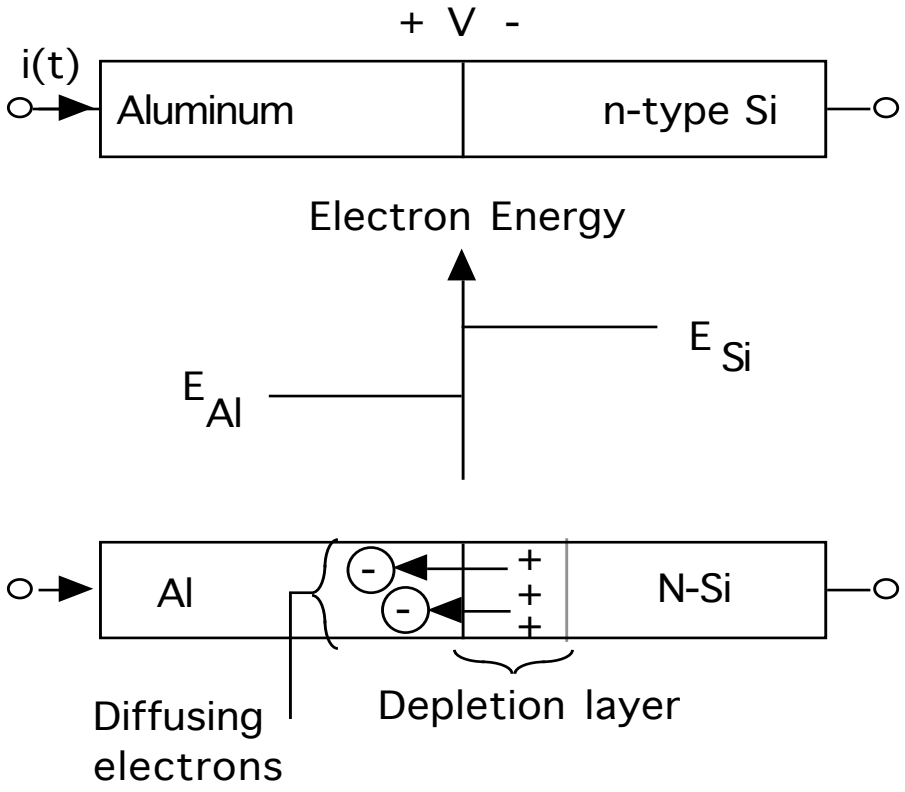
Characteristics

- V(on) = 0.3 - 0.5 volts.
- Breakdown voltages ≤ 100-200 volts.
- Majority carrier device - no stored charge.
- Fast switching because of lack of stored charge.



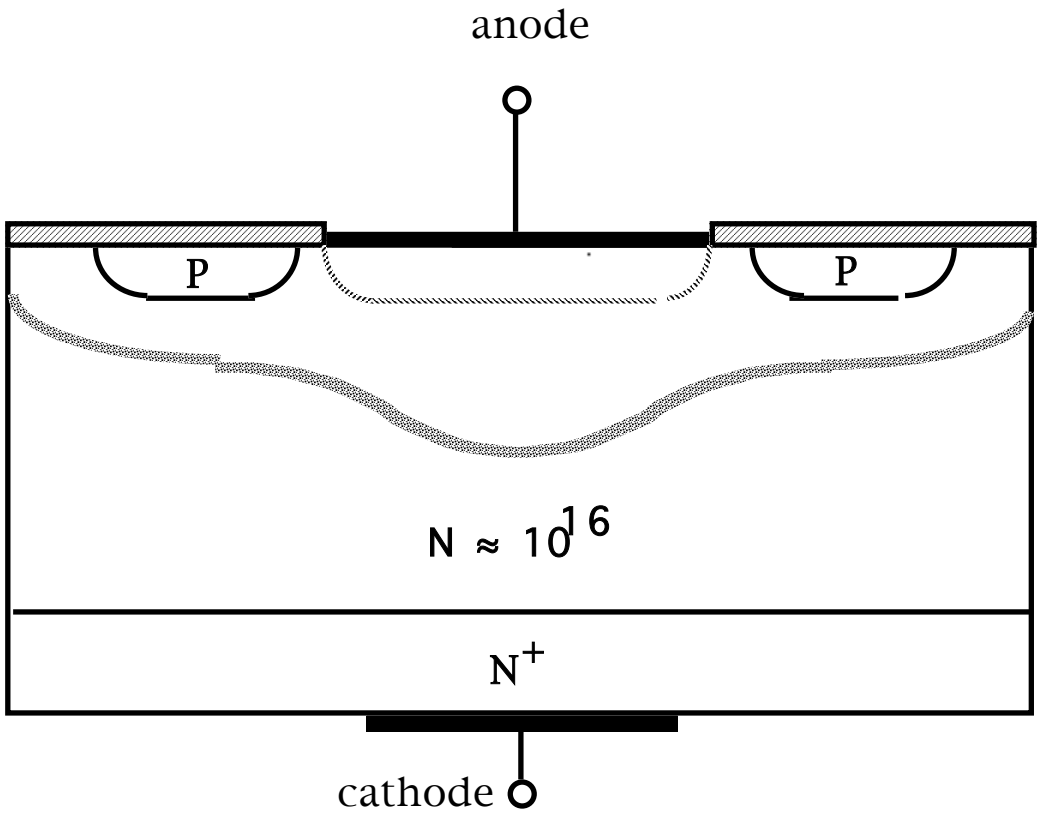
Physics of Schottky Diode Operation

- Electrons diffuse from Si to Al because electrons have larger average energy in silicon compared to aluminum.
- Depletion layer and thus potential barrier set up. Gives rise to rectifying contact.
- No hole injection into silicon. No source of holes in aluminum. Thus diode is a majority carrier device.
- Reverse saturation current much larger than in pn junction diode. This leads to smaller V(on) (0.3 - 0.5 volts)



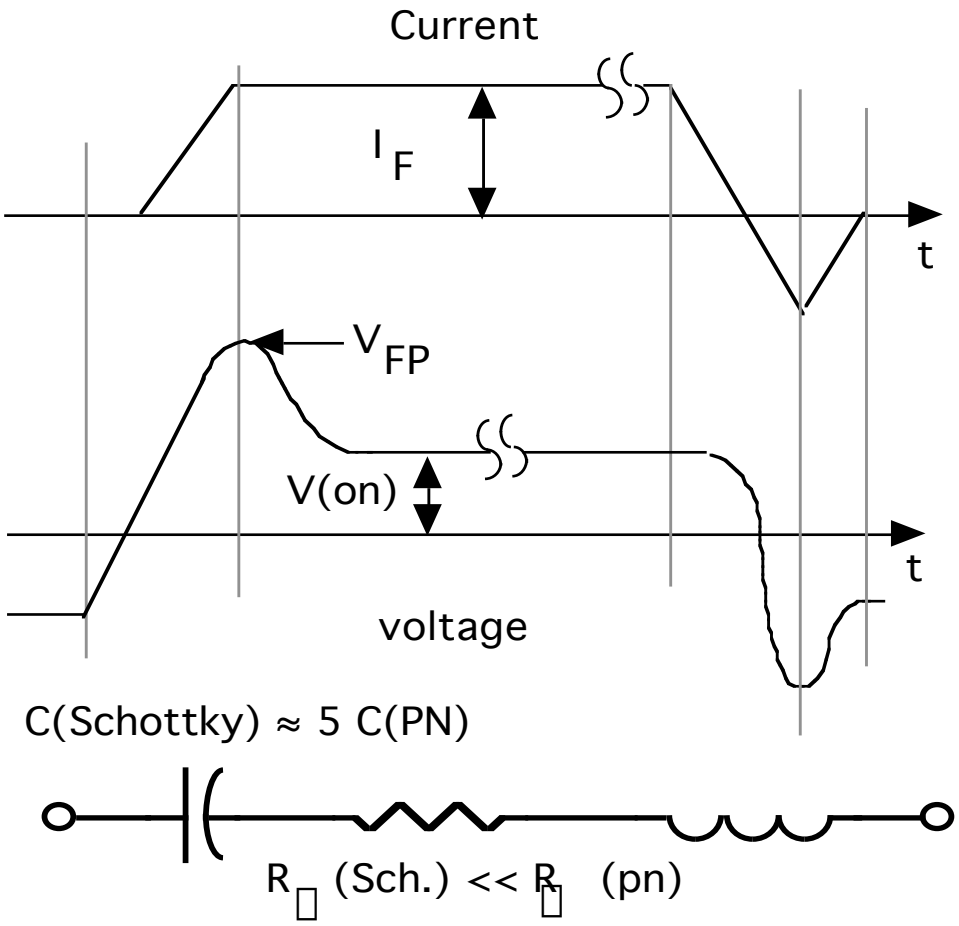
Schottky Diode Breakdown Voltage

- Breakdown voltage limited to 100-200 volts.
- Narrow depletion region widths because of heavier drift region doping needed for low on-state losses.
- Small radius of curvature of depletion region where metallization ends on surface of silicon. Guard rings help to mitigate this problem.
- Depletion layer forms right at silicon surface where maximum field needed for breakdown is less because of imperfections, contaminants.



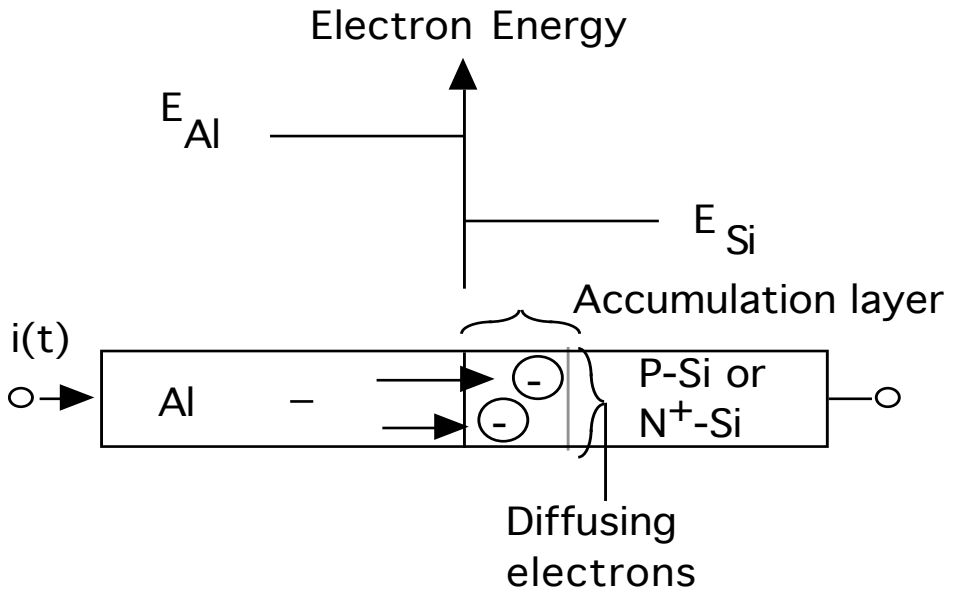
Schottky Diode Switching Waveforms

- Schottky diodes switch much faster than pn junction diodes. No minority carrier storage.
- Foreward voltage overshoot V_{FP} much smaller in Schottky diodes. Drift region ohmic resistance $R_{\square}$.
- Reverse recovery time t_{rr} much smaller in Schottky diodes. No minority carrier storage.
- Reverse recovery current I_{rr} comparable to pn junction diodes. space charge capacitance in Schottky diode larger than in pn junction diode becasue of narrower depletion layer widths resulting from heavier dopings.



Ohmic Contacts

- Electrons diffuse from Al into p-type Si becasue electrons in Al have higher average energy.
- Electrons in p-type Si form an accumulation layer of greatly enhanced conductivity.
- Contact potential and rectifying junction completely masked by enhanced conductivity. So-called ohmic contact.
- In N^+ Si depletion layer is very narrow and electric fields approach impact ionization values. Small voltages move electrons across barrier easily becasue quantum mechanical tunneling occurs.



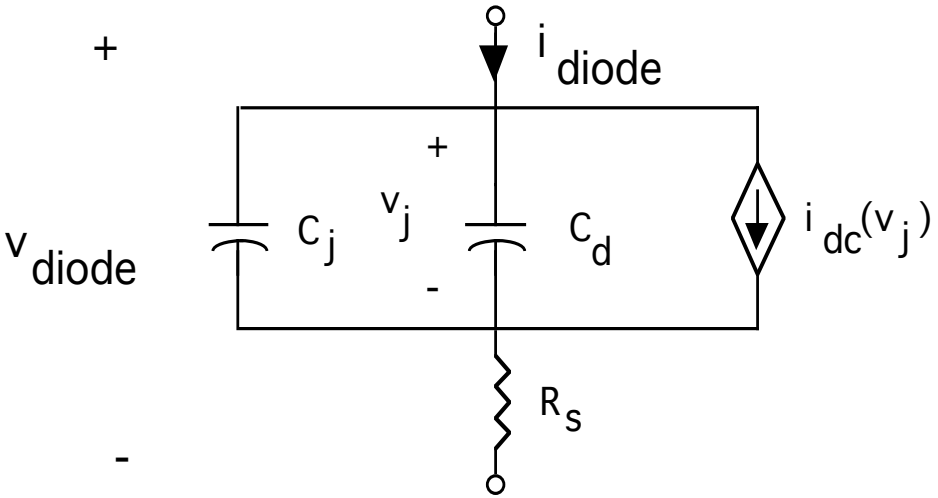
PN Vs Schottkys at Large BV_{BD}

- Minority carrier drift region relationships
  - $I_F \approx \frac{q[\mu_n + \mu_p] n_a A V_d}{W_d}$
- Maximum practical value of $n_a = 10^{17}$ cm^{-3} and corresponding to $\mu_n + \mu_p = 900\ cm^2/(V\text{-}sec)$
- Desired breakdown voltage requires $W_d \geq 10^{-5}\ BV_{BD}$

  $\frac{I_F}{A} = 1.4x10^6 \frac{Vd}{BV_{BD}}$
- Majority carrier drift region relationships
  - $I_F \approx \frac{q[\mu_n + \mu_p] N_d A V_d}{W_d}$
- Desired breakdown voltage requires $N_d = \frac{1.3x10^{17}}{BV_{BD}}$ and $W_d \geq 10^{-5}\ BV_{BD}$
- Large BV_{BD} (1000 V) requires $N_d = 10^{14}\ cm^{-3}$ where $\mu_n + \mu_p = 1500\ cm^2/(V\text{-}sec)$
- $\frac{I_F}{A} \approx 3.1x10^6 \frac{V_d}{[BV_{BD}]^2}$
- Conclusion: Minority carrier devices have lower on-state losses at large BV_{BD}.

PSPICE Built-in Diode Model

- Circuit diagram

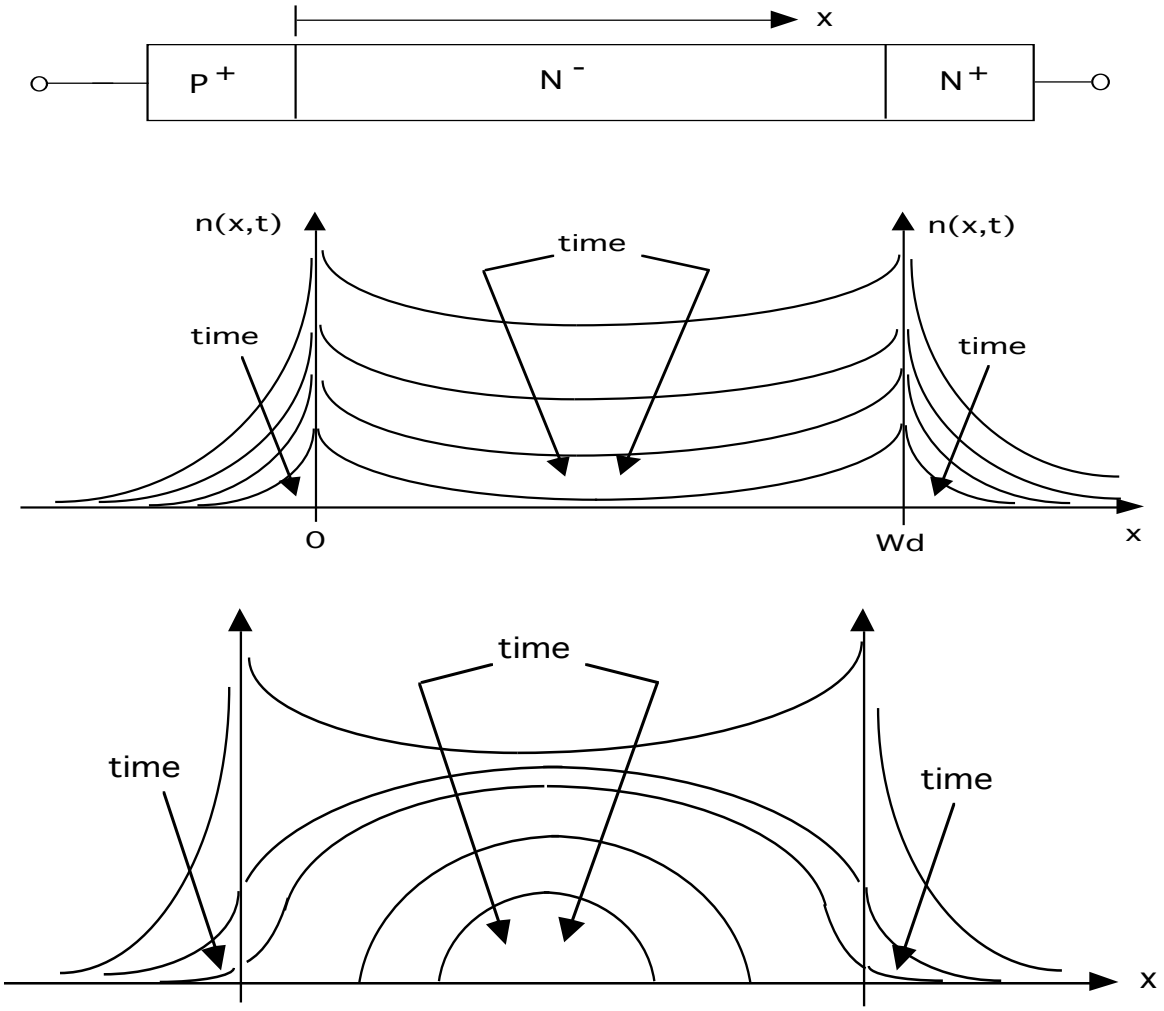


$$v_{diode} = v_j + R_s\, i_{diode}$$

- Components

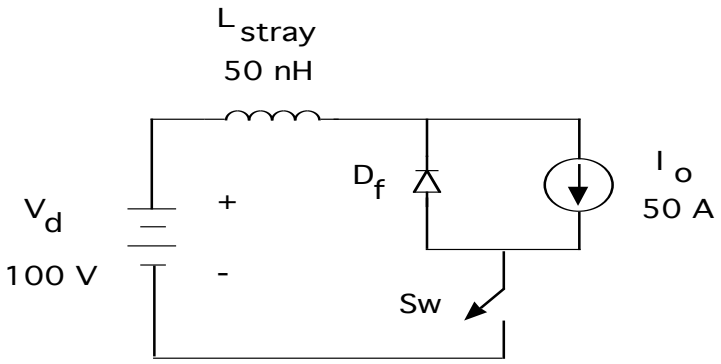
- C_j - nonlinear space-charge capacitance
- C_d - diffusion capacitance. Caused by excess carriers. Based on quasi-static description of stored charge in drift region of diode.
- Current source $i_{dc}(v_j)$ models the exponential I-V characteristic.
- R_s accounts for parasitic ohmic losses at high currents.

Stored Charge in Diode Drift Region - Actual Versus Quasi-static Approximation

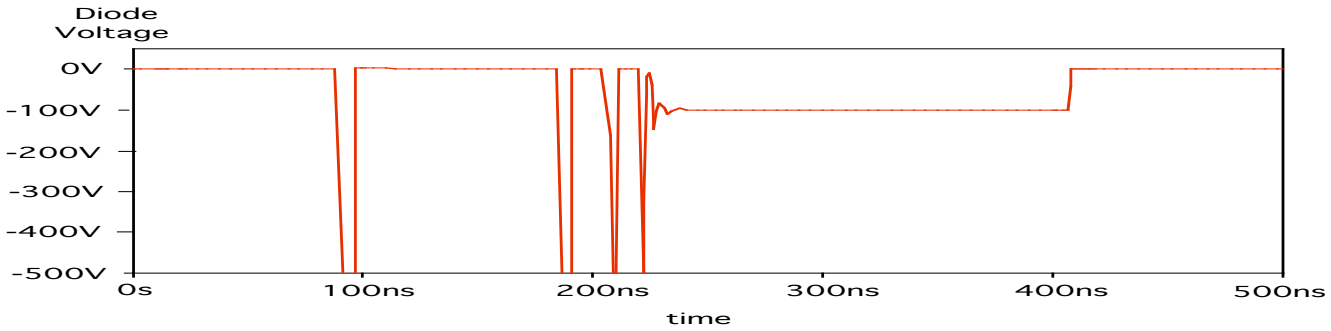


- One dimensional diagram of a power diode.
- Quasistatic view of decay of excess carrier distribution during diode turn-off. $n(x,t) = n(x=0,t)\, f(x)$
- Redistribution of excess carriers via diffusion ignored. Equ;ivalent to carriers moving with inifinte velocity.
- Actual behavior of stored charge distribution during turn-off.

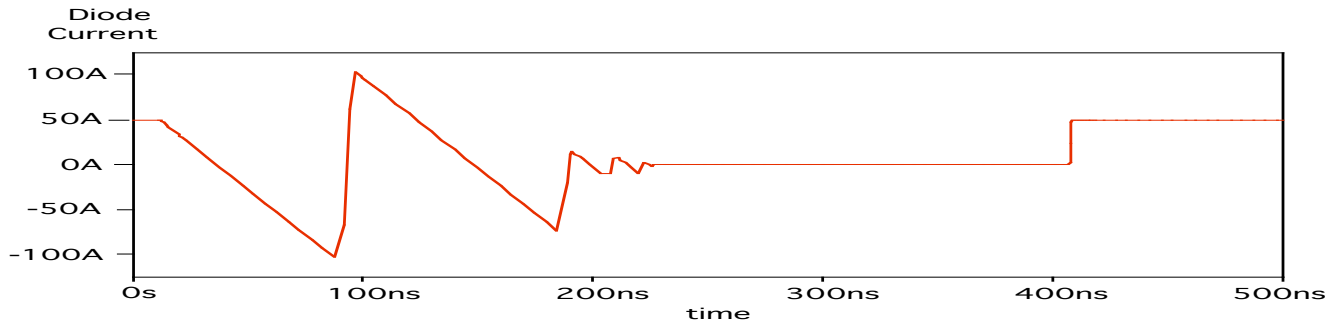
Example of Faulty Simulation Using Built-in Pspice Diode Model



- Test circuit example - step-down converter.
- PSPICE diode model parameters - (TT=100ns Cjo=100pF Rs=.004 Is=20fA)



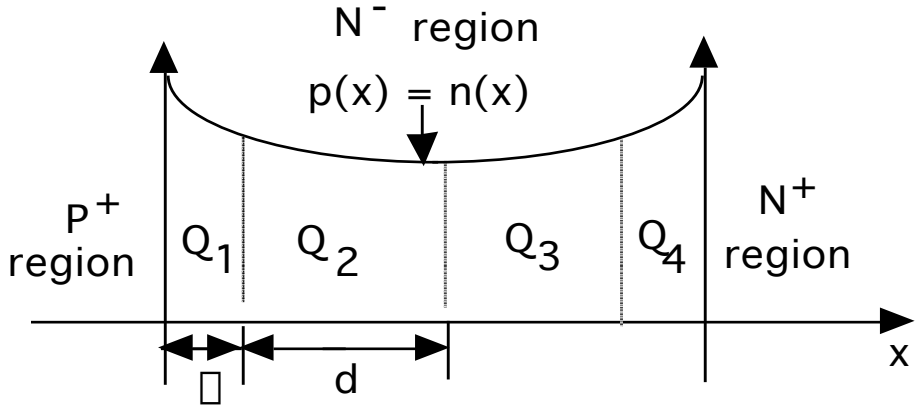
- Diode voltage transient

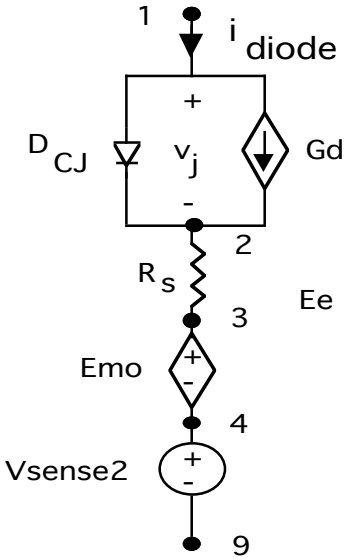


- Diode current transient.

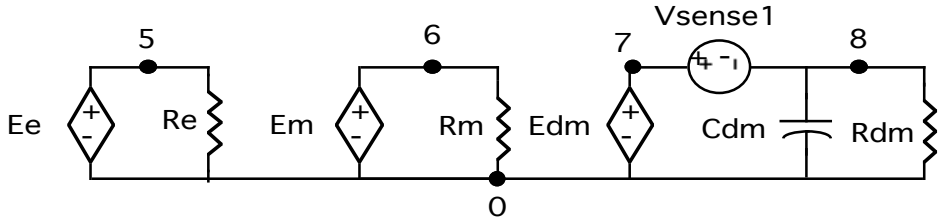
Improved (lumped-charge) Diode Model

- More accurately model distributed nature of excess carrier distribution by dividing it into several regions, each described by a quasi-static function. Termed the lumped-charge approach.





- Circuit diagram of improved diode model. Circuit written in terms of physical equations of the lumped-charge model.



- Detailed equations of model given in subcircuit listing.
- Many other even better (but more complicated models available in technical literature..

Details of Lumped-Charge Model

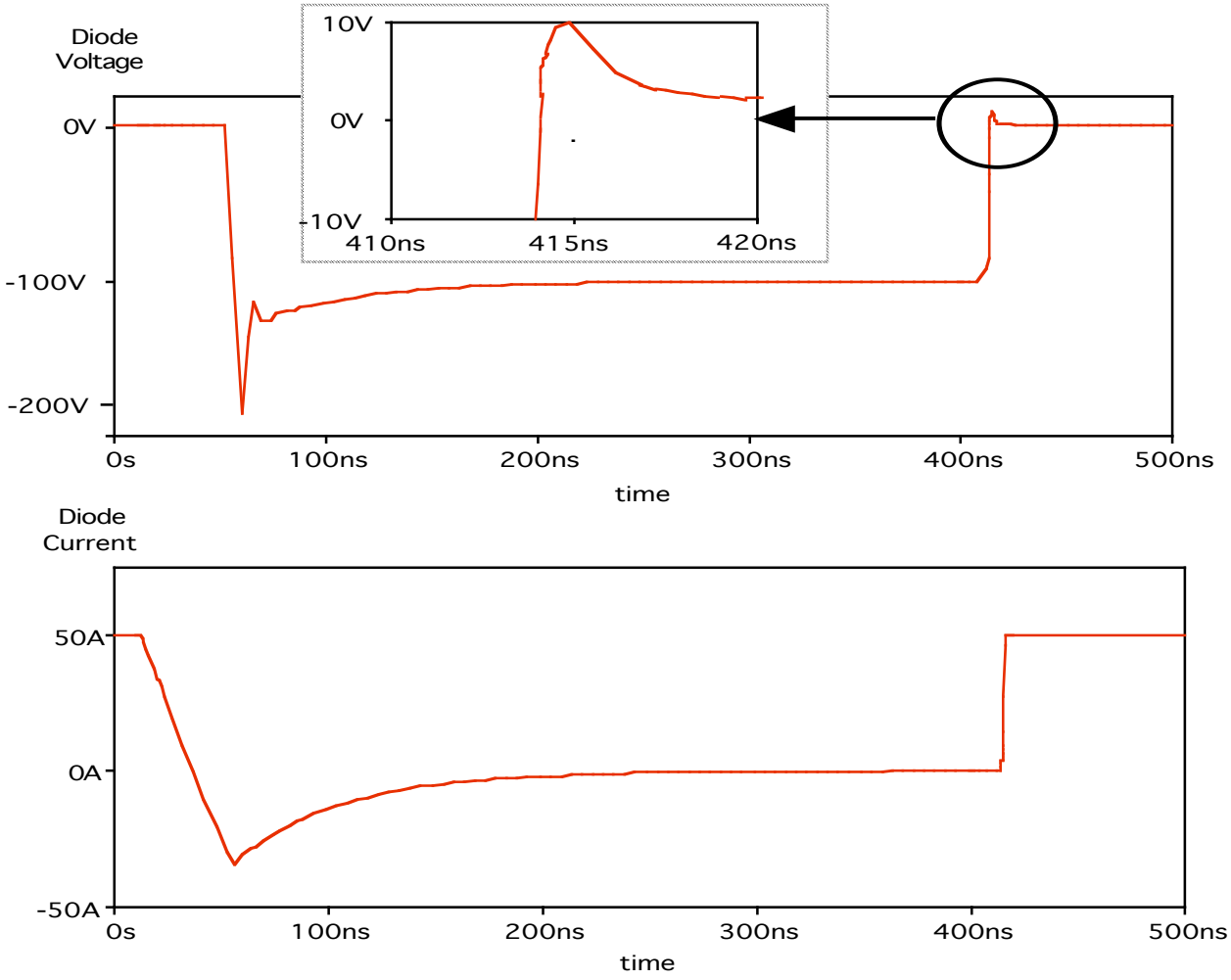
Subcircuit Listing

```
.Subckt DMODIFY 1 9 Params: Is1=1e-6, Ise=1e-40, Tau=100ns,
+Tm=100ns,Rmo=Rs=.001, Vta=.0259, CAP=100p, Gde=.5,
+ Fbcoeff=.5, Phi=1, Irbk=1e20,Vrbk=1e20
*Node 1= anodeand  Node 9 = cathode
Dcj 1 2 Dcap ; Included for space charge capacitance and reverse
*breakdown.
.model Dcap D (Is=1e-25 Rs=0 TT=0 Cjo={CAP} M={Gde}
+FC={Fbcoeff} Vj={Phi} +IBV={Irbk} BV=Vrbk})
Gd 1 2 Value={(v(5)-v(6))/Tm +Ise*(exp(v(1,2)/Vta)-1)}
*Following components model forward and reverse recovery.
Ee 5 0 VALUE = {Is1*Tau*(exp(V(1,2)/(2*Vta))-1)}; Ee=Qe
Re 5 0 1e6
Em 6 0 VALUE = {(V(5)/Tm-i(Vsense1))*Tm*Tau/(Tm+Tau)}
*Em=Qm
Rm 6 0 1e6
Edm 7 0 VALUE = {v(6)};Edm=Qm
Vsense1 7 8 dc 0 ; i(vsense1)=dQm/dt
Cdm 8 0 1
Rdm 8 0 1e9
Rs 2 3 4e-3
Emo 3 4 VALUE={2*Vta*Rmo*Tm*i(Vsense2)
+/(v(6)*Rmo+Vta*Tm)}; Vm
Vsense2 4 9 dc 0
.ends
```

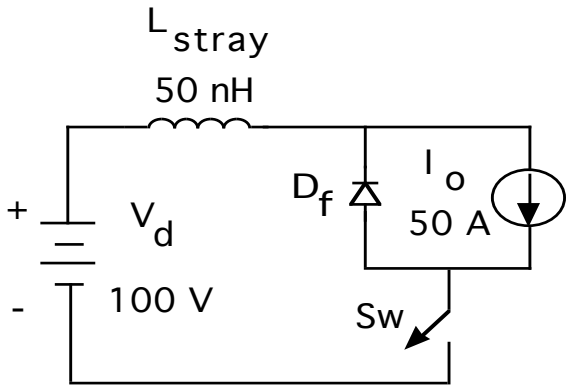
- Symbolize subcircuit listing into SCHEMATICS using SYMBOL WIZARD
- Pass numerical values of parameters Tau, Tm, Rmo,Rs, etc. by entering values in PART ATTRIBUTE window (called up within SCHEMATICS).
- See reference shown below for more details and parameter extraction procedures.
- Peter O. Lauritzen and Cliff L. Ma, "A Simple Diode Model with Forward and Reverse Recovery", IEEE Trans. on Power Electronics, Vol. 8, No. 4, pp. 342-346, (Oct., 1993)

Simulation Results Using Lumped-Charge Diode Model

Diode voltage and current waveforms



Simulation Circuit



- Note soft reverse recovery and forward voltage overshoot. Qualitatively matches experimental measurements.