Lecture Notes

Insulated Gate Bipolar Transistors (IGBTs)

Outline

- Construction and I-V characteristics
- Physical operation
- Switching characteristics
- Limitations and safe operating area
- PSPICE simulation models

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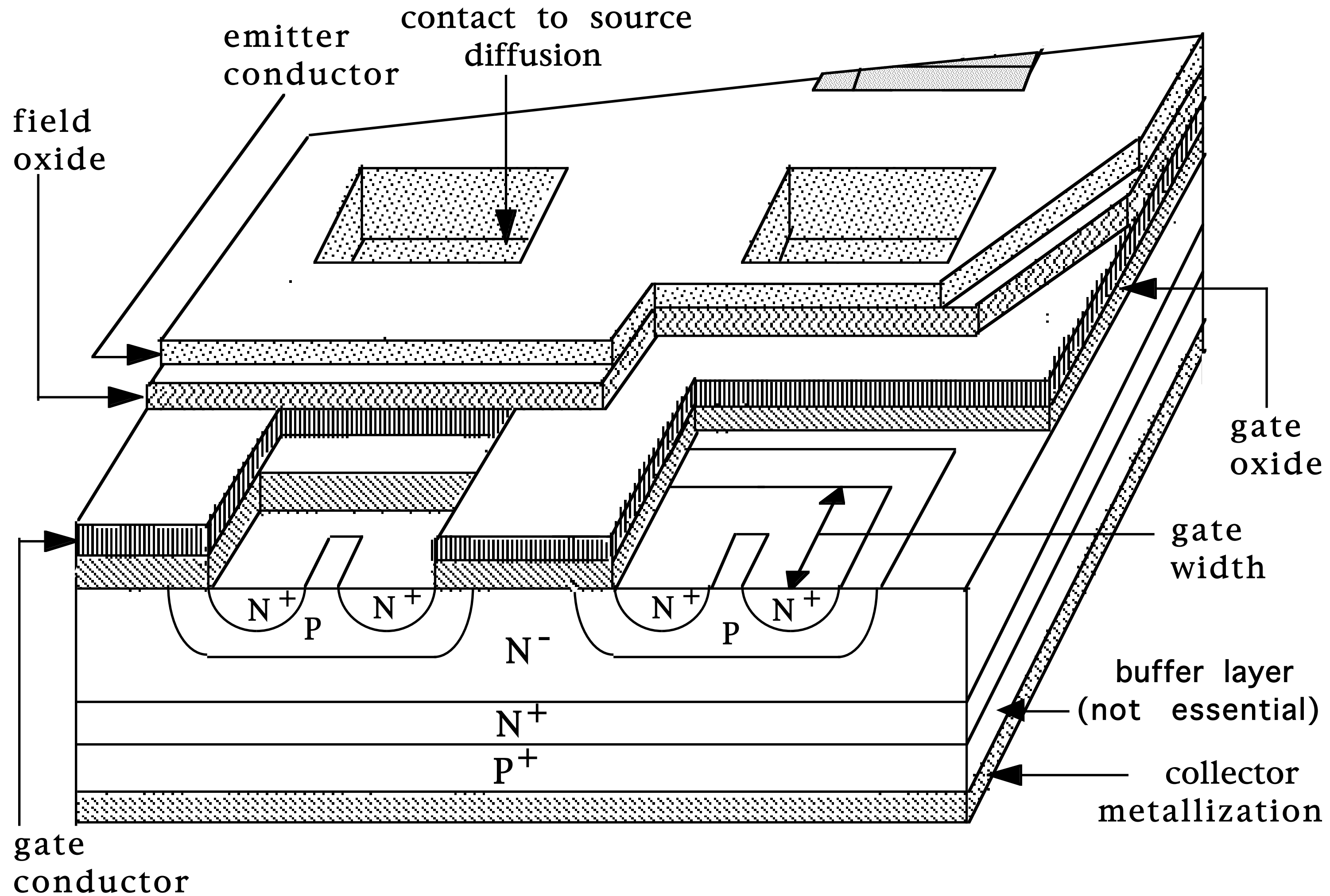
Multi-cell Structure of IGBT

- IGBT = insulated gate bipolar transistor.



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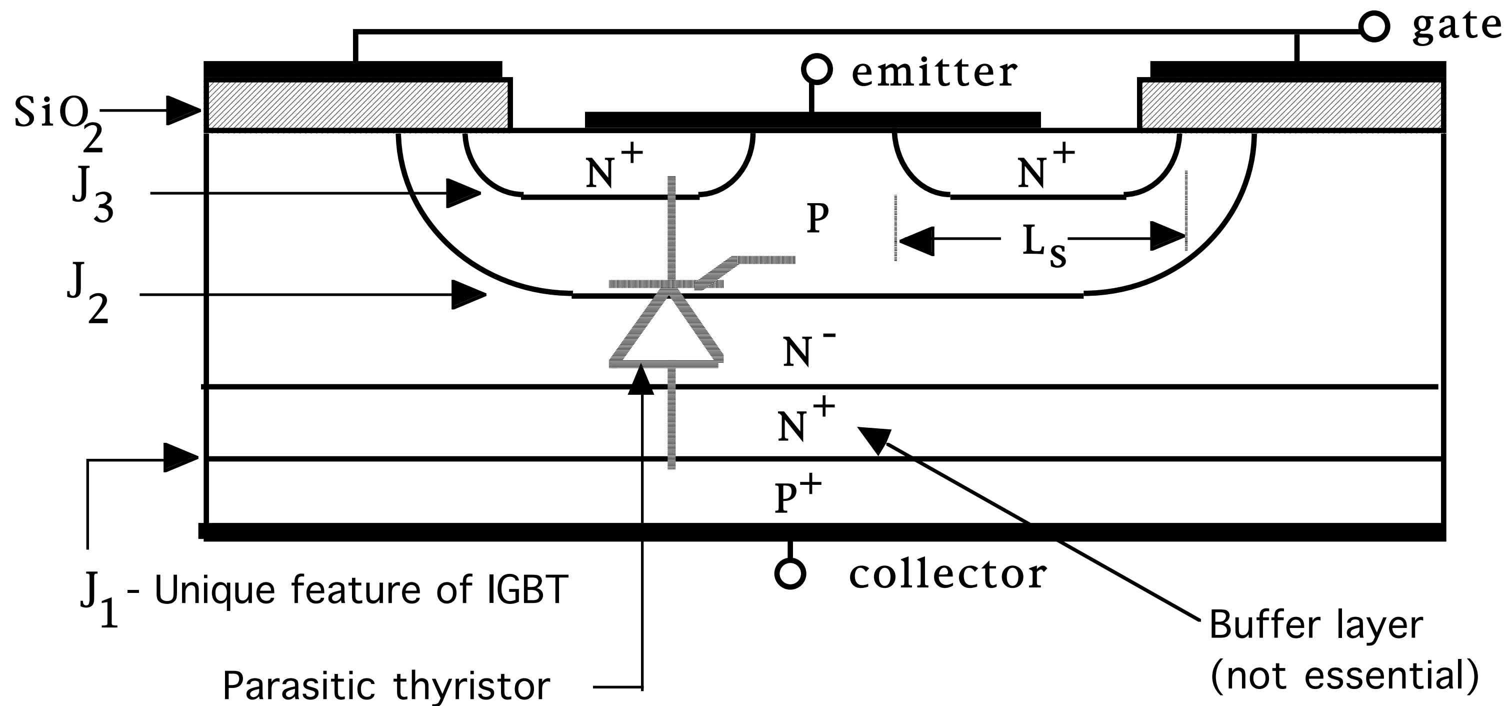
Cross-section of IGBT Cell



- Cell structure similar to power MOSFET (VDMOS) cell.
- P-region at collector end unique feature of IGBT compared to MOSFET.
- Punch-through (PT) IGBT - N^+ buffer layer present.
- Non-punch-through (NPT) IGBT - N^+ buffer layer absent.

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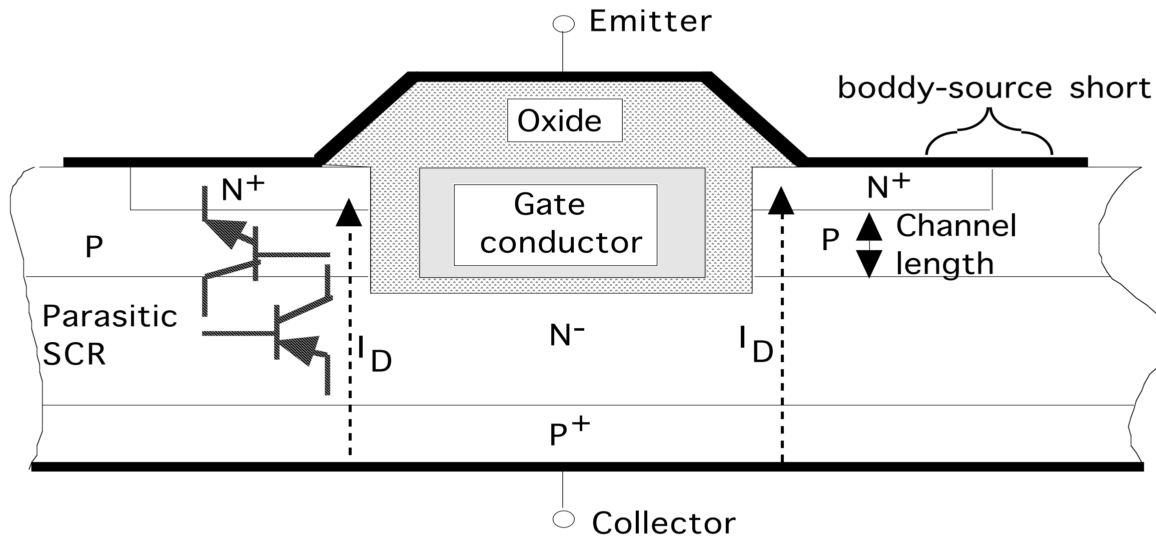
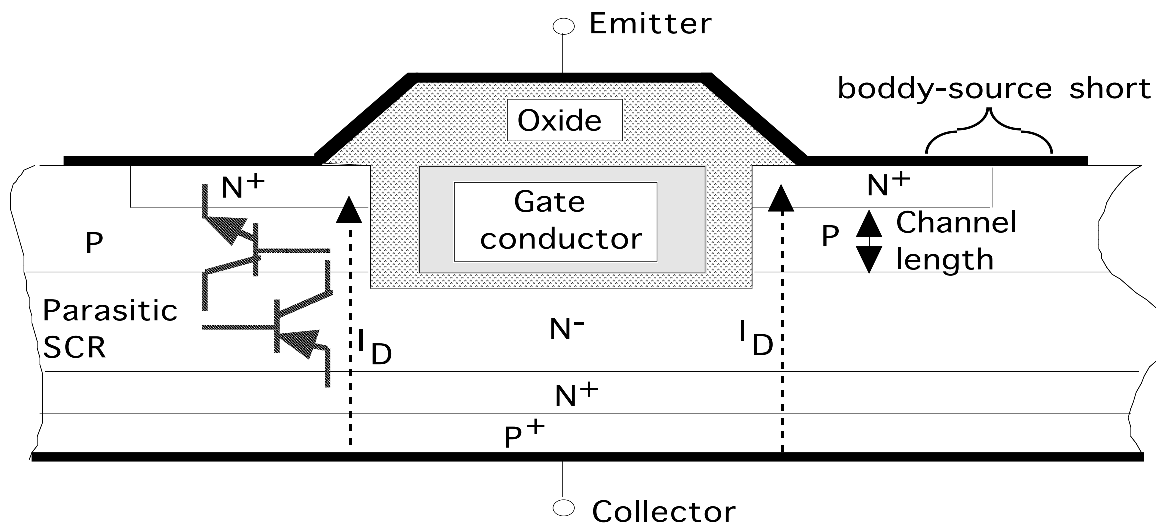
Cross-section of Trench-Gate IGBT Unit Cell



• Non-punch-thru IGBT



• Punch-thru IGBT

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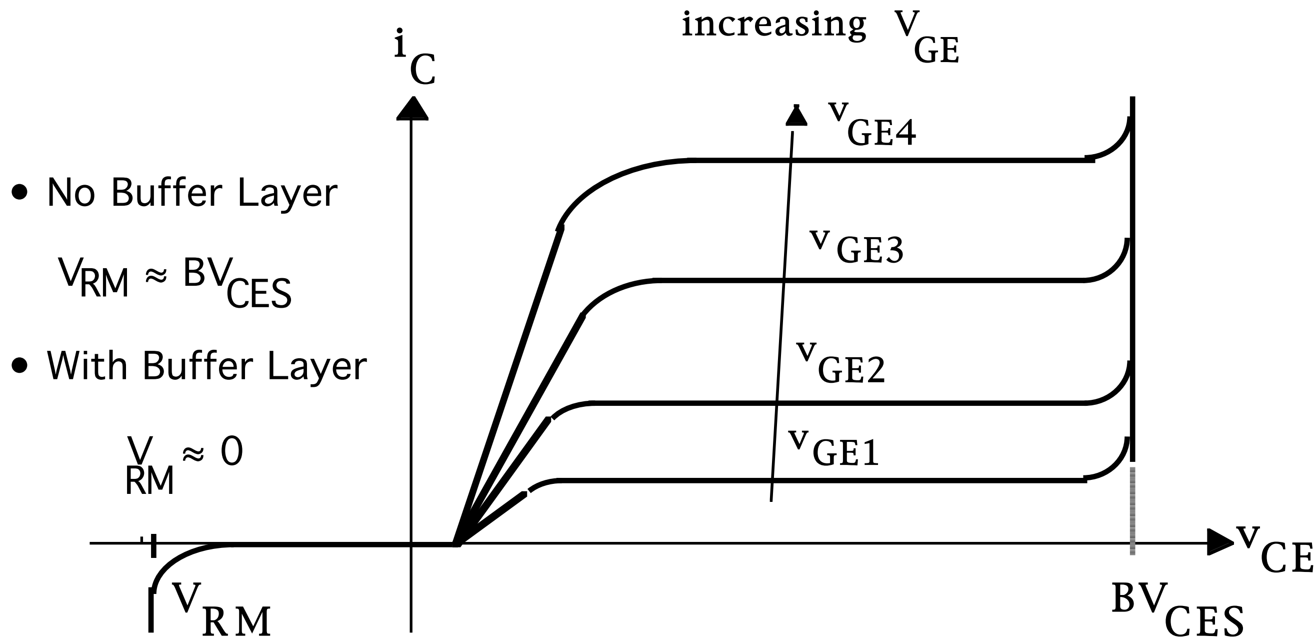
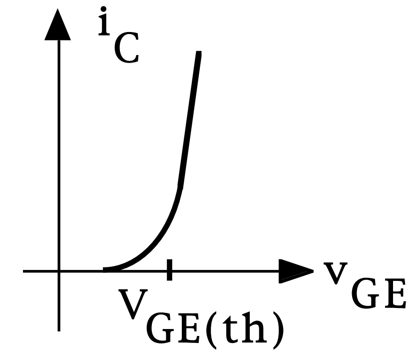
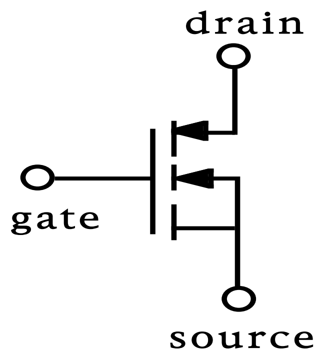
IGBT I-V Characteristics and Circuit Symbols

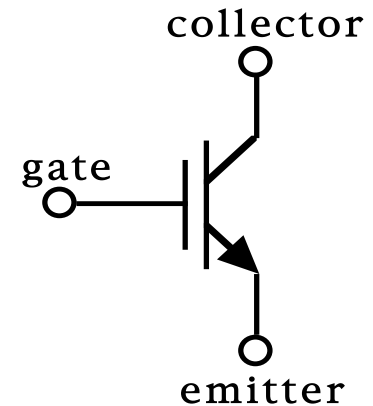




• Transfer curve



• N-channel IGBT circuit symbols



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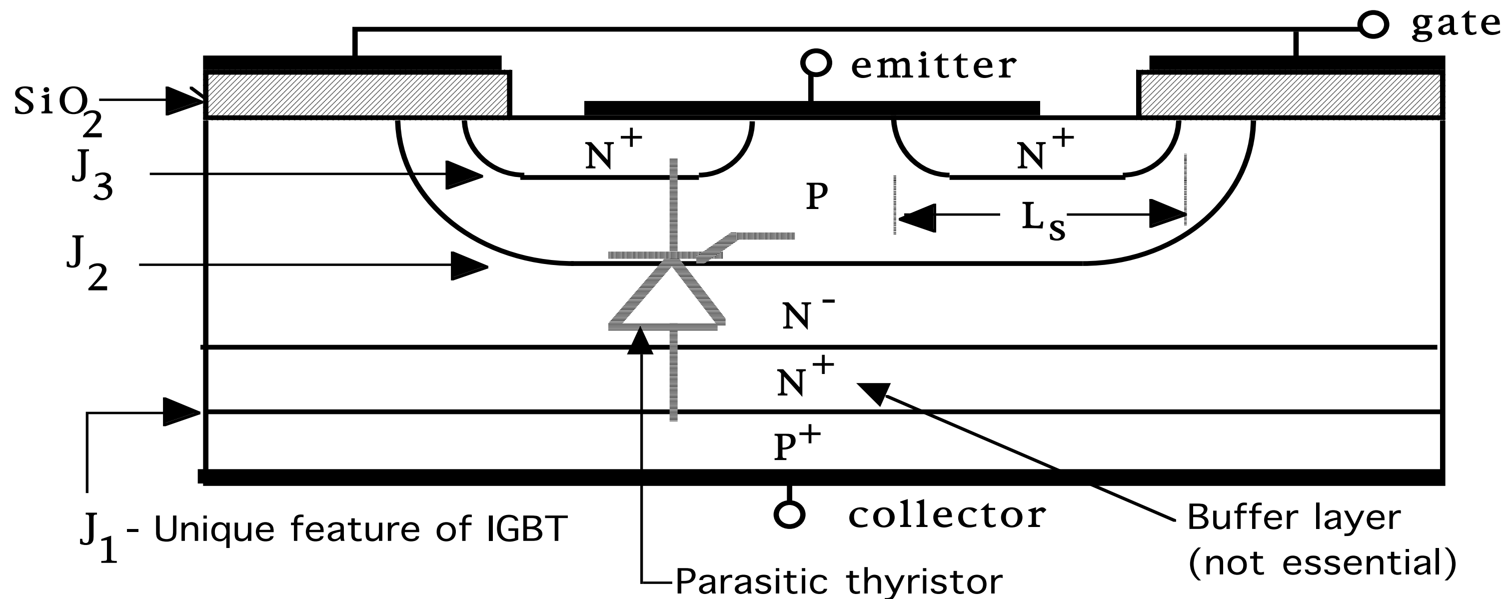
Blocking (Off) State Operation of IGBT



- Blocking state operation - $V_{GE} < V_{GE(th)}$
- Junction J_2 is blocking junction - n^+ drift region holds depletion layer of blocking junction.
- Without N^+ buffer layer, IGBT has large reverse blocking capability - so-called symmetric IGBT
- With N^+ buffer layer, junction J_1 has small breakdownvoltage and thus IGBT has little reverse blocking capability - anti-symmetric IGBT
- Buffer layer speeds up device turn-off

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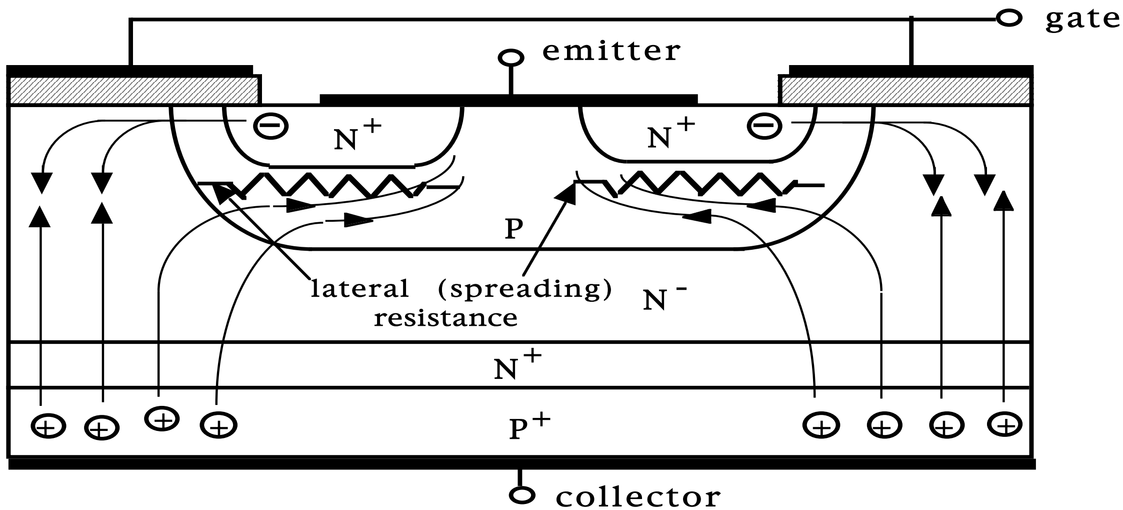
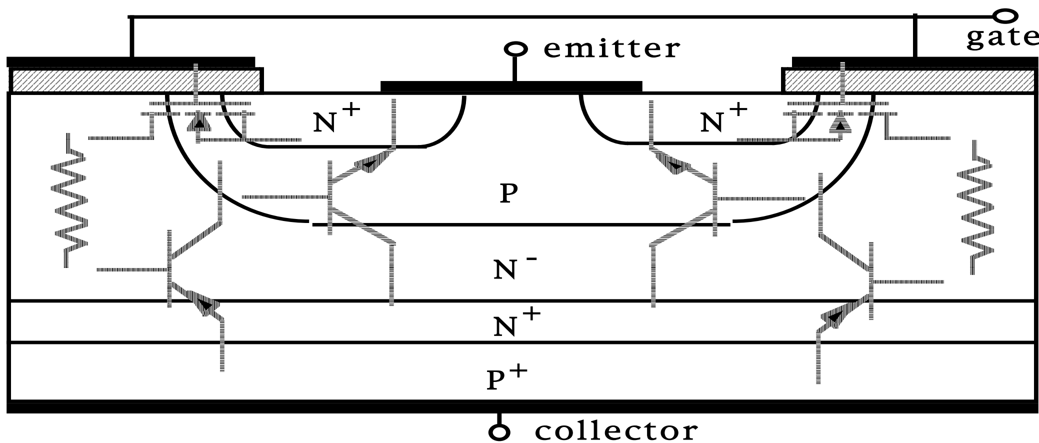
IGBT On-state Operation





- MOSFET section designed to carry most of the IGBT collector current
- On-state $V_{CE(on)} = V_{J1} + V_{drift} + I_C R_{channel}$
- Hole injection into drift region from J_1 minimizes V_{drift}.

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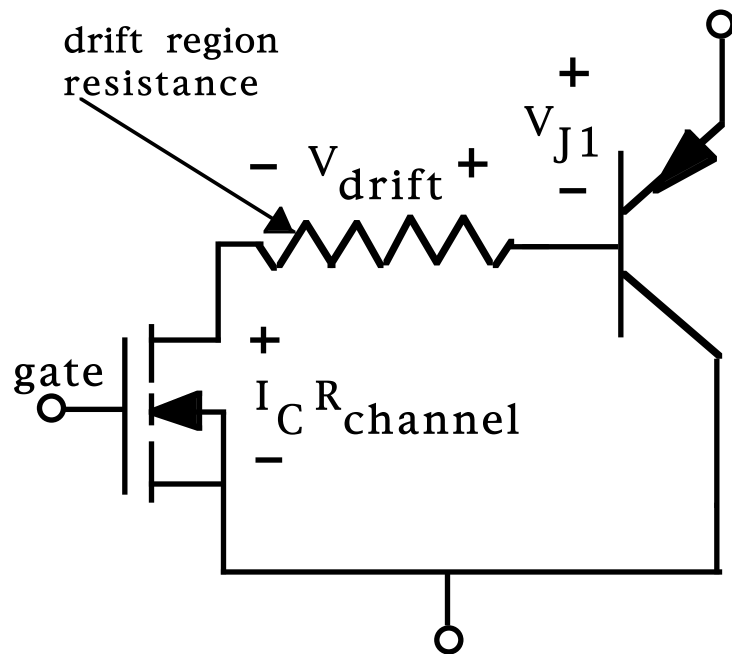
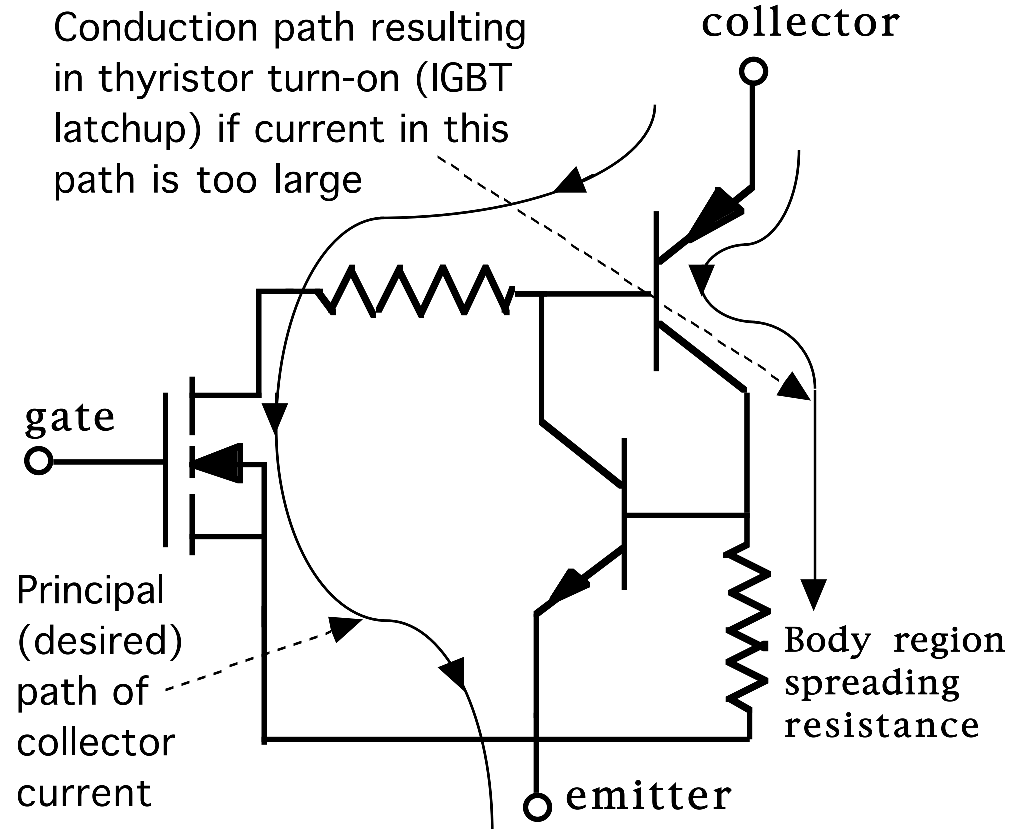
Approximate Equivalent Circuits for IGBTs





- Approximate equivalent circuit for IGBT valid for normal operating conditions.

- $V_{CE(on)} = V_{J1} + V_{drift} + I_C R_{channel}$

- IGBT equivalent circuit showing transistors comprising the parasitic thyristor.

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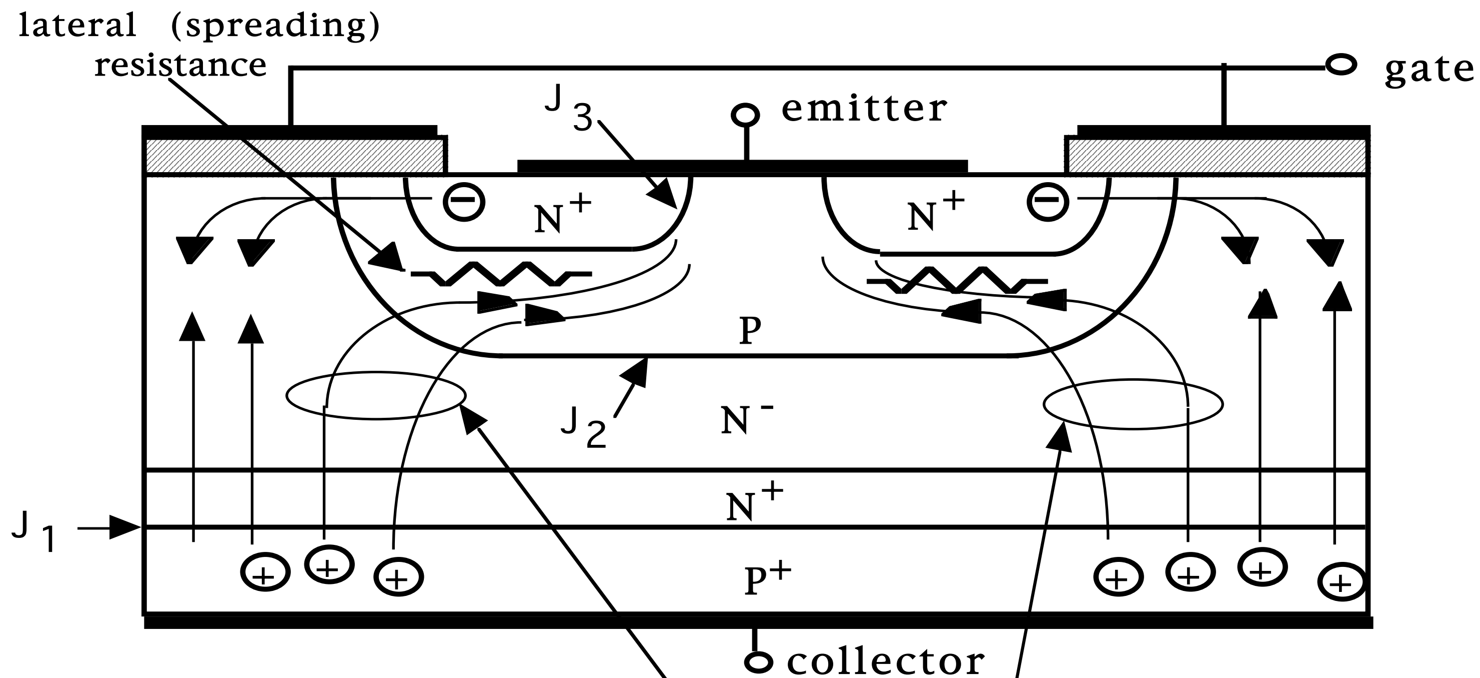
Static Latchup of IGBTs



- Lateral voltage drops, if too large, will forward bias junction J3.
- Parasitic npn BJT will be turned on, thus completing turn-on of parasitic thyristor.
- Large power dissipation in latchup will destroy IGBT unless terminated quickly. External circuit must terminate latchup - no gate control in latchup.

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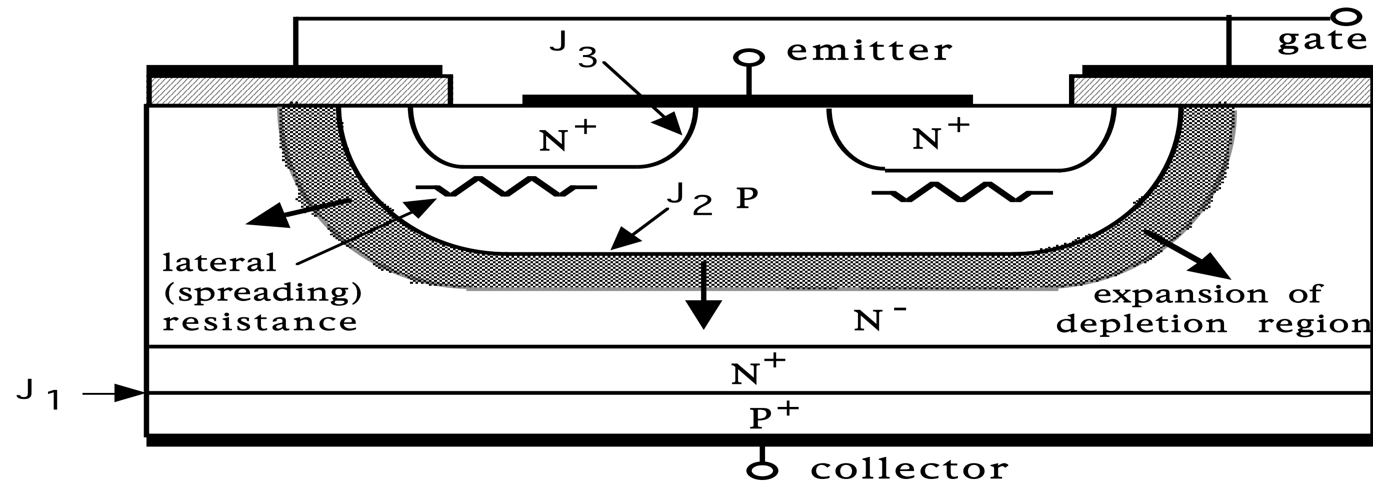
Dynamic Latchup Mechanism in IGBTs



- MOSFET section turns off rapidly and depletion layer of junction J2 expands rapidly into N^- layer, the base region of the pnp BJT.
- Expansion of depletion layer reduces base width of pnp BJT and its a increases.
- More injected holes survive traversal of drift region and become "collected" at junction J2.
- Increased pnp BJT collector current increases lateral voltage drop in p-base of npn BJT and latchup soon occurs.
- Manufacturers usually specify maximum allowable drain current on basis of dynamic latchup.

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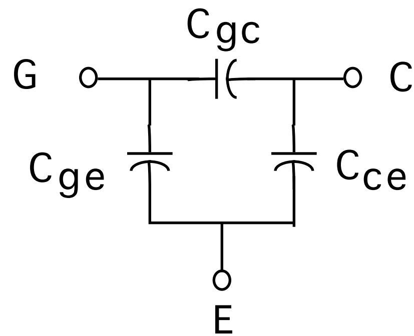
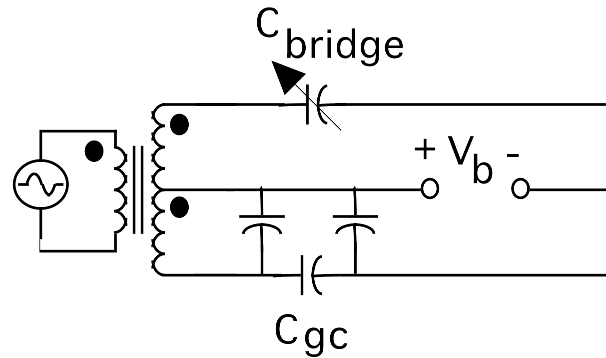
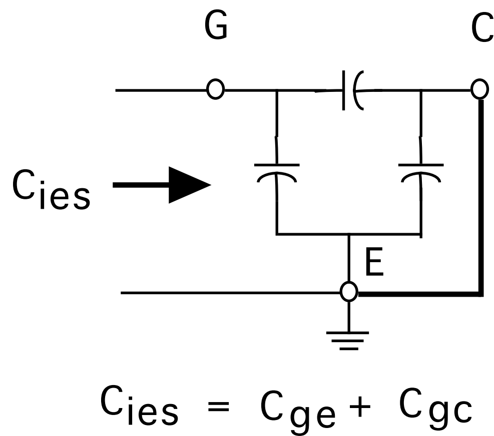
Internal Capacitances Vs Spec Sheet Capacitances

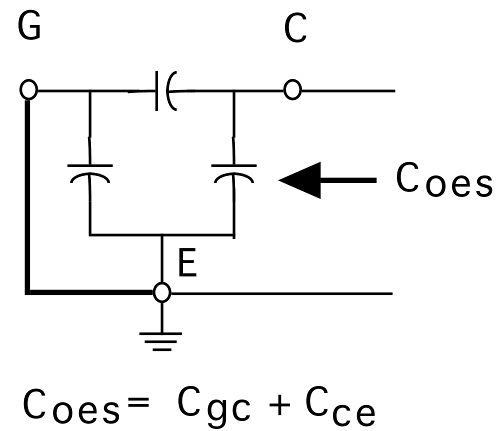




Bridge balanced (Vb=0) $C_{bridge} = C_{gc} = C_{res}$



$C_{ies} = C_{ge} + C_{gc}$



$C_{oes} = C_{gc} + C_{ce}$

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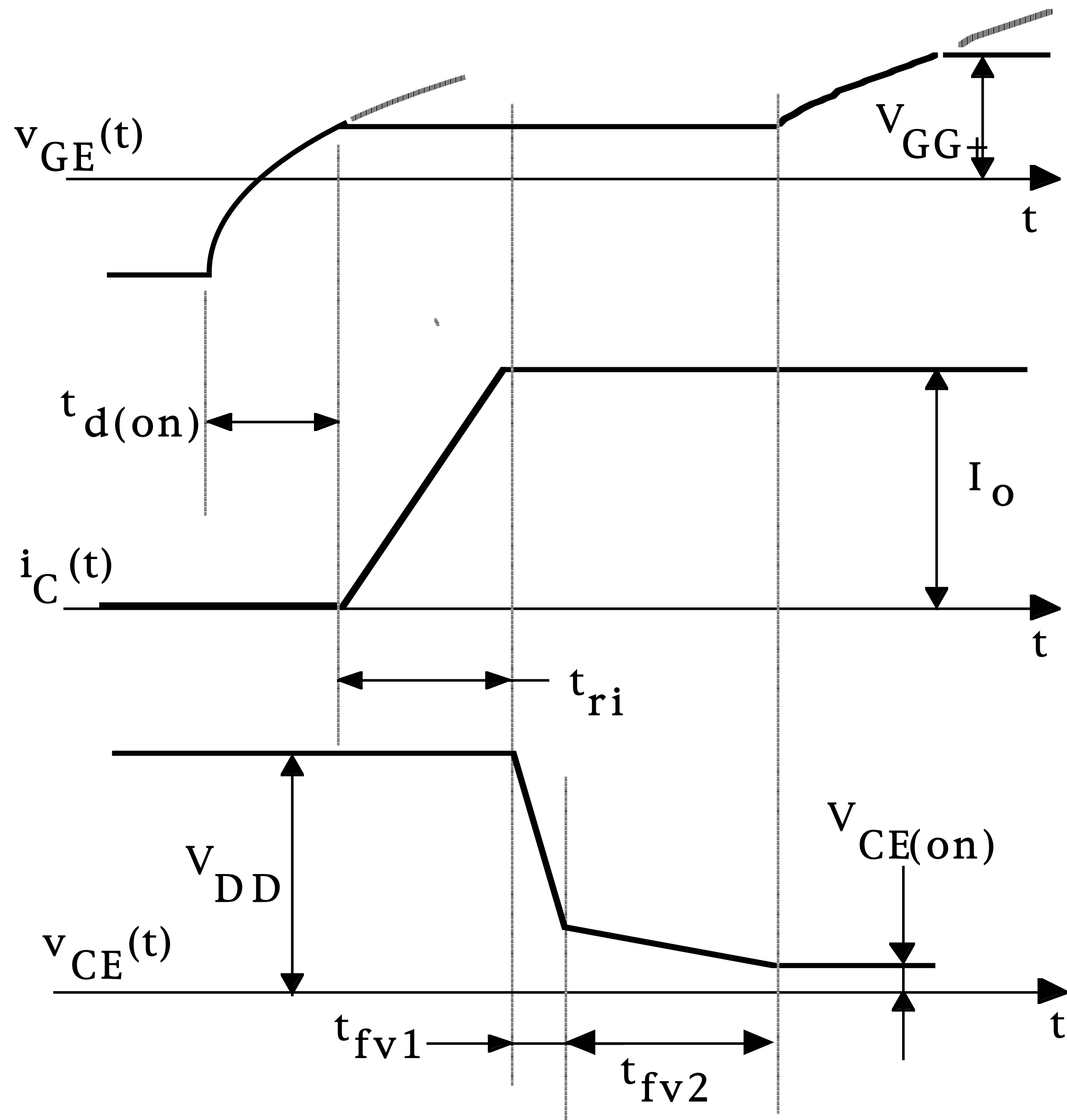
IGBT Turn-on Waveforms

- Turn-on waveforms for IGBT embedded in a stepdown converter.
- Very similar to turn-on waveforms of MOSFETs.
- Contributions to t_{vf2}.
  - Increase in C_{ge} of MOSFET section at low collector-emitter voltages.
  - Slower turn-on of pnp BJT section.



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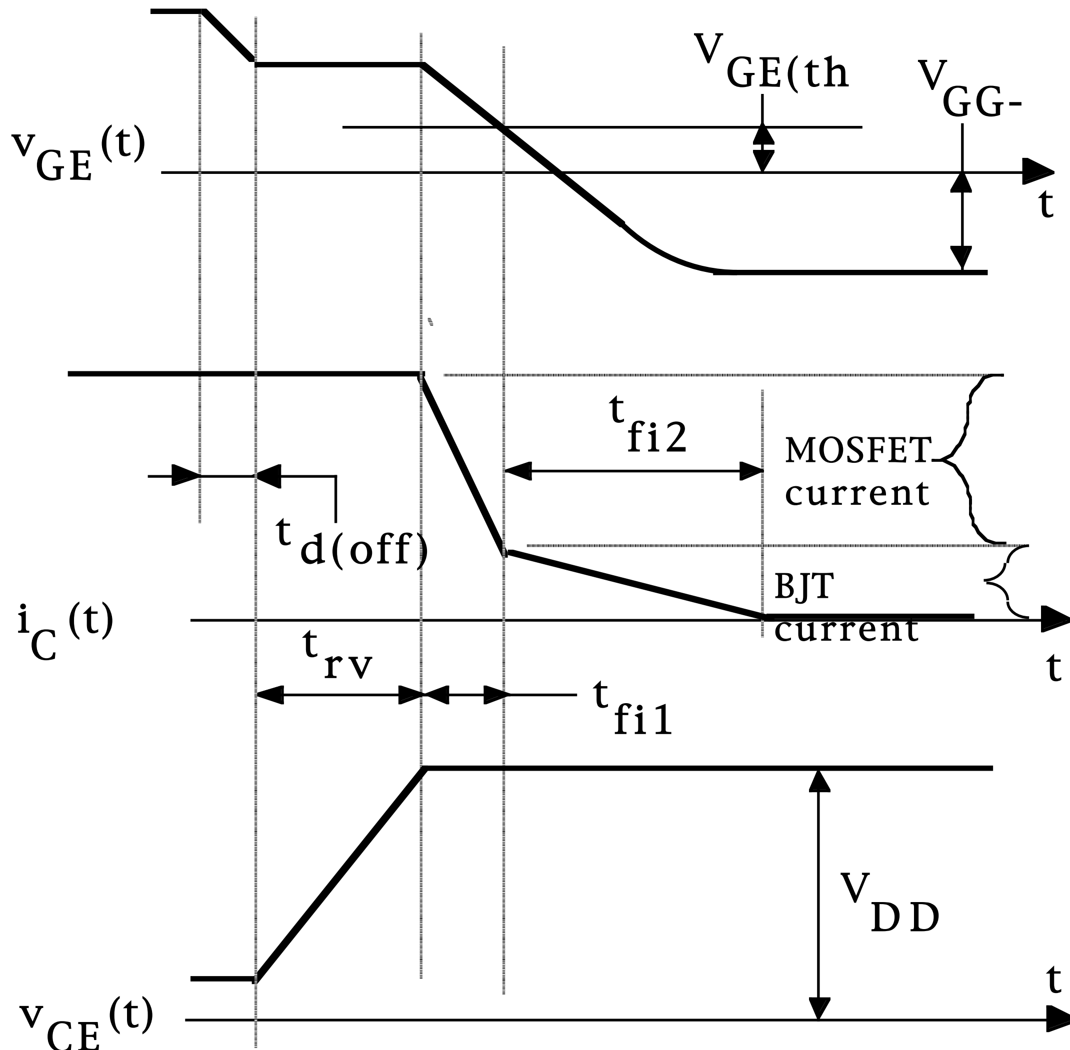
IGBT Turn-off Waveforms



- Turn-off waveforms for IGBT embedded in a stepdown converter.
- Current "tailing" (t_{fi2}) due to stored charge trapped in drift region (base of pnp BJT) by rapid turn-off of MOSFET section.
- Shorten tailing interval by either reducing carrier lifetime or by putting N^+ buffer layer adjacent to injecting P^+ layer at drain.
- Buffer layer acts as a sink for excess holes otherwise trapped in drift region becasue lifetime in buffer layer can be made small without effecting on-state losses - buffer layer thin compared to drift region.

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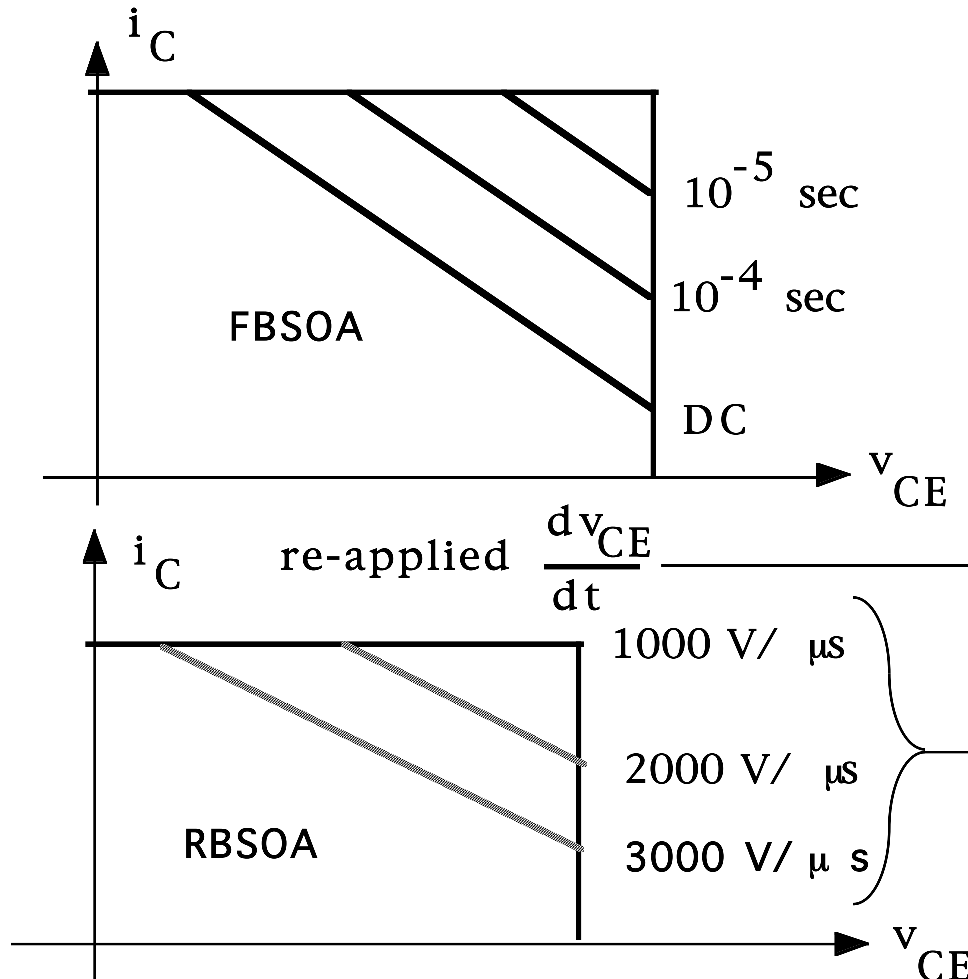
IGBT Safe Operating Area



- Maximum collector-emitter voltages set by breakdown voltage of pnp transistor - 2500 v devices available.
- Maximum collector current set by latchup considerations - 100 A devices can conduct 1000 A for 10 µsec and still turn-off via gate control.
- Maximum junction temp. = 150 C.
- Manufacturer specifies a maximum rate of increase of re-applied collector-emitter voltage in order to avoid latchup.

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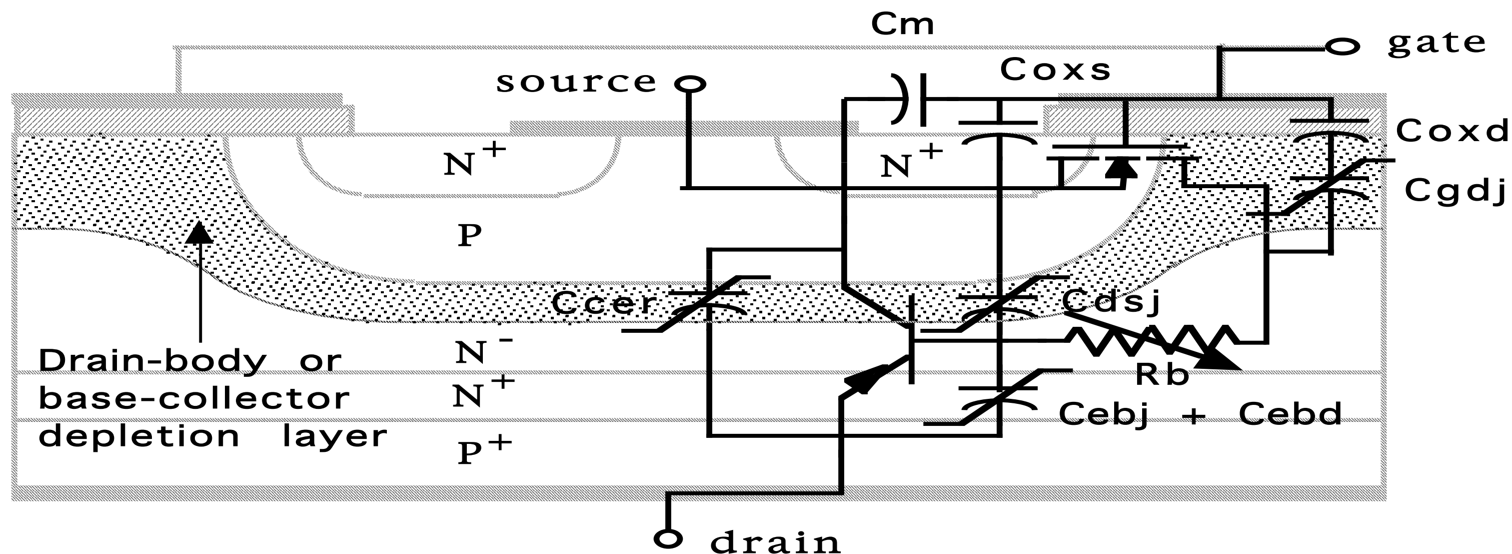
Development of PSpice IGBT Model



- Nonlinear capacitors Cdsj and Ccer due to N^-P junction depletion layer.
- Nonlinear capacitor Cebj + Cebd due to P^+N^+ junction
- MOSFET and PNP BJT are intrinsic (no parasitics) devices
- Nonlinear resistor Rb due to conductivity modulation of N^- drain drift region of MOSFET portion.
- Nonlinear capacitor Cgdj due to depletion region of drain-body junction (N^-P junction).
- Circuit model assumes that latchup does not occur and parasitic thyristor does not turn.

- Reference - "An Experimentally Verified IGBT Model Implemented in the SABER Circuit Simulator", Allen R. Hefner, Jr. and Daniel M. Diebolt, IEEE Trans. on Power Electronics, Vol. 9, No. 5, pp. 532-542, (Sept., 1994)

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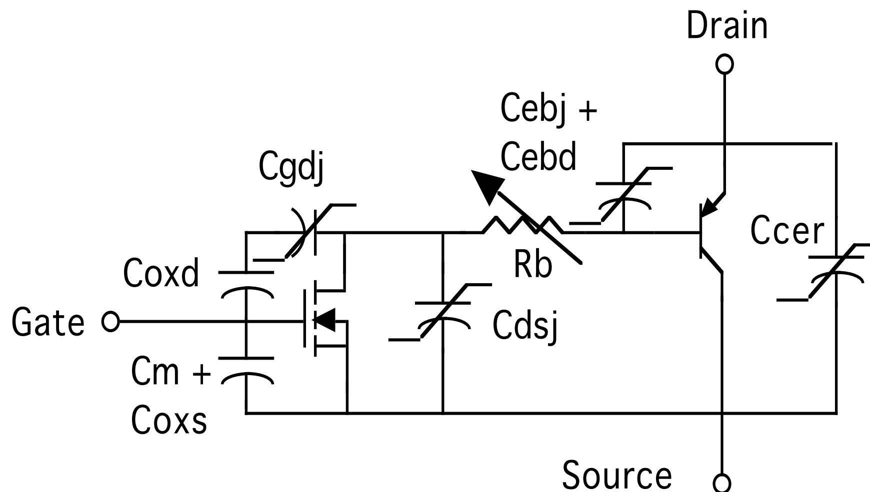
Parameter Estimation for PSpice IGBT Model

- Built-in IGBT model requires nine parameter values.
  - Parameters described in Help files of Parts utility program.

- Parts utility program guides users through parameter estimation process.
  - IGBT specification sheets provided by manufacturer provide sufficient informaiton for general purpose simulations.
  - Detailed accurate simulations, for example device dissipation studies, may require the user to carefully characterize the selected IGBTs.



- Built-in model does not model ultrafast IGBTs with buffer layers (punch-through IGBTs) or reverse free-wheeling diodes

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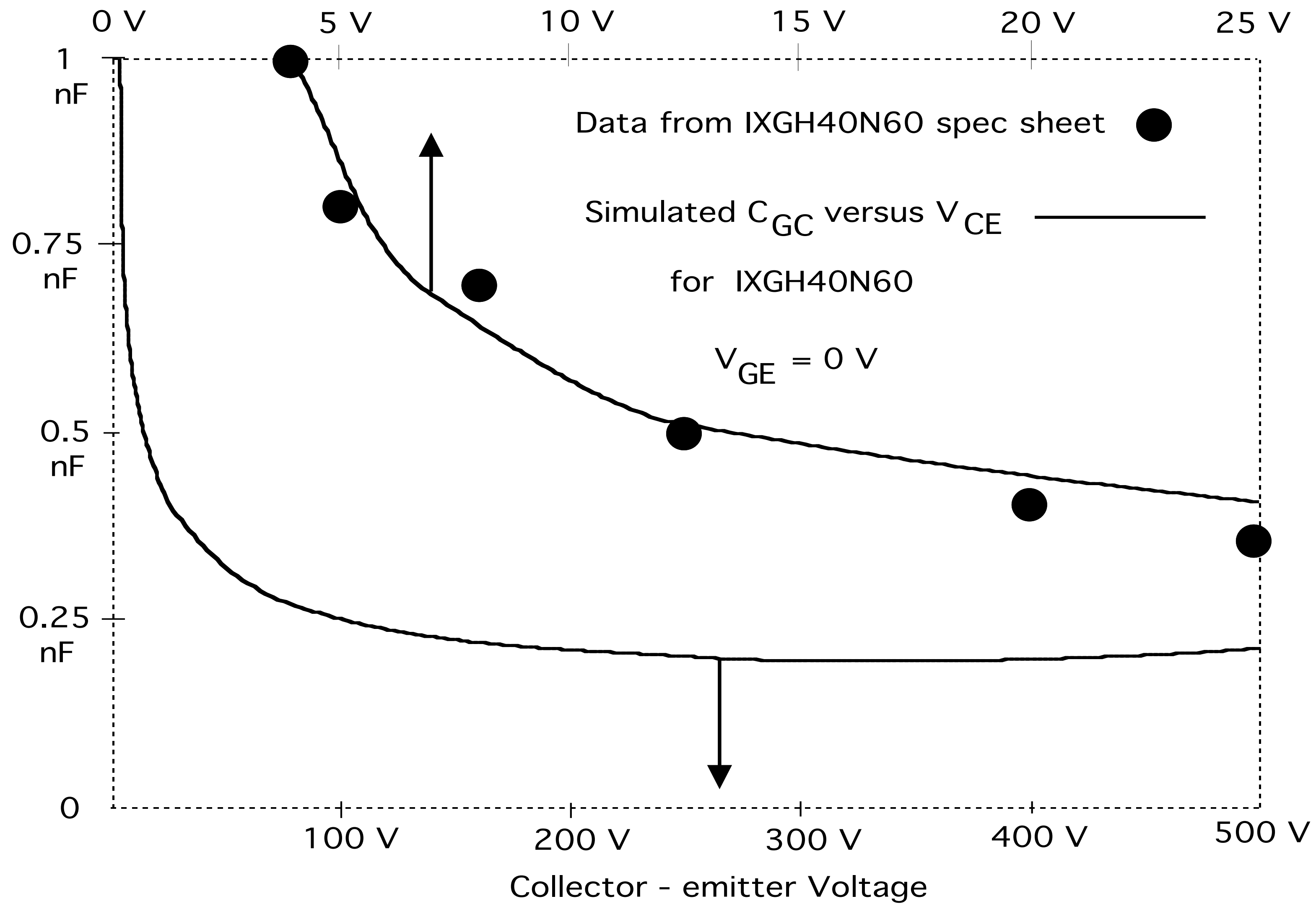
PSpice IGBT - Simulation Vs Experiment



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