WaveFormer Pro & PeakVHDL

SynaptiCAD's WaveFormer Pro is a graphical timing diagram editor with the ability to generate stimulus vectors for Accolade's PeakVHDL simulator. WaveFormer Pro lets you specify and analyze timing diagrams early in the design cycle, then take that same work and use it as stimulus for circuit simulation. With WaveFormer, users create timing diagrams by drawing signals, clocks, busses, and simulating Boolean and registered logic signals. Graphical timing parameters like delays, setups, and holds actively move and monitor signal transitions.

Analyze Timing before creating a Schematic or HDL Model Generate Stimulus Vectors Annotate and Document Simulation Waveforms

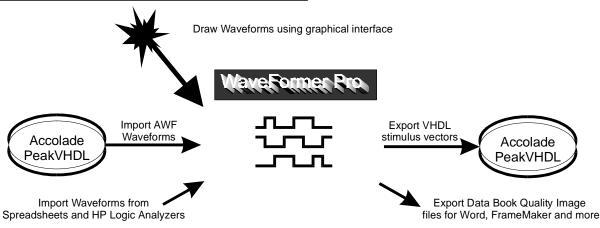
WaveFormer Pro - wrcy File Export Edit Draw B	_	: <u>V</u> iew <u>O</u> j	otions <u>R</u> epor	t <u>W</u> indow <u>H</u> elp	_ _ X
Diagram Add Signal Add Bus Add Clock Add Spacer 95.00ns 45.00ns 0	Hold Text	Marker	-~ :-		20011 54
CLKD	\$	ClkSe	tup Intera		250ns 250ns 400 2500 2500 2500 2500 2500 2500 2500
Data[7:0]	Image: Constraint of the second sec				Name: Enable Properties Active low name (adds bar on top, \$8AR suffix)
Request Addr[7:0] F Enable	FFX A3 X				Boolean Equation: ex. (SIG1 and SIG2) delay 5 (Addr == hA3) & (!Request\$BAR)
Parameter 110 * GateDelay + 5					Clock: Unclocked T Edge/Levet: neg T Clock to Out: 0 Setup: 0 Startup State: unknown Hold: 0
name GateDelay	min 2	max 2	margin na (free)	comment Standard ASIC gate delay	Boolean Equation HDL Code
t _{On Delay}	25	45	. ,	tristate to valid data delay	Simulate Once ✓ Continuously Simulate ✓//m Eqn 2ns=Z (5=1 5=0)*5 9=H 9=L 5=V 5=X ▼
ClkSetup	21	,	-1	Request\$BAR to valid after A	Kront Signal Direction: shared output
while (\$time < CLK0_stop_time) begin #(CLK0_low) CLK0 = 1'b1; #(CLK0_high) CLK0 = 1'b0; INS Row:1					VHDL Type: atd_logic Veriog Type: vire Radix bin P Bus MSB: 0 LSB: 0
[wrcycle.v] ve [wrcycle.v]					

Import & Export Waveforms

WaveFormer Pro supports waveform input from a variety of sources including: drawing waveforms graphically in the timing diagram editor, numerical input from a spreadsheet, waveforms captured by HP's logic analyzers, and simulator output generated by Accolade's PeakVHDL simulator. All waveforms can be exported as stimulus vectors.

Advanced VHDL Support

SynaptiCAD provides 2 levels of VHDL test bench generation. WaveFormer Pro produces single timing diagram stimulus generation, which is perfect for testing small designs and models. And WaveFormer's big brother, Test-Bencher Pro generates multi-diagram, self-testing, reactive test benches. TestBencher Pro is perfect for building bus-functional models of microprocessor and bus interfaces.



For more information about WaveFormer Pro and TestBencher Pro contact SynaptiCAD at (800)804-7073, www.syncad.com, or sales@syncad.com

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