WaveFormer Pro & Viewlogic

SynaptiCAD's WaveFormer Pro is a graphical timing diagram editor with the ability to generate stimulus vectors for Viewlogic's VHDL, Verilog, SPICE and gate level simulators. WaveFormer Pro lets you specify and analyze timing diagrams early in the design cycle, then take that same work and use it as stimulus for circuit simulation. With WaveFormer, users create timing diagrams by drawing signals, clocks, busses, and simulating Boolean and registered logic signals. Graphical timing parameters like delays, setups, and holds actively move and monitor signal transitions.

Generate Stimulus Vectors Annotate and Document Simulation Waveforms Analyze Timing before creating a Schematic or HDL Model

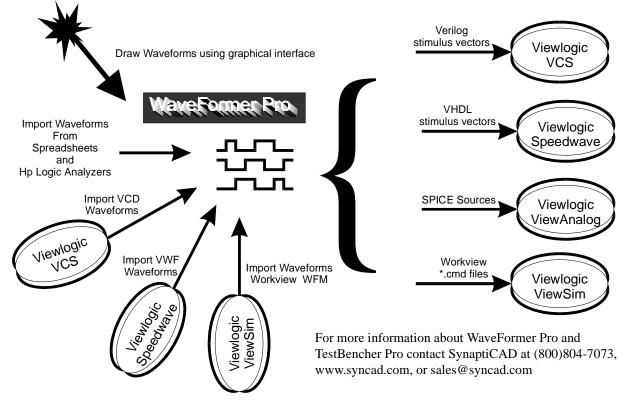
🖉 WaveFormer Pro - wroycle.tim					
File Eyport Edit Draw Bus Libraries View Options Report Window Help					
🖉 Diagram					
Add Signal Add Bus Add Clock Add Spacer	Delay Setu Hold Tex		HIGH LOW	IRI VAL INVA WHI WLO HE	Simulation Zoom In Good Zoom Dut
95.00ns 45.00ns 0ns 150ns (100ns (150ns (200ns (250ns					
ClkSetup Interactive HDL Simulation with editable HDL code					
CLK0			1		Signals Properties Dialog
		L-t,	Dn Delay	t_modelay	
Data[7:0]				valid data	Name: Enable Properties
ReqHold margin=2					active low name (adds bar on top, \$BAR suffix)
Request					Boolean Equation: ex. (SIG1 and SIG2) delay 5
Addr[7:0]	FF) A3)((Addr == 'hA3) & (Request\$8AR)
Enable					Clock: Unclocked 💌 Edge/Level neg 💌
Parameter					
'10 * GateDelay + 5					Clock to Out: 0 Setup: 0
name	min	max	margin	comment	Startup State: unknown Hold: 0
GateDelay	2	2	na (free)	Standard ASIC gate delay	⊕ Boolean Equation ♦ HDL Code
t _{onDelay}	25	45	na (delay)	tristate to valid data delay	Simulate Once Continuously Simulate
ClkSetup	21		-1	Request\$BAR to valid after A	Wim Eqn ReseZ (5=1 5=0)*5 9=H 9=L 5=V 5=X 💌
Report - C:\WaveForm\wrcycle.v					
while (\$time < CLKD_stop_time)					VHDL Type: std_logic 💌
begin #CLKD low) CLKD = 11b1;					Verilog Type: wire
#(CLK0_high) CLK0 = 110;					Radix bin V Bus MSB: 0 LSB: 0
[wrcvcle.v] VeOKCancelApply					

Import & Export Waveforms

WaveFormer Pro supports waveform input from a variety of sources including: drawing waveforms graphically in the timing diagram editor, numerical input from a spreadsheet, waveforms captured by HP's logic analyzers, and simulator output generated by Viewlogicís simulators. Export waveforms as stimulus vectors.

VHDL & Verilog Support

SynaptiCAD provides 2 levels of VHDL and Verilog test bench generation. WaveFormer Pro produces single timing diagram stimulus generation, which is perfect for testing small designs and models. And WaveFormer's big brother, TestBencher Pro generates multi-diagram, self-testing, reactive test benches. Test-Bencher Pro is perfect for building bus-functional models of microprocessor and bus interfaces.



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