

Simulation Frustration?



Get **WaveFormer Pro** for
HDL Power *without* the Pain!

- ✓ **Interactive HDL Simulator**
- ✓ **Timing Diagram Editor**
- ✓ **VHDL, Verilog, SPICE Stimulus Generator**

SynaptiCAD revolutionizes digital design with Interactive HDL Simulation.

Simulate *interactively* with WaveFormer's breakthrough technology: incremental design analysis.

WaveFormer v4.0 is the first EDA tool to incorporate HDL Interactive Simulation (HIS) technology. Changes in design information (logic equations, timing information, component models) and input waveforms *automatically* result in updates to simulation results, providing *instant* feedback on the impact of changes on system functionality and performance. Traditional simulators require a design file or schematics plus a set of test vector stimuli in order to generate simulation results. With WaveFormer's interactive simulator you can design *incrementally*: simulations are performed automatically without the need for complete design information. This allows you to catch mistakes earlier and reduces design time, leaving you more time to optimize your design.

```
'timescale 1ps / 1ps
module testbed(SIG0,CLK0,SIG1);
output SIG0;
reg sig0;
output CLK0;
reg CLK0;
output SIG1;
reg sig1;
initial
begin
//SIGNAL SIG0
SIG0 = 1'b1;
#50000
SIG0 = 1'b0;
#40000
SIG0 = 1'b1;
#90000
SIG0 = 1'b0;
#60000
SIG0 = 1'b1;
#30000
;
end
integer
CLK0_stop_time;
integer
CLK0_period;
CLK0_duty,CLK0_of
freq;
integer CLK0_d1;
CLK0_d2;
initial
begin
//CLOCK CLK0
CLK0_stop_time =
```



Enter design info quickly with WaveFormer's intuitive Logic Wizard and graphical stimulus interface.

Two of the most common complaints about programming in traditional HDL simulators are: (1) it's easy to make syntax errors when writing modeling code and (2) test vector stimulus coding is time-consuming and tedious. WaveFormer eliminates both of these problems: (1) WaveFormer has a point-and-click design equation editor that allows quick modeling of the most common types of models (combinatorial logic, latches, and registers) using VHDL, Verilog, or PAL-type syntax; and (2) WaveFormer's timing diagram editor allows test vector stimuli to be drawn graphically. These two features combined with WaveFormer's automatic resimulation feature create a very comfortable and intuitive design environment.

Get complete control of system timing with min-max timing analysis.

WaveFormer offers full control of simulation timing with global and locally settable options for min, max, and worst case (min-max) timing simulation. Delay, setup, and hold information can also be specified globally or locally for system memory elements. Timing information can be specified using constants or timing parameter variables that can contain mathematical expressions.

Export your design as a complete HDL model when you're done.

WaveFormer generates a *complete* HDL model from the information you enter. This model can then be simulated or analyzed by third party tools such as traditional HDL simulators, synthesis tools, back annotation programs, load and power analysis software, etc. This allows you to move to the next step in your design process *without* having to reenter your design information.

Zero Learning Curve: No previous HDL training required!

Normally there is some learning curve associated with learning a new simulator (even gate-level simulators require you to learn their test vector format), and this is especially true with traditional HDL simulators. Simulating with WaveFormer doesn't require HDL programming skills since a design can be described with simple Boolean equations and test vectors can be drawn *graphically*. WaveFormer makes an excellent training tool for learning HDL coding since WaveFormer can switch back and forth between an equation description and the resulting HDL code. In addition, WaveFormer supports direct entry of native HDL code with immediate resimulation, enabling new users to quickly gain an understanding of the operation of HDL statements.

We've changed the face of HDL simulation. The secret?

WaveFormer Pro reads your mind and generates the desired HDL code.

Or maybe it just feels that way.

Experience it for yourself. Download it for FREE at www.syncad.com.



Design Smarter with WaveFormer Pro.

How do you design with WaveFormer Pro?

WaveFormer Pro is a synergistic combination of 3 tools in one: a timing diagram editor, an interactive HDL simulator, and a stimulus generator. With WaveFormer Pro you begin your design cycle by constructing timing diagrams that define your system requirements using the timing diagram editing and boolean simulation features. The Logic Wizard allows you to rapidly design digital circuits without having to create schematic or HDL models to verify basic functionality. The timing diagram editing features calculate critical timing paths and automatically assure that timing requirements are met. If you then simulate your design, you can use the stimulus generator features to export your waveforms to drive your favorite gate-level or HDL simulator for a final check on system functionality. Finally, when it comes time to document your system, your work is already half done since you can create professional quality documentation for your design from the timing diagrams you created at the beginning of your design process (they're also great for impressive design reviews).

Why is designing with WaveFormer Pro so quick?

Designers with WaveFormer Pro have two major advantages over engineers using traditional gate-level and HDL simulators. First, WaveFormer Pro works with circuits at the same level of abstraction (boolean equations, delay paths, timing requirements) as engineers do when they first start formalizing their design. This means designers can rapidly enter the essential elements of their design without having to create schematics or HDL models. The second major advantage is that unlike most EDA tools, WaveFormer Pro is *fully* interactive and gives designers *instant* feedback as they make changes to their design. The combination of these two features, rapid design entry and rapid feedback on system functionality and performance, makes WaveFormer Pro the ideal tool for the iteration intensive process of designing digital circuits and examining design tradeoffs.



Key Features

- ❑ **Built-in static timing analyzer**
- ❑ **Visual display of min and max critical paths**
- ❑ **Interactive HDL Simulator with true min-max timing**
SIG3 = (SIG0 and SIG1) delay 5ns or SIG2 delay D0
- ❑ **Integrated report window for HDL editing**
- ❑ **Temporal Equation Simulator**
SIG3 (H=10ns L=20ns) * 4
- ❑ **Stimulus Generation**
VHDL/Verilog/SPICE/ViewLogic/Mentor and more
- ❑ **Create scalable metafiles and EPS files for Word**
- ❑ **Create FrameMaker MIF images**
- ❑ **Automated common delay removal**
- ❑ **Links to popular simulators and logic analyzers**
- ❑ **Spreadsheet-based test vector generation**
- ❑ **Data Book documentation features**
Complete superscript/subscript/bold/italic support
Realistic parameter names like t_{pd} supported
Active low signal names with over bars (e.g. \overline{WE})
Signal edge and text placement grids
- ❑ **Bus support for VHDL & Verilog**
- ❑ **Clocks with formulas**
- ❑ **State label equations for counter/shifter waveforms**
- ❑ **Hierarchical modeling at all levels**
Behavioral, RTL (33 operators), gate (14 pre-defined n-input logic gates), and switch (9 transistor models)

Order now and start designing faster with fewer mistakes and a 60-day no-risk money back guarantee

OR

Download a free evaluation copy from www.syncad.com and see for yourself how WaveFormer Pro reads your mind.

WaveFormer Pro v4.0 for Windows NT, 95, and 3.1

- First copy \$1750
- Each add'l copy purchased at same time \$1550
- 5 user workgroup license \$6800

WaveFormer Pro v4.0 for UNIX SunOS, Solaris, or HP-UX

- One license (display locked) \$2000
- One licence (floating) \$3500
- 5 user workgroup license \$9500

Optional Software Subscriptions

Subscription owners automatically receive the next 3 updates to WaveFormer Pro from the version that they purchase.

| Purchased | Windows | UNIX |
|-----------------------|------------|------------|
| • With initial order | \$350/copy | \$500/copy |
| • After initial order | \$500/copy | \$700/copy |