



# PAL22V10C PAL22VP10C

## Universal PAL® Device

### Features

- Ultra high speed supports today's and tomorrow's fastest microprocessors
  - $t_{PD} = 6$  ns
  - $t_{SU} = 3$  ns
  - $f_{MAX} = 117$  MHz
- Reduced ground bounce and undershoot
- PLCC and LCC packages with additional  $V_{CC}$  and  $V_{SS}$  pins for lowest ground bounce
- Up to 22 inputs and 10 outputs for more logic power
- Variable product terms
  - 8 to 16 per output

- 10 user-programmable output macrocells
  - Output polarity control
  - Registered or combinatorial operation
  - 2 new feedback paths (PAL22VP10C)
- Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability
- High reliability
  - Proven Ti-W fuse technology
  - AC and DC tested at the factory
- Security Fuse

### Functional Description

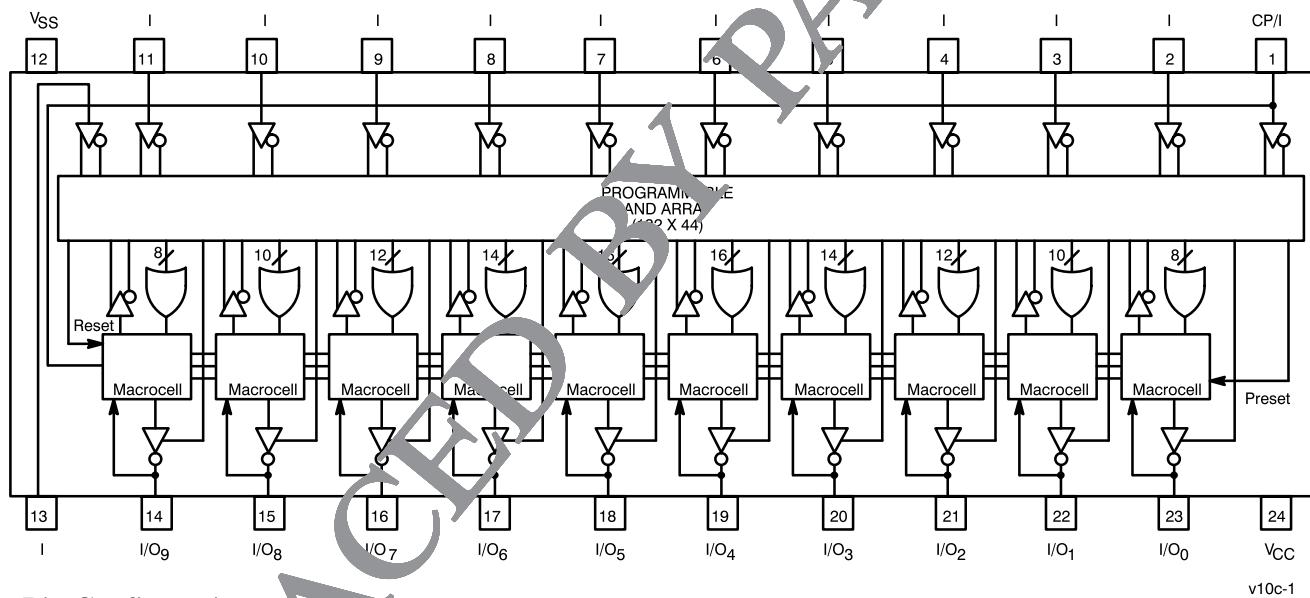
The Cypress PAL22V10C and PAL22VP10C are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10C and PAL22VP10C use the familiar sum-of-products(AND-OR) logic structure and a new concept, the programmable macrocell.

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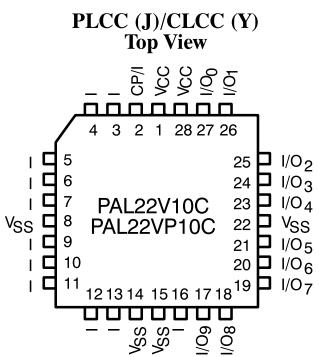
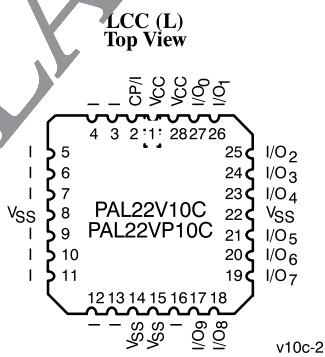
Both the PAL22V10C and PAL22VP10C provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10C and PAL22VP10C feature variable product term architecture, where 8 to 16 product terms are allocated to each output.

### Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



### Pin Configurations



PAL is a registered trademark of Advanced Micro Devices.

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