PRELIMINARY **CY3141**

Warp3™ PROSeries Bolt-In

Features

- **Seamless integration into Viewlogic's PROSeries design environment to provide state-of-the-art PLD/CPLD/FPGA design, synthesis, and simulation. Highlights include:**
  - **— Hierarchical schematic design entry or mixed-mode entry with VHDL**
  - **— IEEE1164 VHDL synthesis provides design retargetablity**
  - **— Full timing simulation and waveform analysis**
  - **— Full Cypress programmable logic device support**
- **Viewlogic's PROSeries design environment provides:**
  - **— Advanced graphical user interface for Windows™**
  - **— Schematic capture (PROcapture)**
  - **— Symbol generator (PROgen)**
  - **— Interactive timing simulator (PROsim)**
  - **— Waveform analyzer (PROwave)**
- **The core of *Warp3*™ bolt-in is an IEEE1164 and 1076 standard VHDL compiler:**
  - **— VHDL is a powerful IEEE standard design language**
  - **— IEEE1164 compliance facilitates design portability across devices and/or CAE environments**
  - **— VHDL facilitates the use of industry-standard simulation and synthesis tools for board and system-level design**
  - **— VHDL facilitates hierarchical design with support for functions and libraries**
- **Support for ALL Cypress UltraLogic™ devices:**
  - **— small PLDs (e.g. 22V10)**
  - **— MAX340 CPLD family**
  - **— FLASH370™ family**
  - **— pASIC38x FPGA family**

Functional Description

The *Warp3* PROSeries Bolt-In is an integration of Cypress's advanced VHDL synthesis and fitting technology into the customer's existing Viewlogic PROSeries CAE design environment.

Design Flow

Figure 1 is a block diagram of the typical design flow of the *Warp3* PROSeries design environment.

The *Warp3* PROSeries design flow begins with design entry which can be done using schematic symbols, text (VHDL), or a combination of both schematic and text. Schematics are entered using the schematic capture tool (PROcapture), and lower-level schematics can be generated into symbols (PROgen) to be used in higher levels, providing a hierarchical design structure. Designs can also be entered in VHDL, and if desired, a symbol can be created for this VHDL block and placed in the schematic. This is especially powerful since some designs (i.e., state machines) are much easier to implement in VHDL than in schematic.

After design entry, all schematic designs are converted to IEEE1164 VHDL (EXPTVHDL in PROcapture). The next step is to compile and synthesize the exported VHDL design (Galaxy). Designs can be targeted to PLDs, CPLDs, and FPGAs. For PLDs, and CPLDs, a JEDEC file is generated for device programming, and timing models are generated for timing simulation. For FPGAs a QDIF file is produced for place and route.

For FPGAs, the next step would be to place and route (SpDE). The place and route result is saved, and a LOF file is generated for device programming. Timing models are also generated for simulation purposes.

Post-synthesis simulation for all PLDs, CPLDs, and FPGAs is done using the timing simulator (PROsim). Waveform analysis of the simulation results can also be done (PROwave).

(**see *Figure 2***)

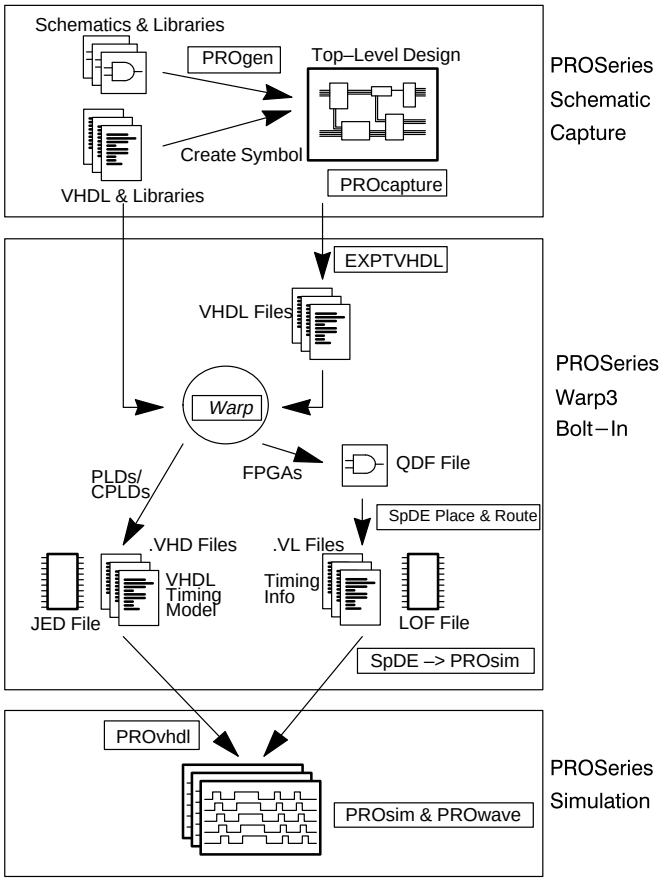

Figure 1. Warp3 PROSeries Design Environment

System Requirements

For PCs

IBM PC-AT or equivalent (486 or higher recommended)

PC-DOS version 3.3 or higher

16 Mbytes of RAM

EGA or VGA display

35-Mbyte hard disk space

1.44-Mbyte floppy disk drive

Two- or three-button mouse

Microsoft Windows Version 3.1

Ordering Information

CY3141 *Warp3* PROSeries Bolt-In:
- 3½-inch, 1.4-Mbyte floppy disks
- Warp3 PROSeries Users Guide
- Warp Synthesis Reference
- Registration Card

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