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PRELIMINARY **CY3146**

Synopsys Design Software Kit for pASIC380™

Features

- **High-level design methodology: VHDL and Verilog input formats**
- **Supports all Synopsys design features**
- **Seamless integration using EDIF 2 0 0 format as interface**
- **Supports the full family of pASIC380 devices**
- **Available on Sun workstation design platforms**

Introduction

Users of the Synopsys Design Compiler can now access Cypress's pASIC380 family of FPGA devices through the seamless integration of the Synopsys Design Software Kit. The kit includes an extensive design macro library for Synopsys and the *Warp*™ SpDE place & route tool.

Functional Description

Design entry in the Synopsys design environment begins with the input of VHDL, Verilog, or a variety of other netlist formats. The design can then be functionally simulated using the VHDL System Simulator (VSS). It then goes through a synthesis and technology mapping process (utilizing the pASIC380 design macro library elements). All Synopsys design methodologies like constraint-driven optimization, finite-state machine extraction, and automatic/manual pad placements are fully supported. The synthesis output (in EDIF 2 0 0 format) then goes into *Warp* SpDE for place & route.

The SpDE place and route tool accepts the EDIF file as input. SpDE generates a LOF file for device programming and timing models (e.g., Verilog, LMC EDIF) for post-synthesis device simulation in many third-party simulators including VSS.

System Requirements

Sun Platform

SPARC CPU

Sun OS 4.1 or later

Motif GUI

16 Mbytes RAM

50 Mbytes of disk space

Floppy drive (for Synopsys libraries)

Cartridge tape drive (for *Warp2+*™ software)

Ordering Information

CY3146 Synopsys pASIC380 FPGA Design Software (Sun-based) includes:

- 3½-inch disk Sun version pASIC FPGA Synopsys Library (1 disk)
- User's Guide
- Registration Card, and
- CY3125 *Warp2*+ for Sun Package which includes:
  - *Warp* Synthesis Reference
  - *Warp2*™ User's Guide
  - *Warp2*+ Software for SUN (1 cartridge)

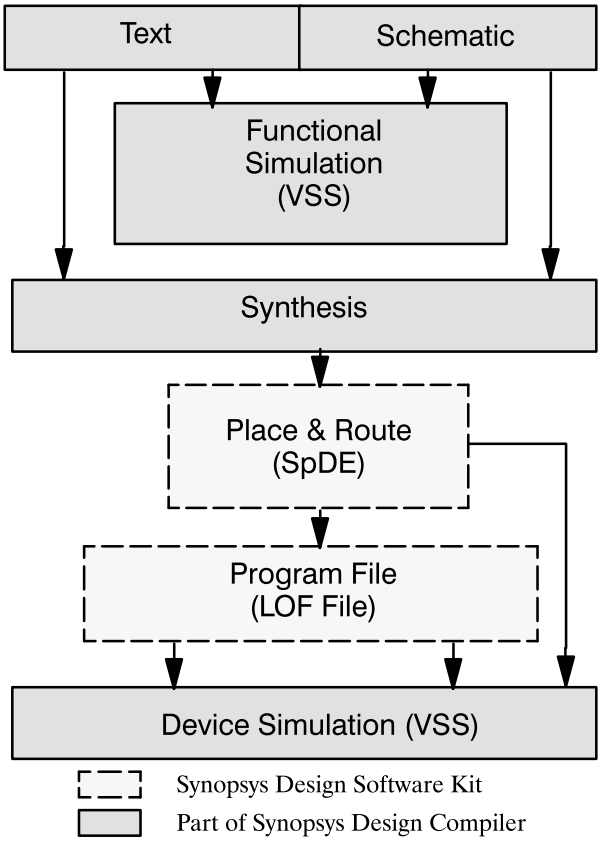

Figure 1. pASIC/Synopsys Design

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