PRELIMINARY

Third-Party Tool Support

Support for Cypress programmable logic devices is available in many software products from third-party vendors. Some companies include support for the entire design process in products that they sell. Others provide software for a portion of the design process (i.e., schematic capture, synthesis, or simulation) and interface with Cypress's *Warp*™ software tools to complete the design flow. This section will describe the design flow using these third-party software products and will describe the interface between these products and Cypress's *Warp* software.

In describing the design flow through these tools, it is useful to break the process into its major functional blocks. *Figure NO TAG* shows these blocks. A similar figure is included for each of the third-party products, and the portions of this flow that are covered by that product are highlighted. Where applicable, the portion of the flow covered by Cypress's *Warp* software is also highlighted.

At the top of each figure are the "Text" and "Sch" blocks. These represent hardware description language (HDL) entry and schematic capture, respectively. Some tools offer design simulation at the design entry stage. This is known as "pre-synthesis" simulation, and is represented by "Simulation" block.

After design entry and simulation are complete, the design description is synthesized. The "Synthesis" block represents the translation of the design description into logic equations, and the optimization of these equations to a device architecture. If targeting a small PLD or CPLD, the next step is device fitting, represented by the "Fitting" block. Here, the logic equations are mapped into the resources of the device. If targeting an FPGA, the next step is automatic place and route, the "APR" block on the figure. Place and route consists of mapping the logic equations into the FPGA logic cells, determining the placement of these logic cells in the device, and the connections between logic cells via routing channels. The result of both "Fitting" and "APR" is a file used to program the device.

The last block in the flow diagram is "Device Sim." This corresponds to simulation of the design according to its implementation in the device. Some simulators will take the timing parameters (i.e., propagation delay) of the device into account, and will provide simulation results consistent with this timing. Others will verify that the programming file is functionally consistent with the design description, but will not contain device timing information.

Finally, along the left of the diagram is the Design Flow Manager. The Design Flow Manager keeps track of the design process for the user. This module typically informs the designer which steps of the design flow have been completed and which have not. This flow manager can also be used to launch vendor tools such as *Warp* synthesis and SpDE place and route.

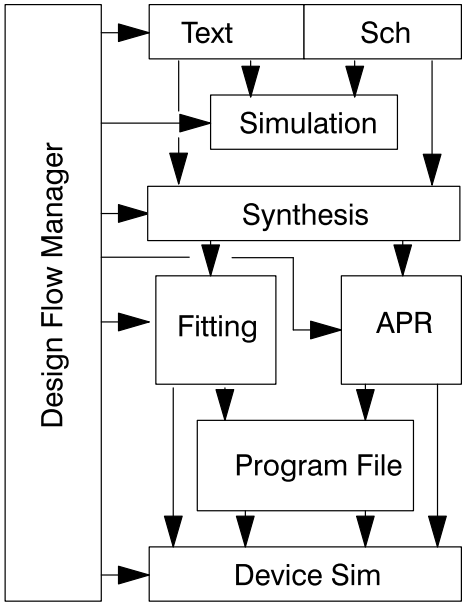

Figure 1

Contents

Acugen

Product

AAQL/ATGEN

Device Support

Small PLDs, MAX340™, FLASH370™, pASIC380™

Input Format

JEDEC file or EDIF

Required Cypress Product

Warp2™, *Warp2+*™, or *Warp3*™ for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Acugen's ATGEN software can automatically generate test vectors to be used with device programmers or with automatic test equipment (ATE) for Cypress PLDs, CPLDs, and FPGAs. For small PLDs and CPLDs, the JEDEC file output by *Warp* is read into the ATGEN software, where test vectors are generated for the design. ATGEN can output a JEDEC file with test vectors to be used on a device programmer, or a test program to be used on a tester. For FPGAs, the flow is the same, but the EDIF file (.edo) output by *Warp*'s place and route software, SpDE, is first translated to JEDEC format by Acugen's AAQL software.

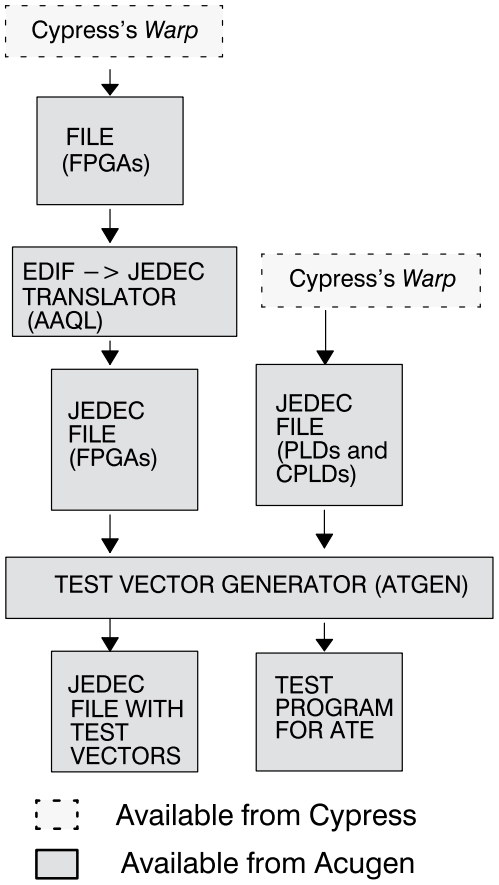

Figure 2

Aldec

Product

Active-CAD

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

Schematic Entry and VHDL

Required Cypress Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Active-CAD integrates with the *Warp* tools through the Active Design Manager. Designs entered as schematics or VHDL can be functionally simulated and then fed into *Warp* for synthesis and fitting (for small PLDs, MAX340, and FLASH370) or place and route (for pASIC380). The resulting output files can then be used for device-level simulation and device programming.

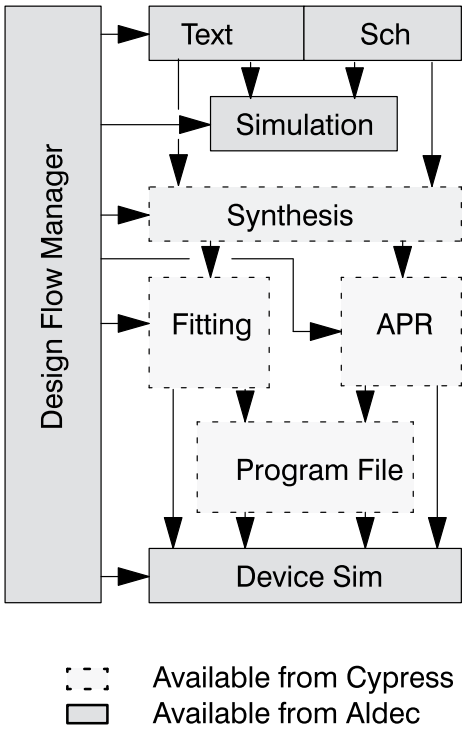

Figure 3

Cadence Design Systems

Product

Cadence Concept or Cadence Composer

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

Schematic Entry and VHDL

Required Cypress Product

Warp2™, *Warp2+*™, or *Warp3*™ for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Both schematic and textual designs (VHDL) are supported using the Cadence Concept or Composer schematic capture tools. The *Warp* software interfaces to these tools and provides the synthesis, fitting and/or automatic place and route steps of the design flow. Timing information and simulation models are then produced by *Warp* and fed back into the Cadence environment for device-level simulation. Programming files are also produced for device programming.

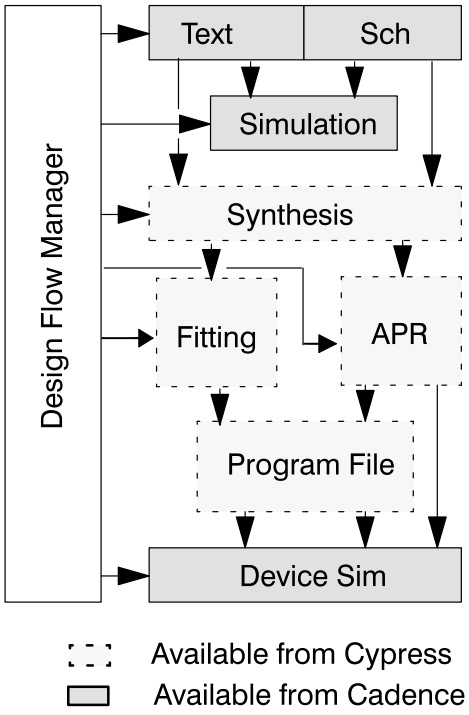

Figure 4

Cadence Design Systems

Product

PIC Designer

Device Support

Small PLDs, MAX340, FLASH370

Input Format

Schematic Entry, VHDL, and Verilog

Required Cypress Product

None

Design Flow Description

Both schematic and textual (VHDL) design entry are supported in PIC Designer. Source-code simulation is used to catch design errors before the design is synthesized and fit to a Cypress PLD or CPLD. PIC Designer then synthesizes the design description, optimizes it, and fits it to the target device. A JEDEC file is output for device programming and timing simulation using PIC Designer's simulator.

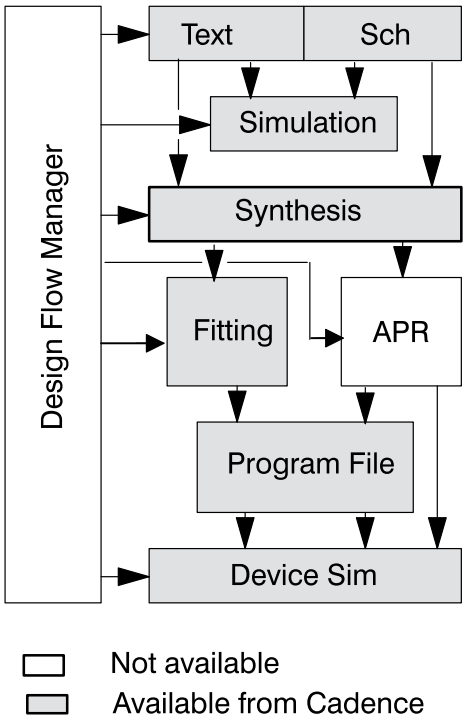

Figure 5

Data I/O

Product

ABEL4, ABEL5, and ABEL6

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

ABEL−HDL

Required Product

None for Small PLDs or MAX340

Cypress ABEL Fitter Kit for FLASH370 (CY3140)

Data I/O pASIC Fitter Kit for pASIC380

Design Flow Description

Designs entered in ABEL−HDL can first be functionally simulated using PLASIM and then go through logic optimization and minimization. The output files from ABEL will then go through fitting or place and route. The resulting output files can then be used for device-level simulation and device programming.

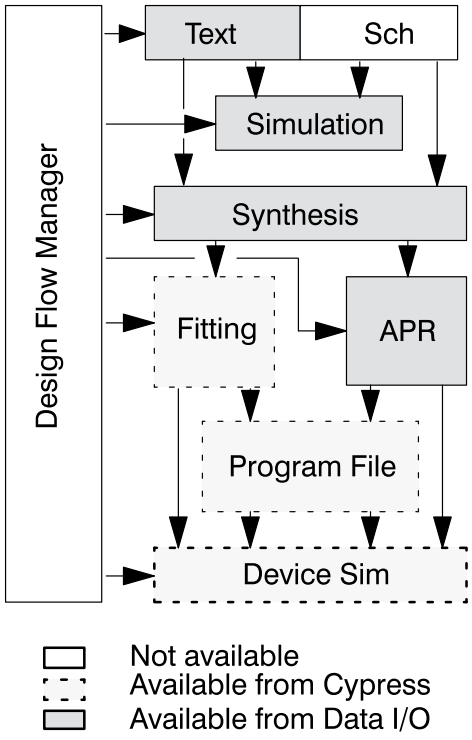

Figure 6

Data I/O

Product

Synario

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

Schematic Entry, VHDL, and ABEL−HDL

Required Product

None for Small PLDs or MAX340

Cypress ABEL Fitter Kit for FLASH370 (CY3140)

Data I/O pASIC Fitter Kit for pASIC380

Design Flow Description

The user is guided through the design process by the Project Navigator. Designs can be entered in schematic entry, VHDL, or ABEL-HDL. Designs entered can be functionally simulated and then optimized by Synario. The designs will then go through fitting or place and route. The resulting output files can be used for device-level simulation and device programming.

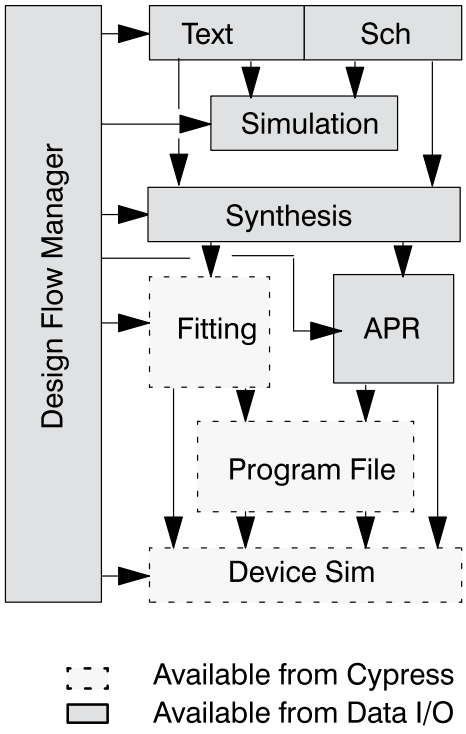

Figure 7

Exemplar Logic

Product

Galileo

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

VHDL, Verilog, OpenABEL, Berkeley PLA, EIL, EDIF, ADL, XNF

Required Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Exemplar Logic's Galileo synthesis software accepts any of the above file formats and synthesizes the logic to any of the Cypress programmable logic devices. Galileo outputs a PLA file that can be read into any of the *Warp* tools, where device fitting and JEDEC (programming file) output occurs for any of the small PLDs, MAX340 CPLDs, or FLASH370 CPLDs. If the target architecture is the pASIC380 FPGA family, Galileo outputs a QDIF file that is read into the *Warp* place and route software. After place and route, a programming file is output. Galileo also provides timing simulation for the design once fitting or place and route have been performed.

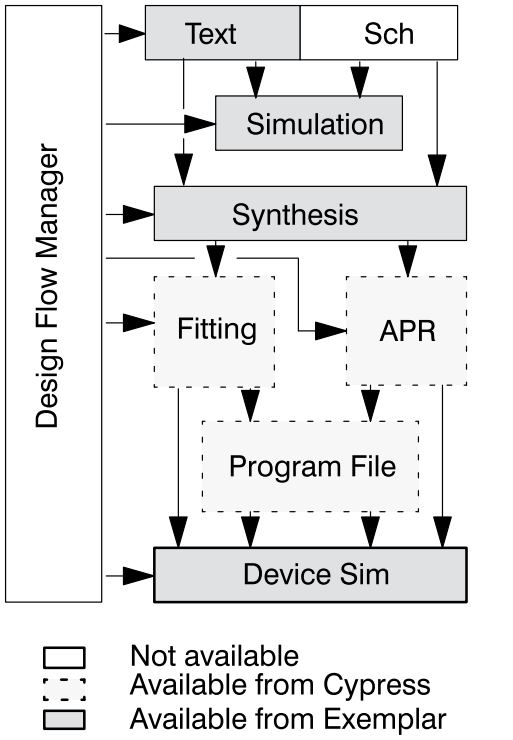

Figure 8

Flyn Systems

Product

FS-ATG

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

JEDEC file or EDIF

Required Cypress Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Using FS-ATG from Flynn Systems, users can automatically generate test vectors to be used on device programmers or in-circuit testers. For small PLDs and CPLDs, the JEDEC file output by *Warp* is read into the FS-ATG software, where test vectors are generated automatically. The user can enter constraints for this generator as desired. FS-ATG then outputs the JEDEC File with test vectors, to be used on a device programmer. It also outputs test vector files that can be translated for use with an in-circuit tester. This translator will take the test vectors and convert them to an automatic test equipment program. The path for FPGAs is the same, but the input to FS-ATG is an EDIF (.edo) file output by *Warp*'s place and route software, SpDE.

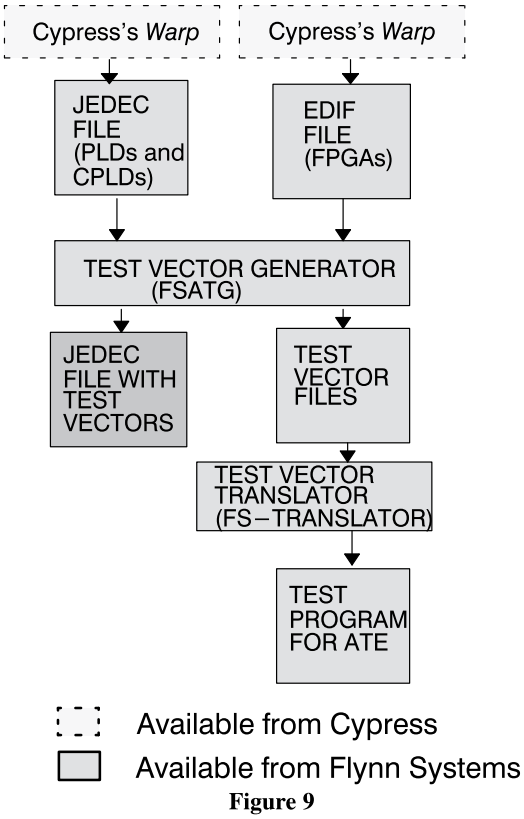

Figure 9

Intergraph

Product

Veribest Design System

Device Support

pASIC380

Input Format

Schematic Entry, Verilog

Required Product

Cypress FPGA Design Kit from Intergraph

Design Flow Description

Design flow begins with setting up a design project with the Design Manager. Design entry can either be schematic (with the ACEPlus Design Capture tool) or Verilog. The design is then compiled into an internal database format using the Compile ACEPlus tool. A Verilog simulation netlist can then be generated for pre-layout simulation. The design is then compiled and synthesized, and an EDIF 2 0 0 output file is generated. This file then goes into the *Warp* SpDE place and route tool. A LOF file is then generated for device programming and timing models for device simulation.

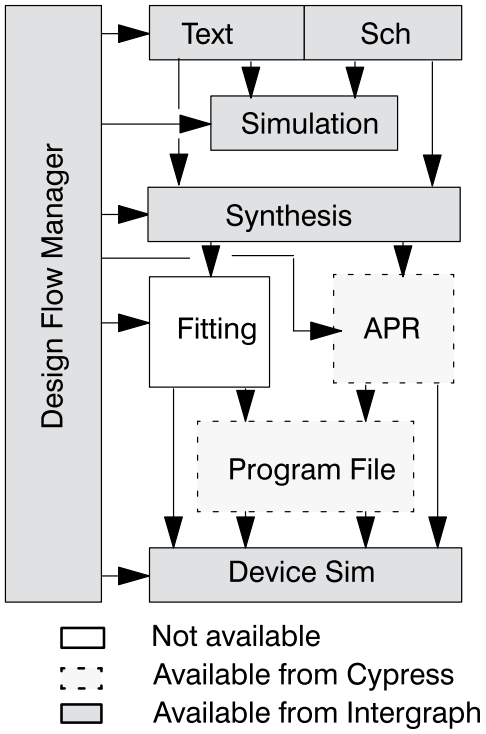

Figure 10

Isdata

Product

LOG/iC

Device Support

Small PLDs, MAX340, FLASH370

Input Format

LOG/iC−HDL

Required Cypress Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Design entry in LOG/iC is done using schematic capture or Isdata's proprietary LOG/iC hardware description language. After design description and debugging of the source code, the design is synthesized and fit to a Cypress PLD or CPLD via the *Warp2*, *Warp2+*, or *Warp3* software. After synthesis and fitting, the software outputs a programming file. Simulation is also available to complete the design flow.

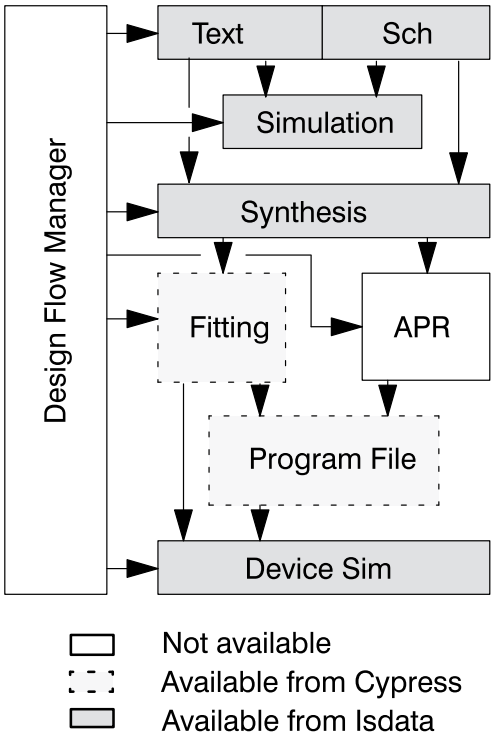

Figure 11

IST

Product

ASYL+

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

VHDL, Verilog, Palasm, OpenABEL, and netlists

Required Cypress Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Designs are entered in HDL or netlist format. After optimization and synthesis, a VHDL file is generated for PLDs/CPLDs, which can be read into *Warp* for fitting. An EDIF or QDIF file can also be generated for pASIC, which would then go into the *Warp* SpDE tool for place and route. Simulation capability is also available from Cypress as well as many other third party tool vendors.

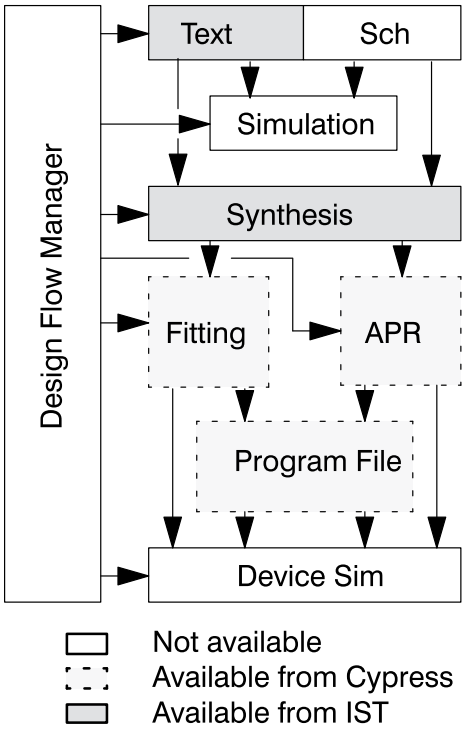

Figure 12

Logical Devices

Product

CUPL

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

CUPL−HDL

Required Cypress Product

None for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Design entry is done using Logical Devices' proprietary CUPL hardware description language. Source-code simulation is used to catch design errors before the design is synthesized and fit to a Cypress device. If the user is targeting a pASIC380 FPGA, a QDIF file is output by CUPL and read into Cypress's *Warp2+* or *Warp3* tool. The design is then placed and routed in the FPGA and a programming file is output.

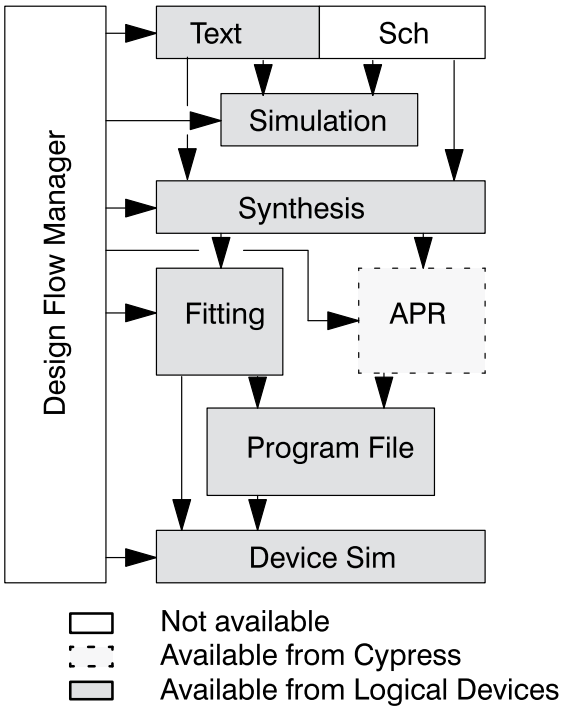

Figure 13

Mentor Graphics

Product

Design Architect

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

Schematic Entry and VHDL

Required Cypress Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Both schematic and textual designs (VHDL) are supported using the Mentor Design Architect schematic capture tool. The *Warp* software interfaces to this tool and provides the synthesis, fitting and/or automatic place and route steps of the design flow. Timing information and simulation models are then produced by *Warp* and fed back into the Mentor environment for device-level simulation. Programming files are also produced for device programming.

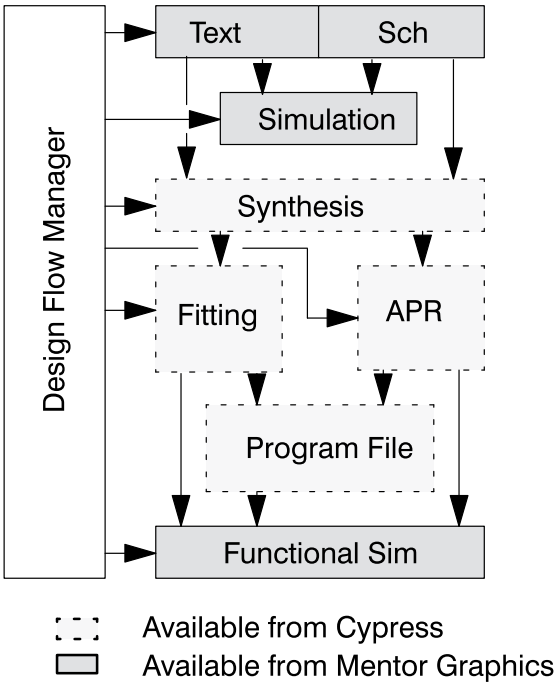

Figure 14

Mentor Graphics

Product

PLDSynthesis II

Device Support

Small PLDs, MAX340, FLASH370

Input Format

Schematic Entry and VHDL

Required Cypress Product

None

Design Flow Description

Both schematic and textual (VHDL) design entry are supported in PLDSynthesis II. Source-code simulation is used to catch design errors before the design is synthesized and fit to a Cypress PLD or CPLD. PLDSynthesis II then synthesizes the design description, optimizes it, and fits it to the target device. A JEDEC file is output for device programming and timing simulation using PLDSynthesis II's simulator.

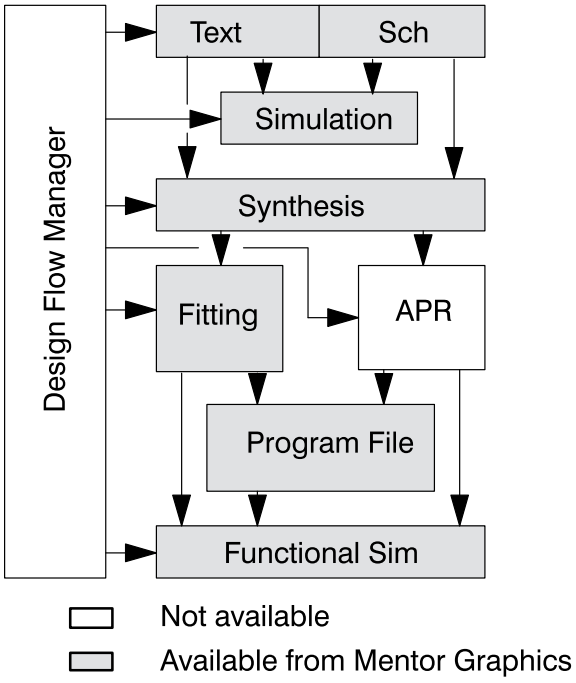

Figure 15

MicroSim

Product

PLSyn

Device Support

Small PLDs, MAX340, and FLASH370

Input Format

Schematic entry and VHDL

Required Cypress Product

None

Design Flow Description

Both schematic and textual (VHDL) design entry are supported in PLSyn. Source-code simulation is used to catch design errors before the design is synthesized and fit to a Cypress PLD or CPLD. PLSyn then synthesizes the design description, optimizes it, and fits it to the target device. A JEDEC file is output for device programming and timing simulation using PLSyn's simulator.

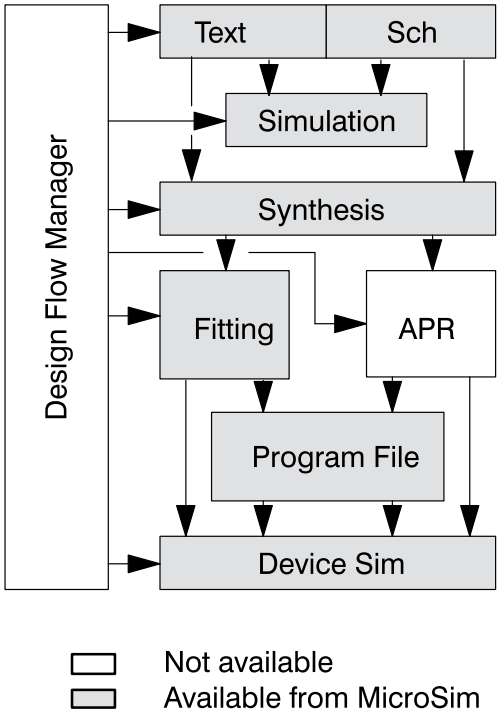

Figure 16

Minc

Product

PLDesigner-XL

Device Support

Small PLDs, MAX340, and FLASH370

Input Format

Minc "Design Synthesis Language" (DSL)

Required Cypress Product

None

Design Flow Description

Design entry is done in PLDesigner-XL using Minc's proprietary hardware description language, DSL. Designs written in DSL are device-independent, but can be made device specific using a physical information file. After entering the design, the user enters constraints for logic synthesis, which includes support for partitioning the design to several PLDs or CPLDs. PLDesigner-XL generates several solutions based on these constraints, and generates a JEDEC programming file for each device targeted. After fitting, the user can functionally simulate the design using Minc's simulator.

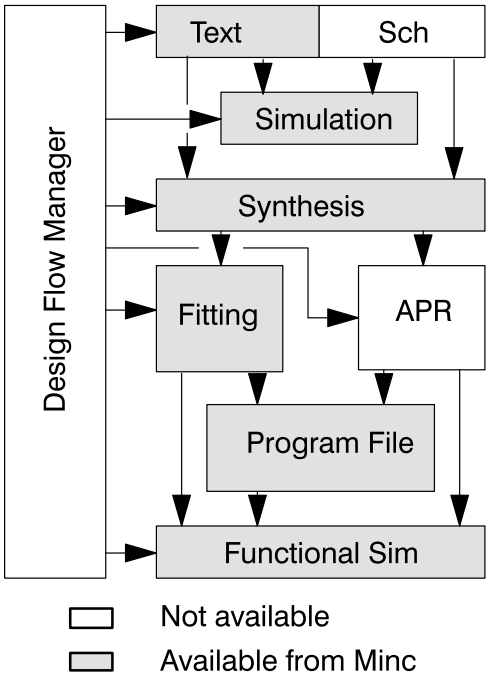

Figure 17

Orcad

Product

PLD386+

Device Support

Small PLDs, MAX340, FLASH370

Input Format

Orcad−HDL

Required Cypress Product

None

Design Flow Description

PLD386+ interfaces to the other tools in Orcad's design software suite to provide complete design entry, synthesis, and simulation. Designs are entered using Orcad's proprietary design language, or by Orcad's schematic capture software. After design description and debugging of the source code, the design is synthesized and fit to a PLD or CPLD from within the PLD386+ software. PLD386+ outputs the programming file, which is also used for device timing simulation to complete the design flow.

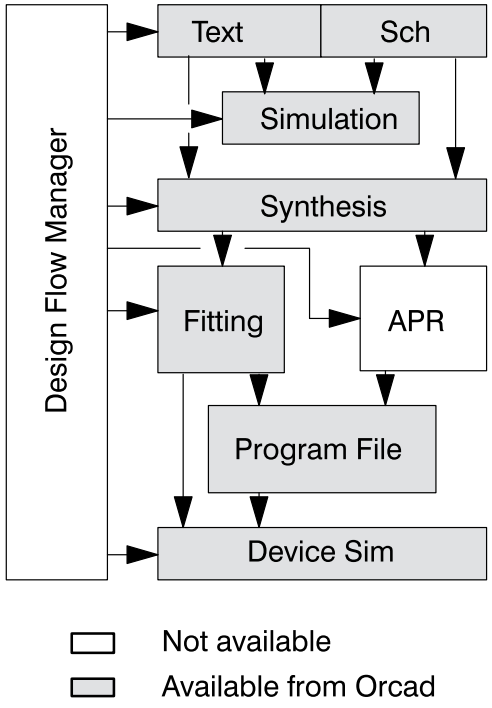

Figure 18

Orcad

Product

Capture for Windows

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

Schematic Entry

Required Cypress Product

Warp2, *Warp2+*, or *Warp3* for small PLDs, MAX340, and FLASH370

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Both schematic and textual designs (VHDL) are supported using the Orcad Capture for Windows schematic capture tool. The *Warp* software interfaces to this tool and provides the synthesis, fitting and/or automatic place and route steps of the design flow. Timing information and simulation models are then produced by *Warp* and fed back into the Orcad environment for device-level simulation. Programming files are also produced for device programming.

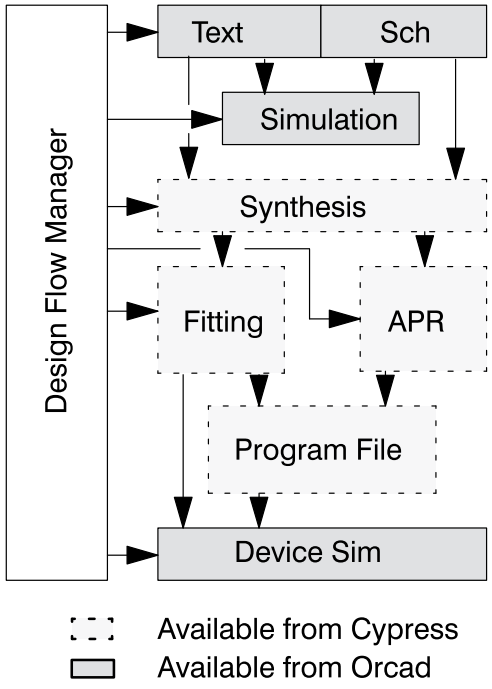

Figure 19

Synopsys

Product

Design Compiler

Device Support

FLASH370, pASIC380

Input Format

VHDL and Verilog

Required Product

Synopsys Design Software Kit for FLASH370

Synopsys Design Software Kit for pASIC380 (CY3146)

Design Flow Description

Designs are entered in either HDL, or netlist format. It can then be functionally simulated using the VHDL System Simulator (VSS). The next step in the process is logic optimization and technology mapping. The output then goes into the *Warp* SpDE place and route tool, or *Warp* fitter, and programming and simulation files are generated for device programming and device-level simulation with VSS.

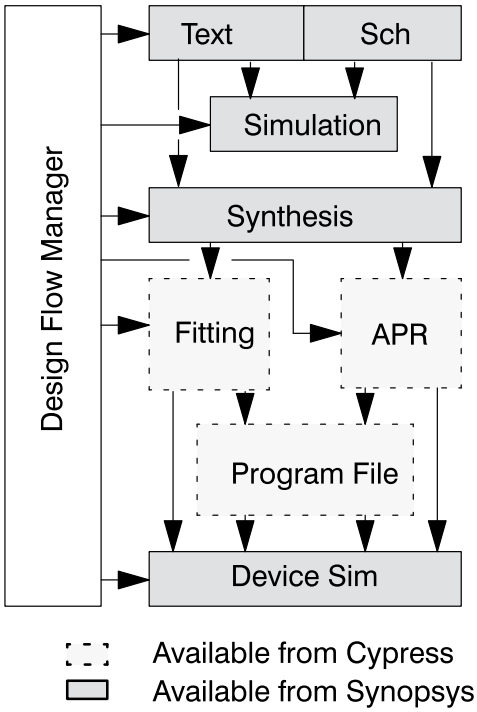

Figure 20

Synplicity

Product

Synplify

Device Support

pASIC380

Input Format

VHDL and Verilog

Required Cypress Product

Warp2+ or *Warp3* for pASIC380

Design Flow Description

Designs are entered in VHDL or Verilog for synthesis with the Synplicity software. The output of synthesis is then fed into the *Warp* place and route software for pASIC380 designs. The place and route software generates the device programming file as well as the simulation model with timing information. Simulation capability is available from Cypress as well as many other third party tool vendors.

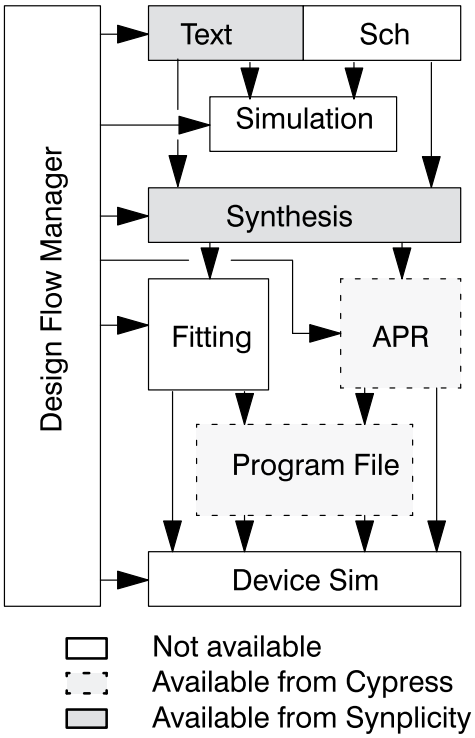

Figure 21

ViewLogic

Product

PROSeries

Device Support

Small PLDs, MAX340, FLASH370, pASIC380

Input Format

Schematic Entry and VHDL

Required Product

Warp3 PROSeries Bolt-In (CY3141)

Design Flow Description

Schematics and/or VHDL files can be used for design entry. The PROSeries design will then be exported into a VHDL file, which would go into the *Warp3* PROSeries Bolt-In for optimization and synthesis. For PLDs and CPLDs, the design will then go through fitting, resulting in a JEDEC file for device programming and timing models for device-level simulation. For pASIC380 devices, a QDF file will be generated, which will go into the SpDE place and route tool within the PROSeries Bolt-In. A LOF file will be generated for device programming, while timing models will be generated for device-level simulation.

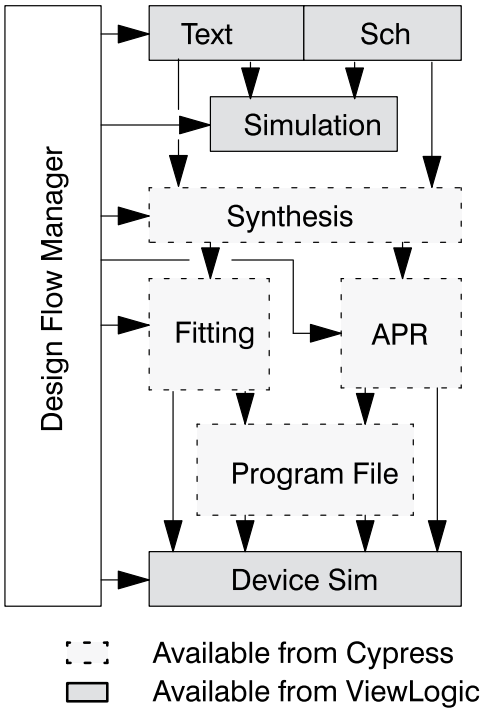

Figure 22

ViewLogic

Product

Workview Plus, Powerview

Device Support

Smal PLDs, MX340, FLASH370, pASIC380

Input Format

Schematic entry and VHDL

Required Cypress Product

Warp3 Workview Plus Bolt-In (CY3131)

Warp3 Powerview Bolt-In (CY3136)

Design Flow Description

Schematics and/or VHDL files can be used for design entry. The design will then be exported into a VHDL file, which would go into the *Warp3* Bolt-In for optimization and synthesis. For PLDs and CPLDs, the design will then go through fitting, resulting in a JEDEC file for device programming and timing models for device-level simulation. For pASIC380 devices, a QDF file will be generated, which will go into the SpDE place and route tool within the *Warp3* Bolt-In. A LOF file will be generated for device programming, while timing models will be generated for device-level simulation.

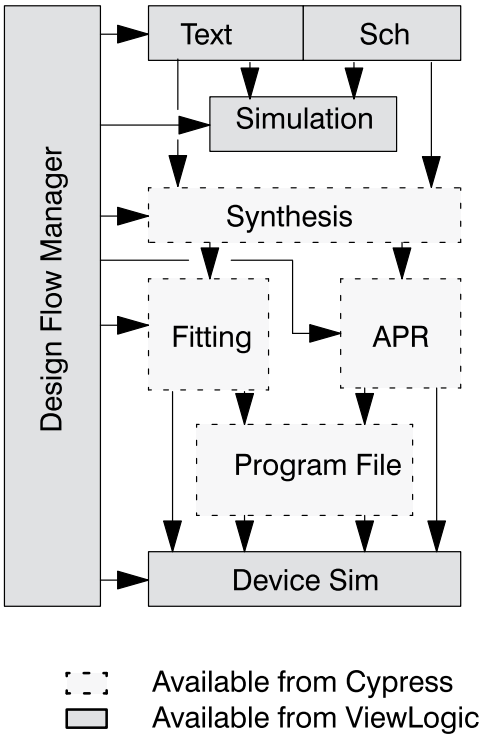

Figure 23

PRELIMINARY **Third-Party Tool Support**

Company Addresses

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(805) 499−6867

Cadence Design Systems, Inc.
555 River Oaks Parkway
San Jose, CA 95134
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Data I/O
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