7c341: 5/28/90
Revision: October 19, 1995

CY7C341B

192-Macrocell MAX® EPLD

Features

- **192 macrocells in 12 LABs**
- **8 dedicated inputs, 64 bidirectional I/O pin**
- **Advanced 0.65-micron CMOS technology to increase performance**
- **Programmable interconnect array**
- **384 expander product terms**
- **Available in 84-pin HLCC, PLCC, and PGA packages**

Functional Description

The CY7C341B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341B is divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C341B allows them to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multifunction chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341B allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341B reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and 8 are buried, while for LABs B, C, D, E, H, I, J, and K, 4 macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

Logic Array Blocks

There are 12 logic array blocks in the CY7C341B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341B provide 8 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C341B may be easily determined using *Warp2™/Warp2+™*, or *Warp3™* software or by the model shown in *Figure 1*. The CY7C341B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* software provides a timing simulator.

Design Recommendations

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

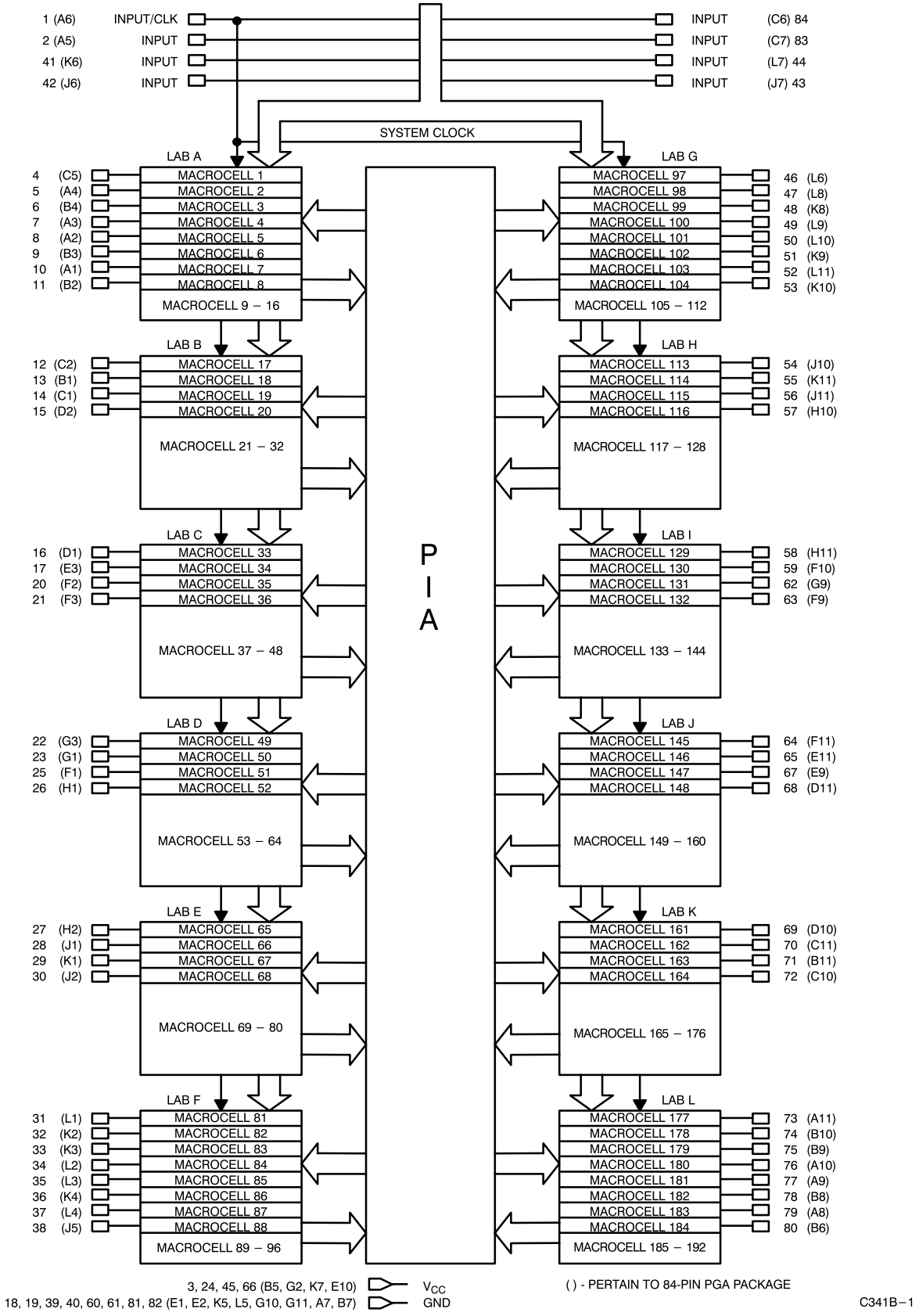
The CY7C341B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

Selection Guide

		7C341B–15	7C341B–20	7C341B–25	7C341B–30	7C341B–35
Maximum Access Time (ns)		15	20	25	30	35
Maximum Operating Current (mA)	Commercial	380	380	380	380	380
	Industrial	480	480	480	480	480
	Military		480	480	480	480
Maximum Standby Current (mA)	Commercial	360	360	360	360	360
	Industrial	435	435	435	435	435
	Military		435	435	435	435

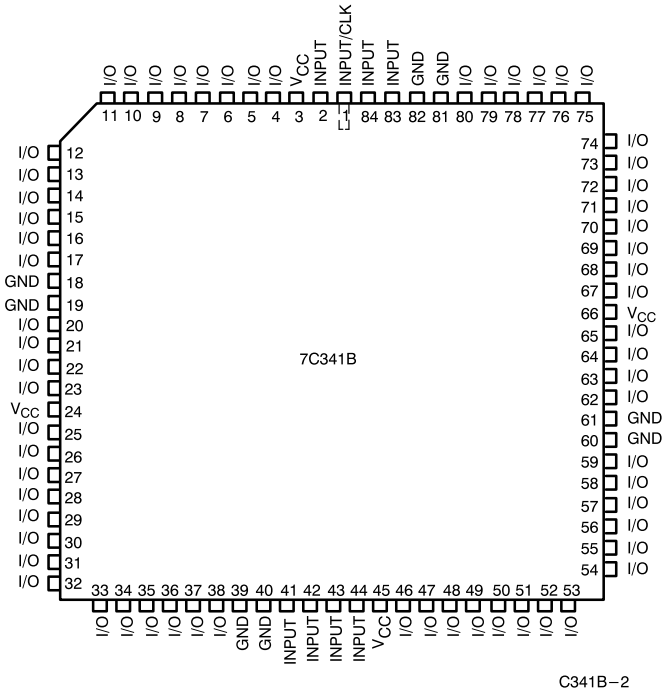
Shaded area contains preliminary information.

Logic Block Diagram

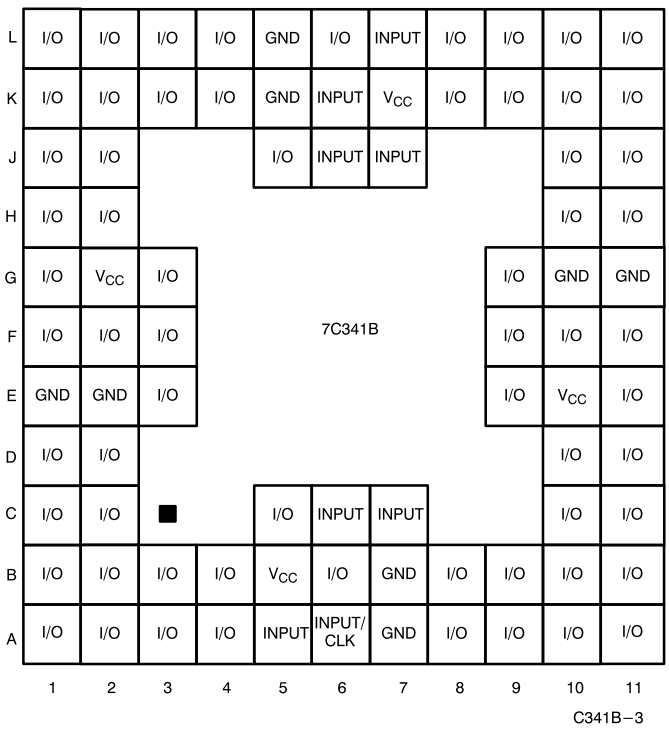


Pin Configurations

PLCC/HLCC
Top View



PGA
Bottom View



Design Security (continued)

The CY7C341B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

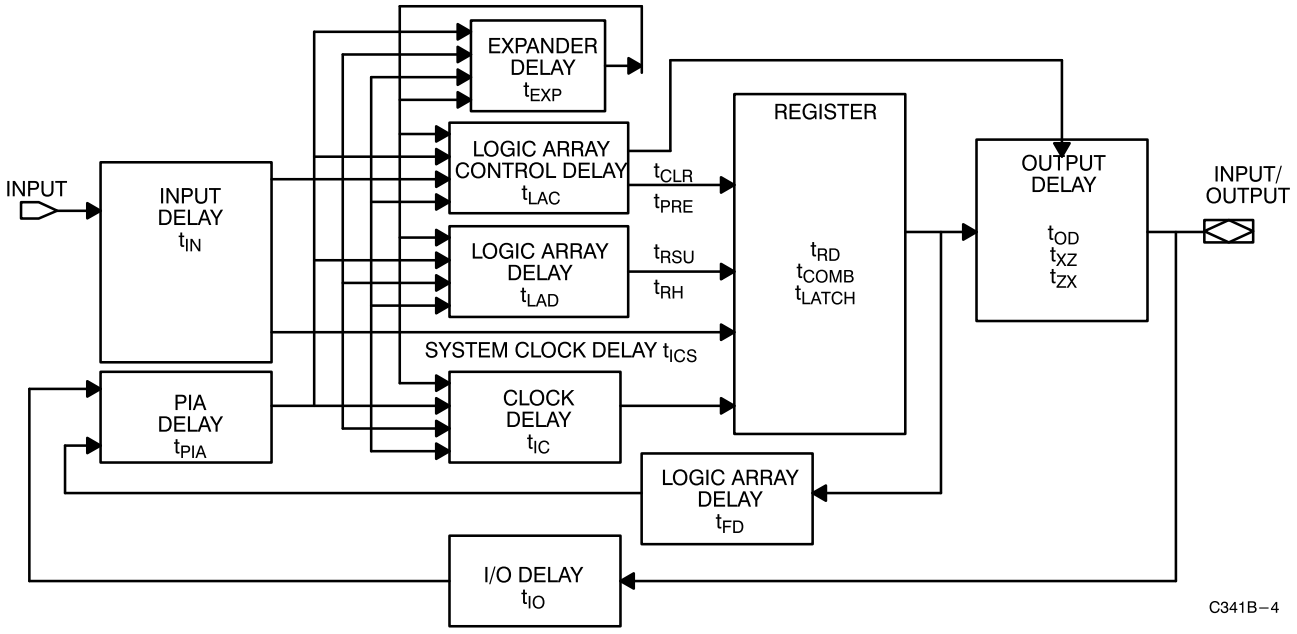


Figure 1. CY7C341B Internal Timing Model

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >1100V (per MIL-STD-883, method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[3, 4]		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Com'l		360	mA
			Mil/Ind		435	mA
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[3, 5]	Com'l		380	mA
			Mil/Ind		480	mA
t_R (Recommended)	Input Rise Time				100	ns
t_F (Recommended)	Input Fall Time				100	ns

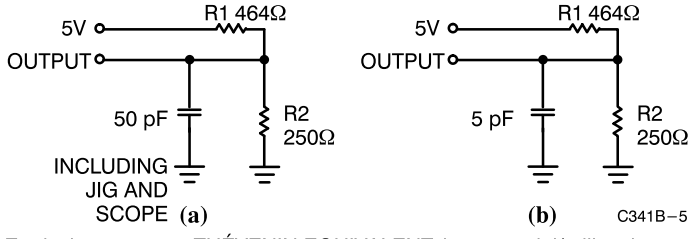
Capacitance[6]

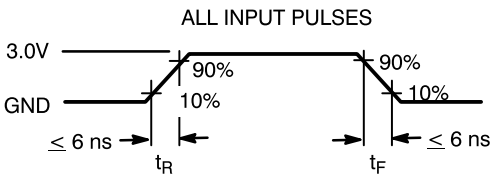
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

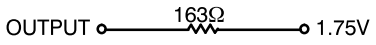
1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Guaranteed but not 100% tested.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB and is tested periodically by sampling production material.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



External Synchronous Switching Characteristics Over the Operating Range[6]

Parameter	Description		7C341B−15		7C341B−20		7C341B−25		7C341B−30		7C341B−35		Unit
			Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l		15		20		25		30		35	ns
		Mil				20		25		30		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l		25		33		40		45		55	ns
		Mil				33		40		45		55	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l		23		30		37		44		55	ns
		Mil				30		37		44		55	
t_{PD4}	I/O Input to Combinatoria l Output Delay with Expander Delay[3, 10]	Com'l		33		43		52		59		75	ns
		Mil				43		52		59		75	
t_{EA}	Input to Output Enable Delay[3, 7]	Com'l		15		20		25		30		35	ns
		Mil				20		25		30		35	
t_{ER}	Input to Output Disable Delay[6]	Com'l		15		20		25		30		35	ns
		Mil				20		25		30		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		7		8		14		16		20	ns
		Mil				8		14		16		20	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[3, 11]	Com'l		17		20		30		35		42	ns
		Mil				20		30		35		42	
t_{S1}	Dedicated Input or Feedback Set-up Time to Synchronous Clock Output[6,12]	Com'l	10		13		15		20		25		ns
		Mil			13		15		20		25		
t_{S2}	I/O Input Set-up Time to Synchronous Clock Input[8]	Com'l	20		24		30		39		45		ns
		Mil			24		30		39		45		
t_H	Input Hold Time from Synchronous Clock Input[6]	Com'l	0		0		0		0		0		ns
		Mil			0		0		0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	5		7		8		10		12.5		ns
		Mil			7		8		10		12.5		
t_{WL}	Synchronous Clock Input Low Time	Com'l	5		7		8		10		12.5		ns
		Mil			7		8		10		12.5		
t_{RW}	Asynchronous Clear Width[3, 6]	Com'l	16		22		25		30		35		ns
		Mil			22		25		30		35		
t_{RR}	Asynchronous Clear Recovery[3, 7]	Com'l	16		22		25		30		35		ns
		Mil			22		25		30		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		15		20		25		30		35	ns
		Mil				20		25		30		35	
t_{PW}	Asynchronous Preset Width[3, 6]	Com'l	15		20		25		30		35		ns
		Mil			20		25		30		35		

Shaded area contains preliminary information.

External Synchronous Switching Characteristics Over the Operating Range[6](continued)

Parameter	Description		7C341B–15		7C341B–20		7C341B–25		7C341B–30		7C341B325		Unit
			Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{PR}	Asynchronous Preset Recovery Time[3, 6]	Com'l	15		20		25		30		35		ns
		Mil					25		30		35		
t_{PO}	Asynchronous Preset to Registered Output Delay[6]	Com'l		15		20		25		30		35	ns
		Mil				20		25		30		35	
t_{CF}	Synchronous Clock to Local Feedback Input[3, 13]	Com'l		3		3		3		3		5	ns
		Mil				3		3		3		5	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[3]	Com'l	12		14		16		20		25		ns
		Mil			14		16		20		25		
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[3, 14]	Com'l	58.8		50		34.5		27.7		22.2		MHz
		Mil			50		34.5		27.7		22.2		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[3, 15]	Com'l	76.9		62.5		55.5		43		33		MHz
		Mil			62.5		55.5		43		33		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[3, 16]	Com'l	100		71.4		62.5		50		40.0		MHz
		Mil			71.4		62.5		50		40.0		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[3, 17]	Com'l	100		71.4		62.5		50		40.0		MHz
		Mil			71.4		62.5		50		40.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[3, 18]	Com'l	3		3		3		3		3		ns
		Mil			3		3		3		3		

Shaded area contains preliminary information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic functions and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.

External Asynchronous Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description		7C341B–15		7C341B–20		7C341B–25		7C341B–30		7C341B–35		Unit
			Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{ACO1}	Dedicated Asynchronous Clock Input to Output Delay[6]	Com'l		15		20		25		30		35	ns
		Mil				20		25		30		35	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output [19]	Com'l		25		32		40		46		55	ns
		Mil				32		40		46		55	
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input[6]	Com'l	5		5		5		6		8		ns
		Mil			5		5		6		8		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[6]	Com'l	14		18		20		27		30		ns
		Mil			18		20		27		30		
t_{AH}	Input Hold Time from Asynchronous Clock Input[6]	Com'l	5		6		6		8		10		ns
		Mil			6		6		8		10		
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	Com'l	9		10		11		14		16		ns
		Mil			10		11		14		16		
t_{AWL}	Asynchronous Clock Input LOW Time[6, 20]	Com'l	7		8		9		11		14		ns
		Mil			8		9		11		14		
t_{ACF}	Asynchronous Clock to Local Feedback Input[21]	Com'l		11		13		15		18		22	ns
		Mil				13		15		18		22	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)	Com'l	16		18		20		25		30		ns
		Mil			18		20		25		30		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[22]	Com'l	50		40		33.3		27		23		MHz
		Mil			40		33.3		27		23		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[23]	Com'l	62.5		55.5		50		40		33.3		MHz
		Mil			55.5		50		40		33.3		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[24]	Com'l	62.5		50		40		33.3		28.5		MHz
		Mil			50		40		33.3		28.5		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[25]	Com'l	62.5		55.5		50		40		33.3		MHz
		Mil			55.5		50		40		33.3		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[26]	Com'l	15		15		15		15		15		ns
		Mil			15		15		15		15		

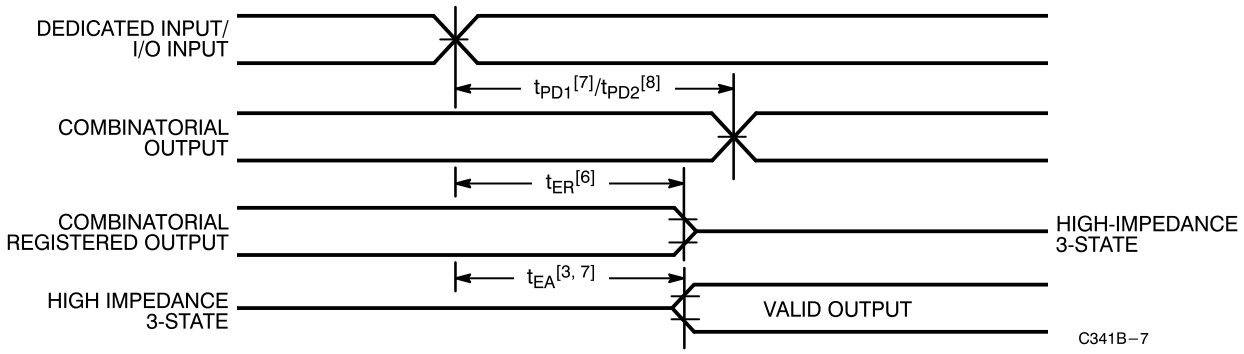
Shaded area contains preliminary information.

Notes:

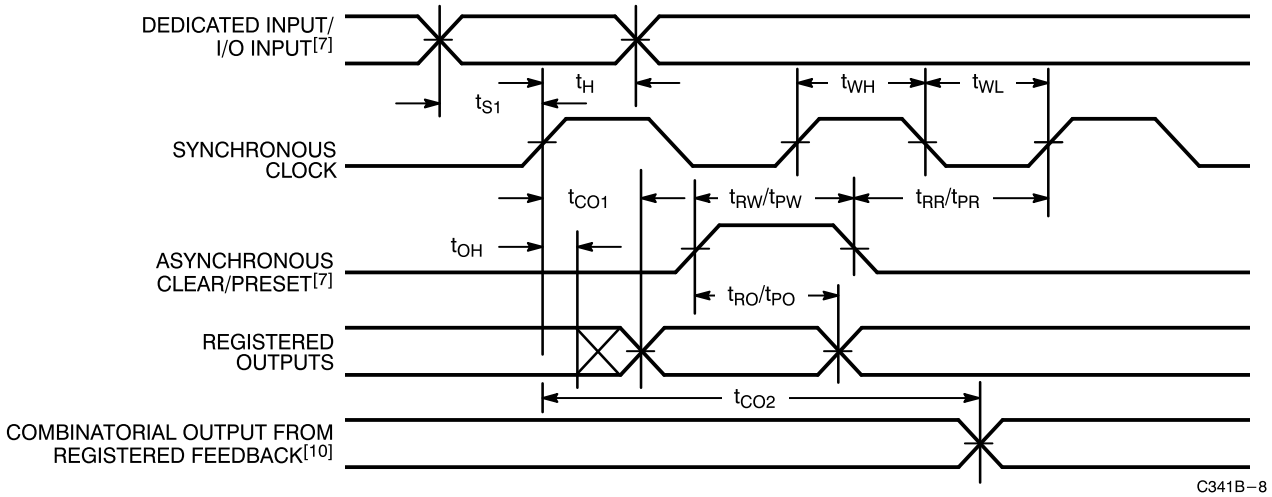
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycle by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.
19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, and assumes there is no expander logic in the clock path and the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.

Switching Waveforms

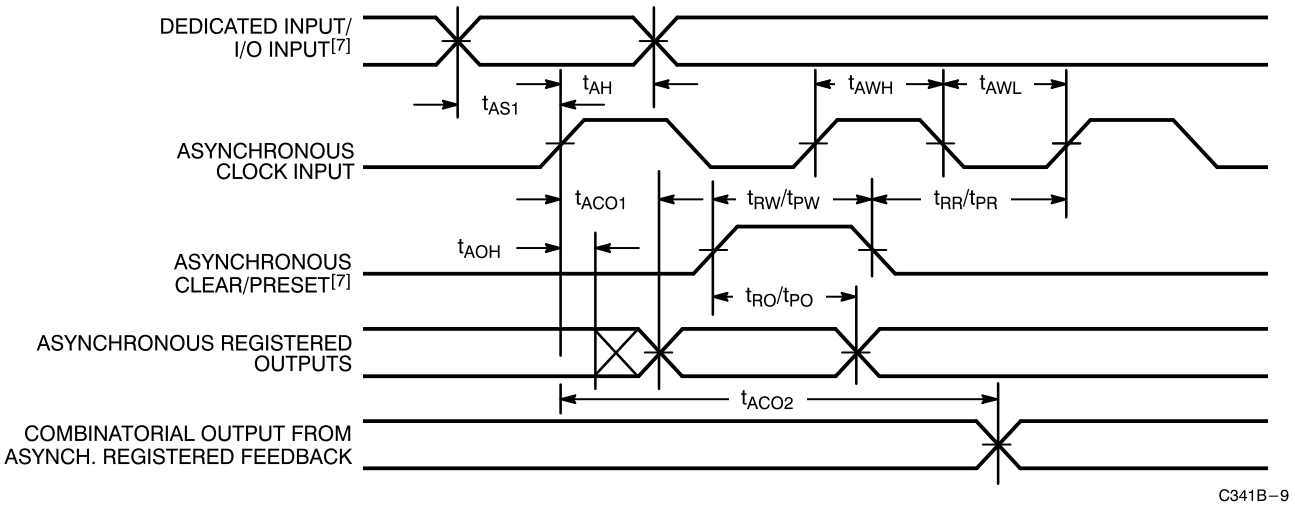
External Combinatorial



External Synchronous



External Asynchronous



Internal Switching Characteristics Over the Operating Range[2]

Parameter	Description		7C341B–15		7C341B–20		7C341B–25		7C341B–30		7C341B–35		Unit
			Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		3		4		5		7		9	ns
		Mil				4		5		7		9	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		3		4		6		6		9	ns
		Mil				4		6		6		9	
t_{EXP}	Expander Array Delay	Com'l		8		10		12		14		20	ns
		Mil				10		12		14		20	
t_{LAD}	Logic Array Data Delay	Com'l		8		10		12		14		16	ns
		Mil				10		12		14		16	
t_{LAC}	Logic Array Control Delay	Com'l		5		7		10		12		13	ns
		Mil				7		10		12		13	
t_{OD}	Output Buffer and Pad Delay	Com'l		3		3		5		5		6	ns
		Mil				3		5		5		6	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l		5		5		10		11		13	ns
		Mil				5		10		11		13	
t_{XZ}	Output Buffer Disable Delay	Com'l		5		5		10		11		13	ns
		Mil				5		10		11		13	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l	4		5		6		8		10		ns
		Mil			5		6		8		10		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	4		5		6		8		10		ns
		Mil			5		6		8		10		
t_{LATCH}	Flow-Through Latch Delay	Com'l		1		2		3		4		4	ns
		Mil				2		3		4		4	
t_{RD}	Register Delay	Com'l		1		1		1		2		2	ns
		Mil				1		1		2		2	
t_{COMB}	Transparent Mode Delay[28]	Com'l		1		2		3		4		4	ns
		Mil				2		3		4		4	
t_{CH}	Clock High Time	Com'l	4		6		8		10		12.5		ns
		Mil			6		8		10		12.5		
t_{CL}	Clock Low Time	Com'l	4		6		8		10		12.5		ns
		Mil			6		8		10		12.5		

Shaded area contains preliminary information.

Notes:

22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/t_{ACF} + t_{AS1})$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander loigc is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

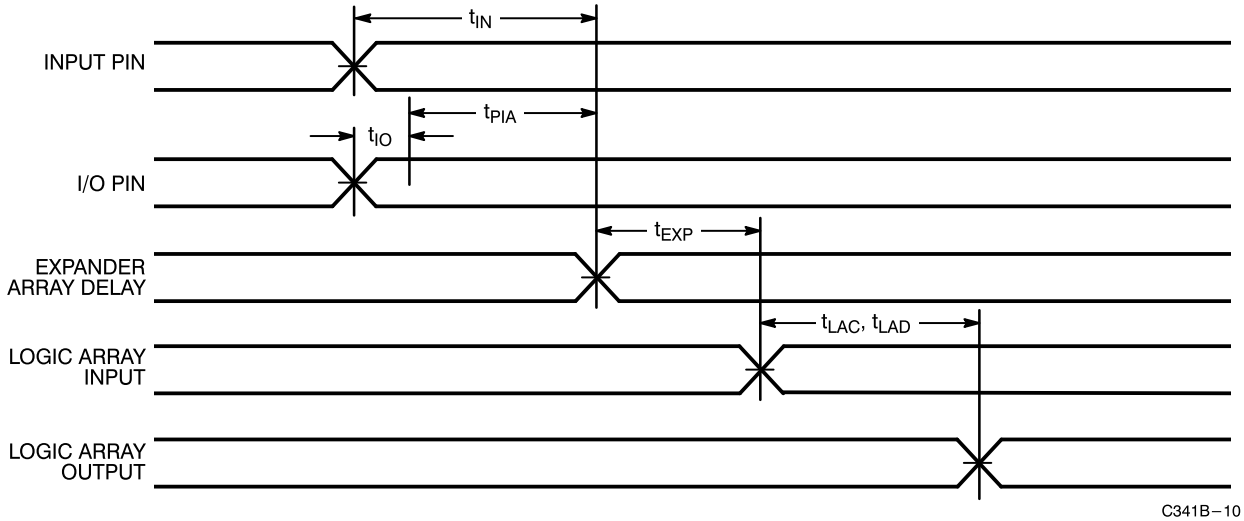
Internal Switching Characteristics Over the Operating Range[2]

Parameter	Description		7C341B−15		7C341B−20		7C341B−25		7C341B−30		7C341B−35		Unit
			Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{IC}	Asynchronous Clock Logic Delay	Com'l		6		8		14		16		18	ns
		Mil				8		14		16		18	
t_{ICS}	Synchronous Clock Delay	Com'l		0.5		0.5		2		2		3	ns
		Mil				0.5		2		2		3	
t_{FD}	Feedback Delay	Com'l		1		1		1		1		2	ns
		Mil				1		1		1		2	
t_{PRE}	Asynchronous Register Preset Time	Com'l		3		3		5		6		7	ns
		Mil				3		5		6		7	
t_{CLR}	Asynchronous Register Clear Time	Com'l		3		3		5		6		7	ns
		Mil				3		5		6		7	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	3		4		5		6		7		ns
		Mil			4		5		6		7		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	3		4		5		6		7		ns
		Mil			4		5		6		7		
t_{PIA}	Programmable Interconnect Array Delay	Com'l		10		12		14		16		20	ns
		Mil								16		20	

Shaded area contains preliminary information.

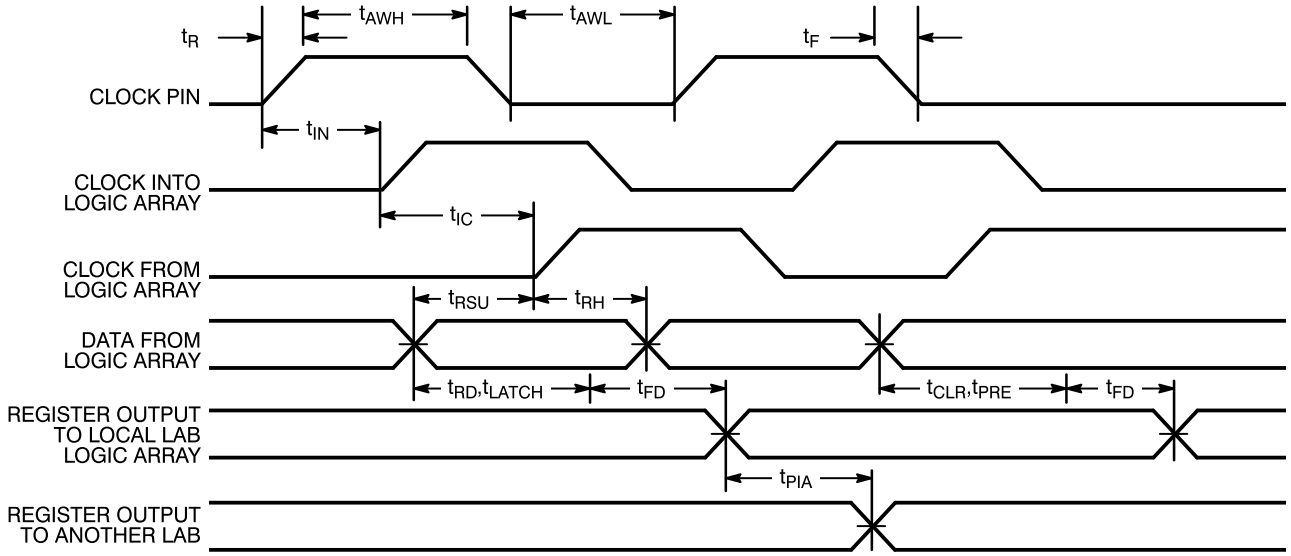
Switching Waveforms (continued)

Internal Combinatorial

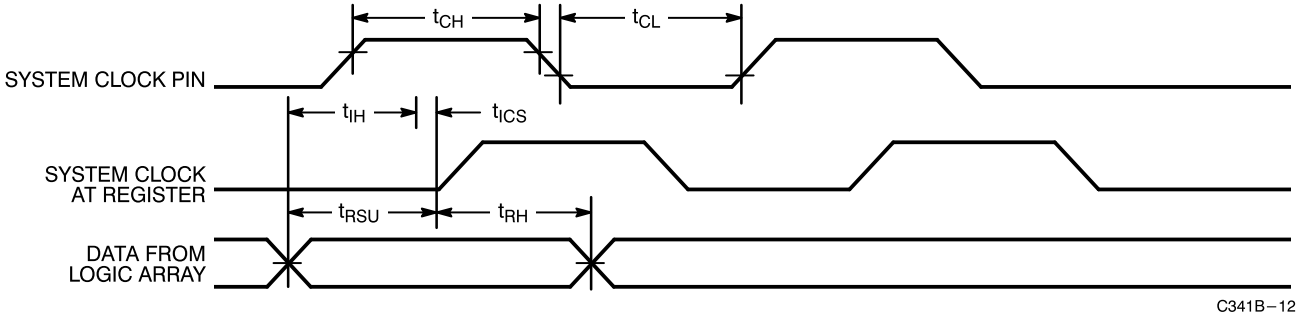


Switching Waveforms (continued)

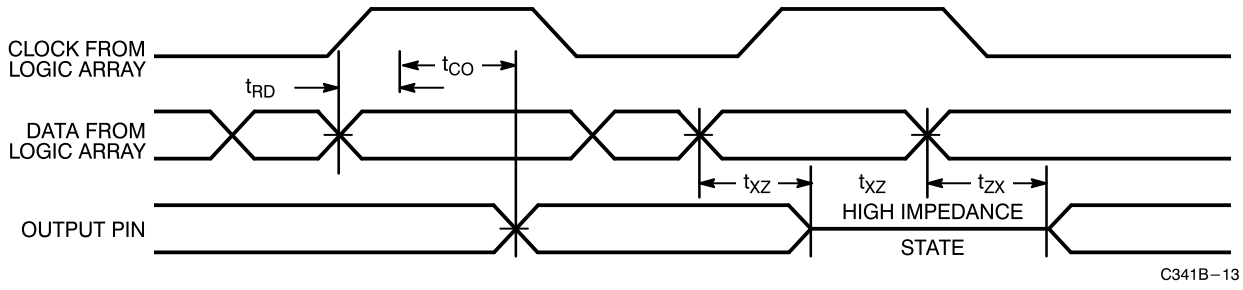
Internal Asynchronous



Internal Synchronous



Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C341B−15HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B−15JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B−15RC/RI	R84	84-Lead Windowed Pin Grid Array	
20	CY7C341B−20HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B−20JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B−20RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B−20HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B−20RMB	R84	84-Lead Windowed Pin Grid Array	
25	CY7C341B−25HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B−25JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B−25RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B−25HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B−25RMB	R84	84-Lead Windowed Pin Grid Array	
30	CY7C341B−30HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B−30JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B−30RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B−30HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B−30RMB	R84	84-Lead Windowed Pin Grid Array	
35	CY7C341B−35HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B−35JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B−35RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B−35HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B−35RMB	R84	84-Lead Windowed Pin Grid Array	

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MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

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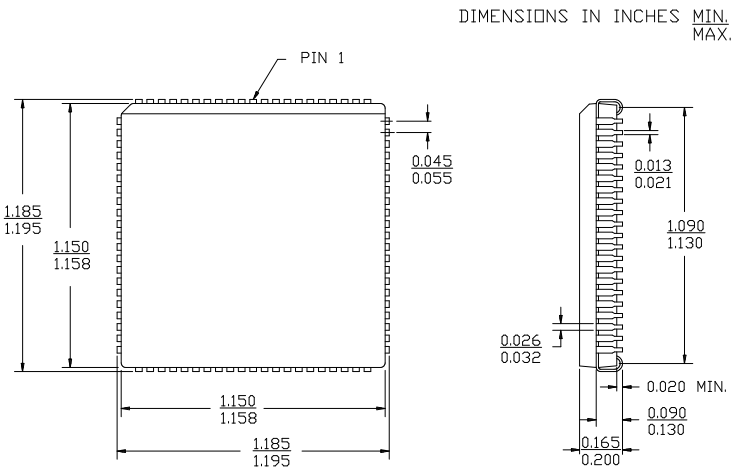
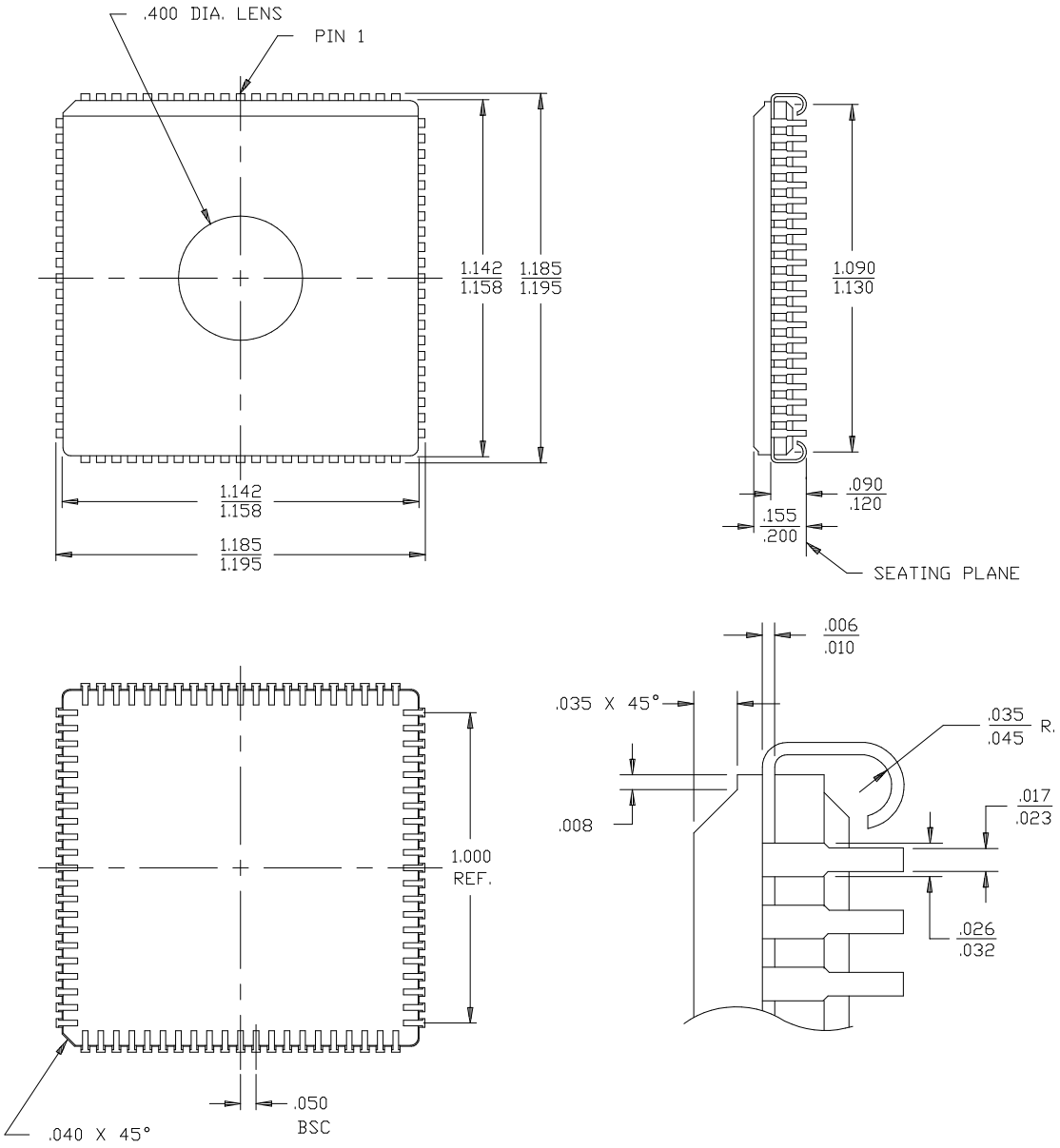
Package Diagrams

84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

84-Lead Windowed Leaded Chip Carrier H84



Package Diagrams (continued)

84-Lead Windowed Pin Grid Array R84