CY7C373

UltraLogic™ 64-Macrocell Flash CPLD

Features

- **64 macrocells in four logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **— f_{MAX} = 125 MHz**
  - **— t_{PD} = 10 ns**
  - **— t_S = 5.5 ns**
  - **— t_{CO} = 6.5 ns**
- **Electrically alterable Flash technology**
- **Available in 84-pin PLCC and 100-pin TQFP packages**
- **Pin compatible with the CY7C374**

Functional Description

The CY7C373 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C373 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

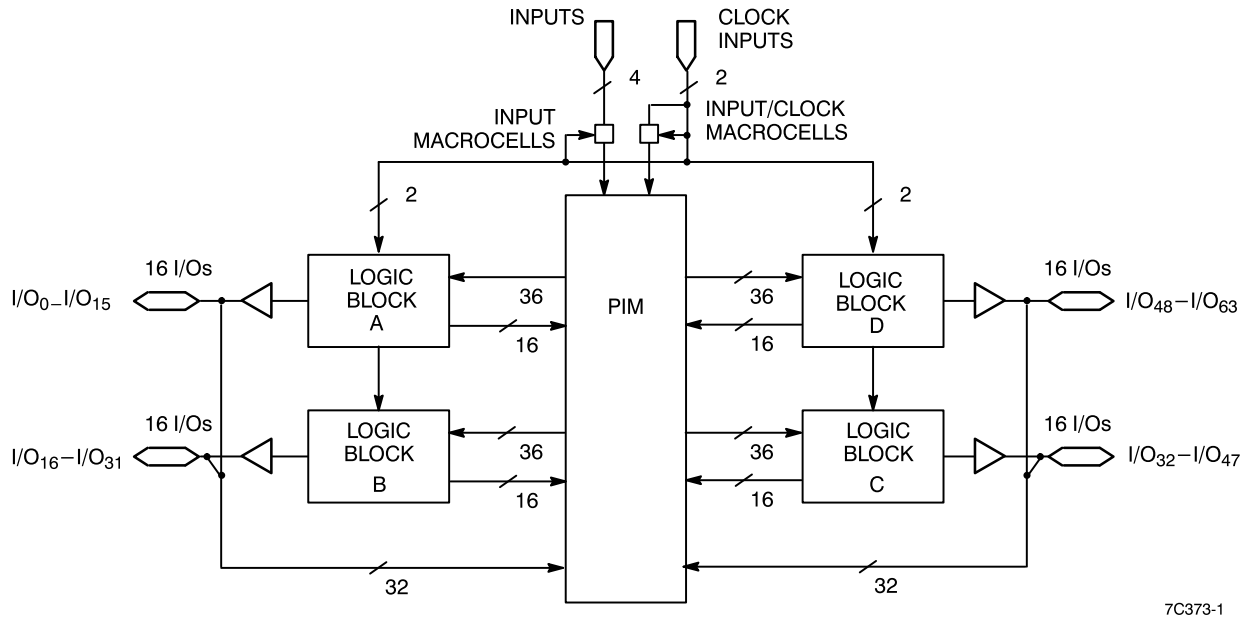
The 64 macrocells in the CY7C373 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C373 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 64 I/O pins on the CY7C373. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C373 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C373 remain the same.

Logic Block Diagram



Selection Guide

		7C373–125	7C373–100	7C373–83	7C373–66	7C373L–66
Maximum Propagation Delay (ns)		10	12	15	20	20
Minimum Set-up, t_S (ns)		5.5	6	8	10	10
Maximum Clock to Output, t_{CO} (ns)		6.5	6.5	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial	280	250	250	250	125
	Industrial			300	300	

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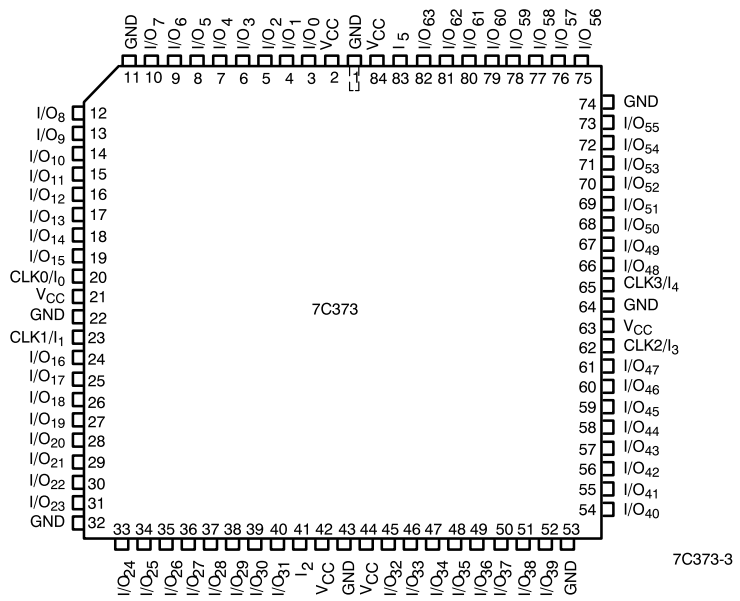
Pin Configurations

PLCC
Top View



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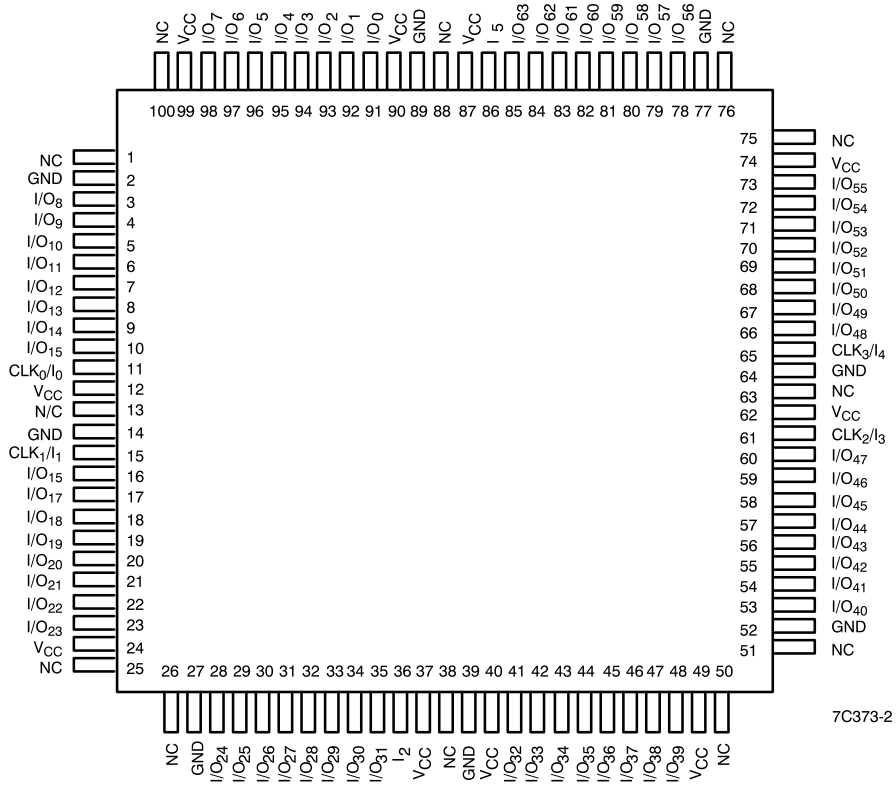
TQFP
Top View



7C373-2

Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C373 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product term resources to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that the product term allocator is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C373 has a separate I/O pin associated with it. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C373 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C373 is available from Cypress's *Warp2*™, *Warp2+*™, and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[1]		2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[2, 3]	V_{CC} = Max., V_{OUT} = 0.5V		−30	−90	mA
I_{CC}	Power Supply Current[4]	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 mHz, V_{IN} = GND, V_{CC}	Com'l		250	mA
			Com'l "L",−66		125	mA
			Com'l −125		280	mA
			Industrial		300	mA

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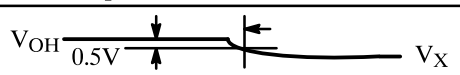
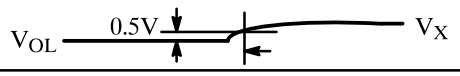
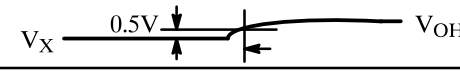
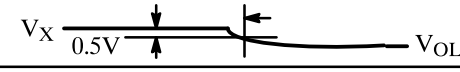
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 5.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 5.0V at f = 1 MHz	12	pF

Endurance Characteristics[3]

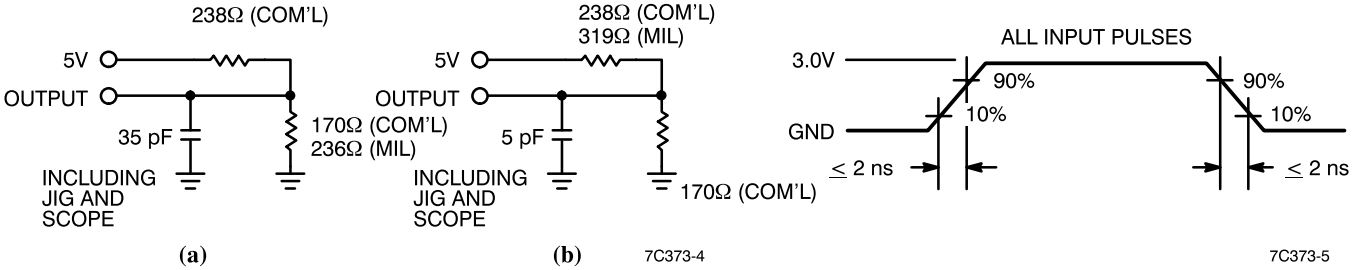
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

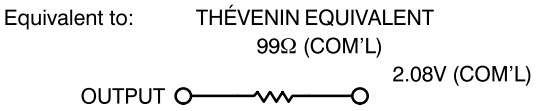
Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{thc}	

(a) Test Waveforms

Notes:
1. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. Measured with 16-bit counter programmed into each logic block.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C373−125		7C373−100		7C373−83		7C373−66 / 7C373L−66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output		10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		13		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		15		16		19		24	ns
t_{EA}	Input to Output Enable		14		16		19		24	ns
t_{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[3]	3		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[3]	3		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		16		18		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output		6.5		6.5		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5.5		6		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		14		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[3]	125		100		83		66		MHz

Shaded area contains preliminary information

Switching Characteristics Over the Operating Range[5] (continued)

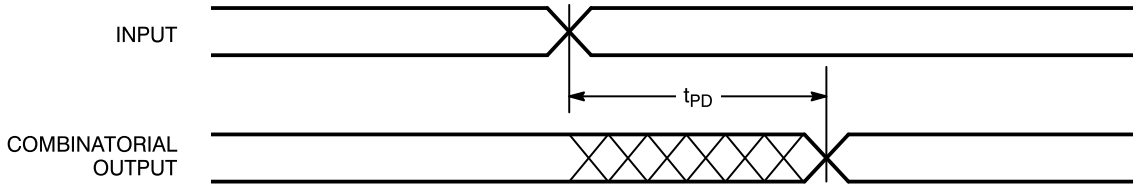
Parameter	Description	7C373−125		7C373−100		7C373−83		7C373−66 / 7C373L−66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[3]	153.8		153.8		125		100		MHz
f_{MAX3}	Maximum Frequency of (2) CY7C373s with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)[3]	83.3		80		62.5		50		MHz
$t_{OH} - t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[3, 6]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[3]	125		83.3		66.6		50.0		MHz
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[3]	10		12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[3]	12		14		17		22		ns
t_{RO}	Asynchronous Reset to Output		16		18		21		26	ns
t_{PW}	Asynchronous Preset Width[3]	10		12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[3]	12		14		17		22		ns
t_{PO}	Asynchronous Preset to Output		16		18		21		26	ns
t_{POR}	Power-On Reset[3]		1		1		1		1	µs

Shaded area contains preliminary information.

Note:
5. All AC parameters are measured with 16 outputs switching.
6. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C373. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

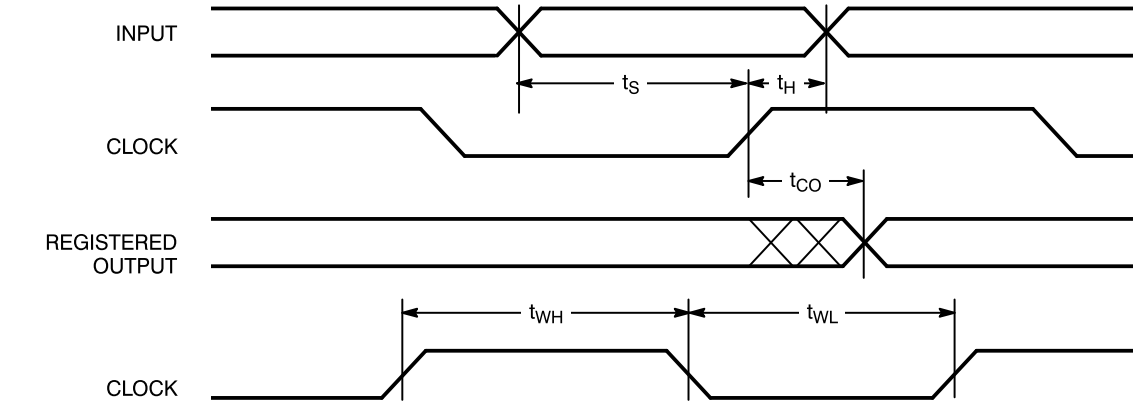
Switching Waveforms

Combinatorial Output



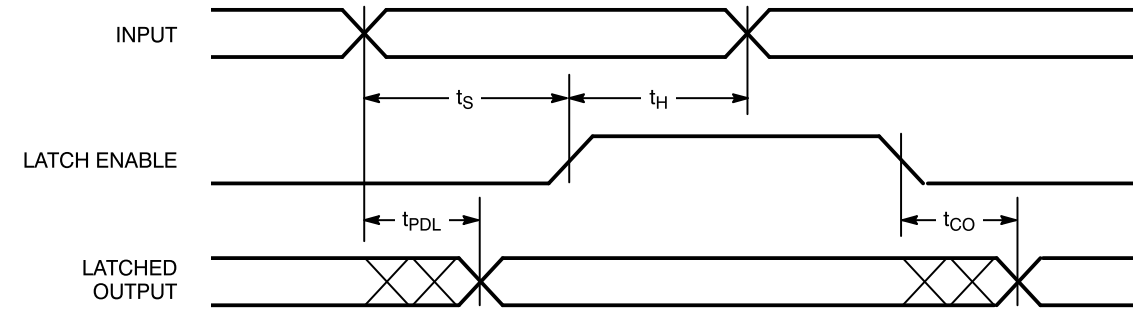
7C373-6

Registered Output



7C373-7

Latched Output



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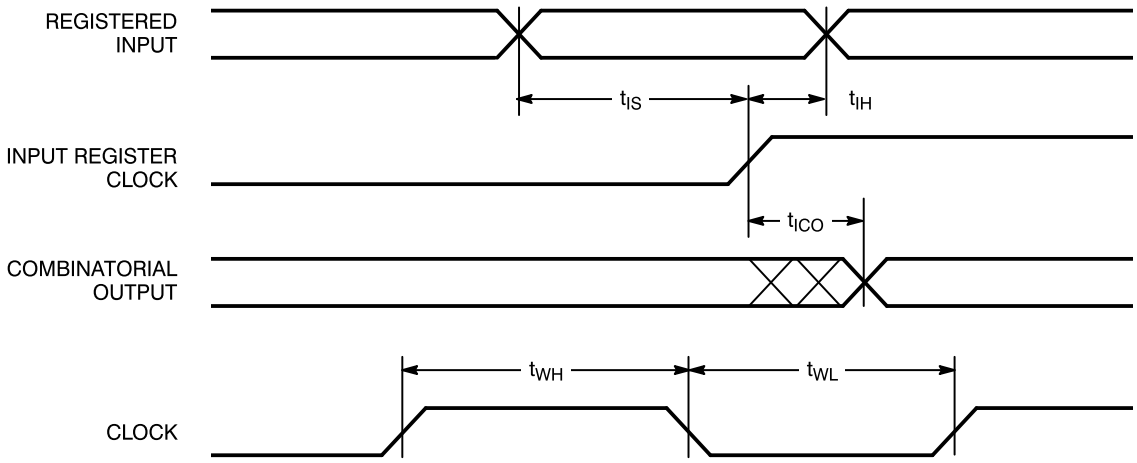
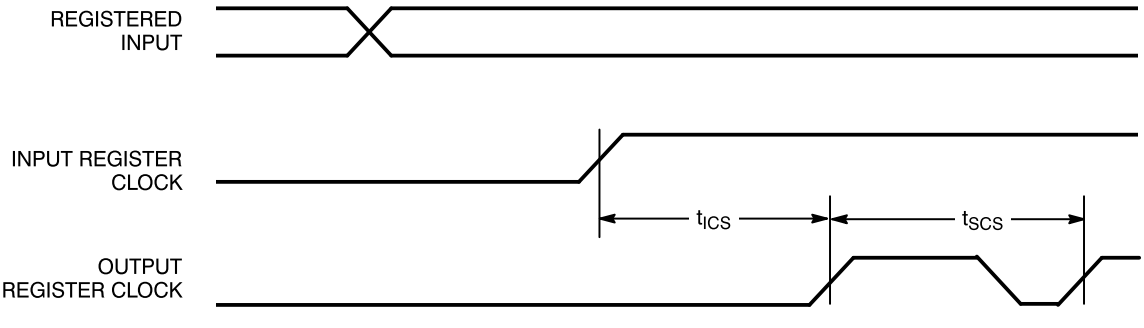
Switching Waveforms (continued)

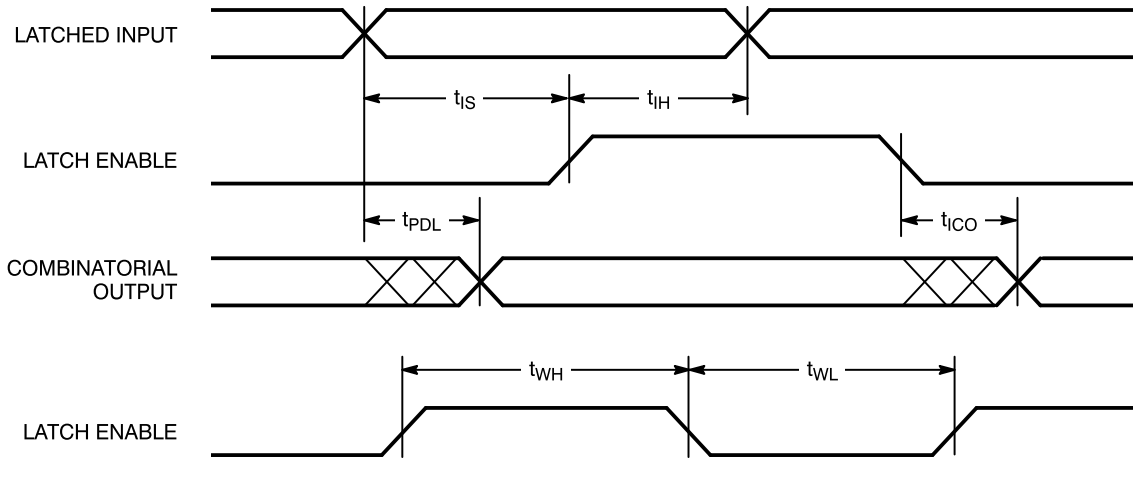
Registered Input



Clock to Clock

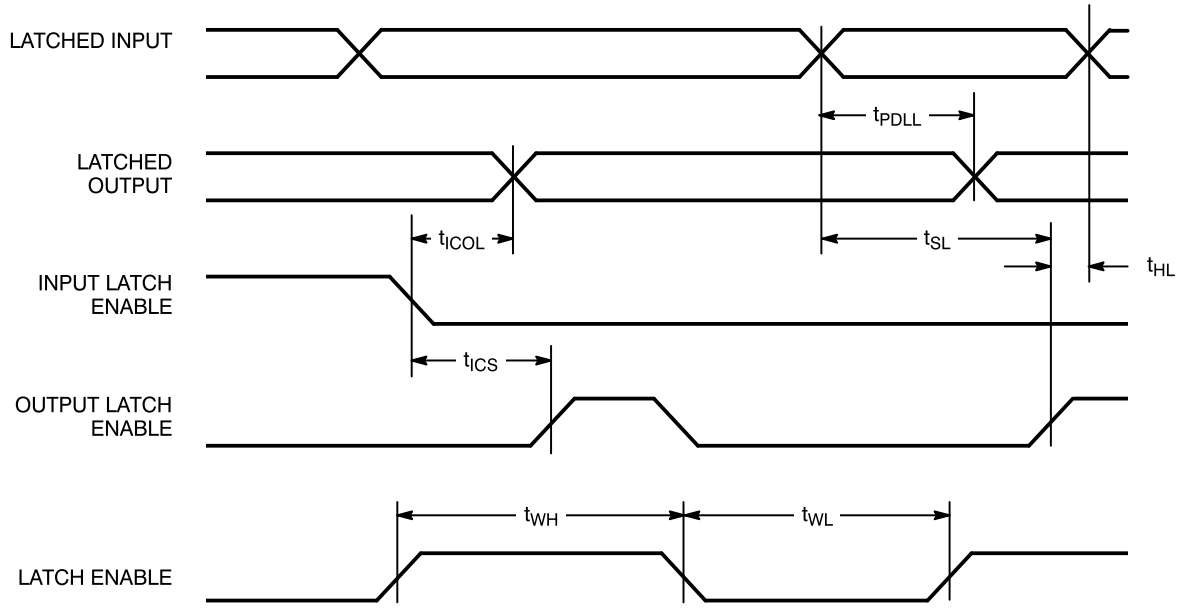


Latched Input

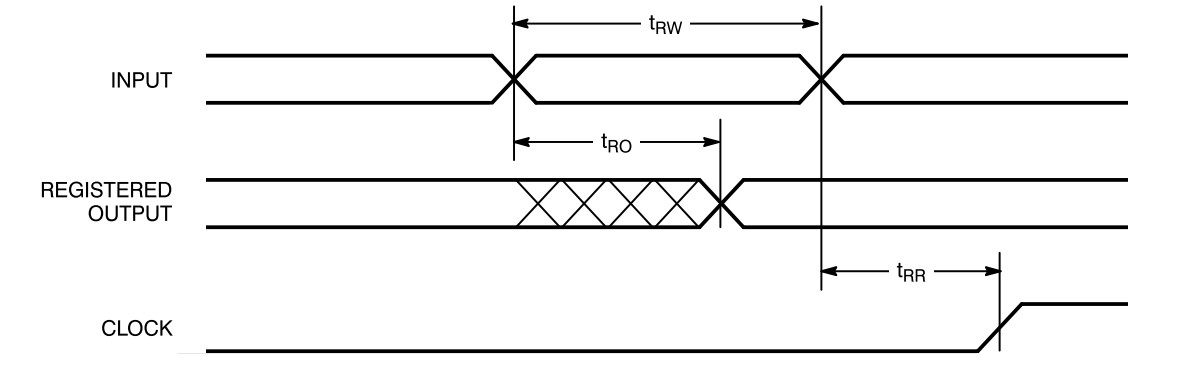


Switching Waveforms (continued)

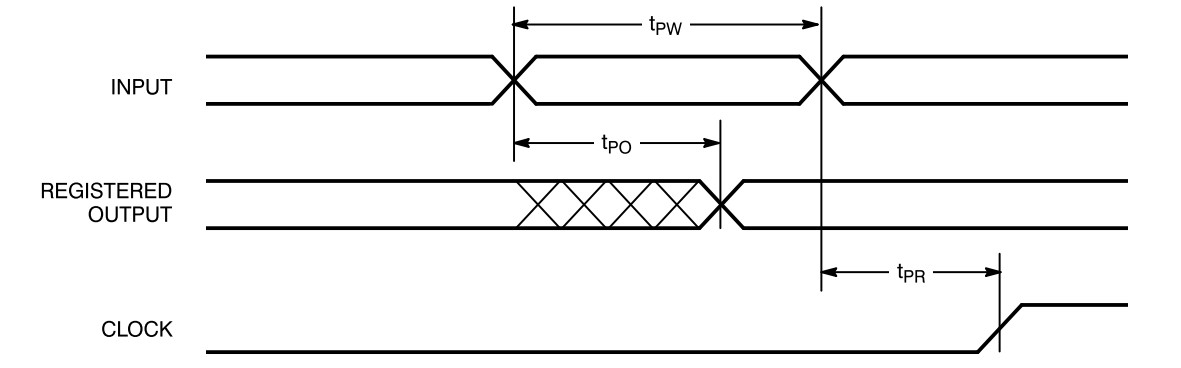
Latched Input and Output



Asynchronous Reset

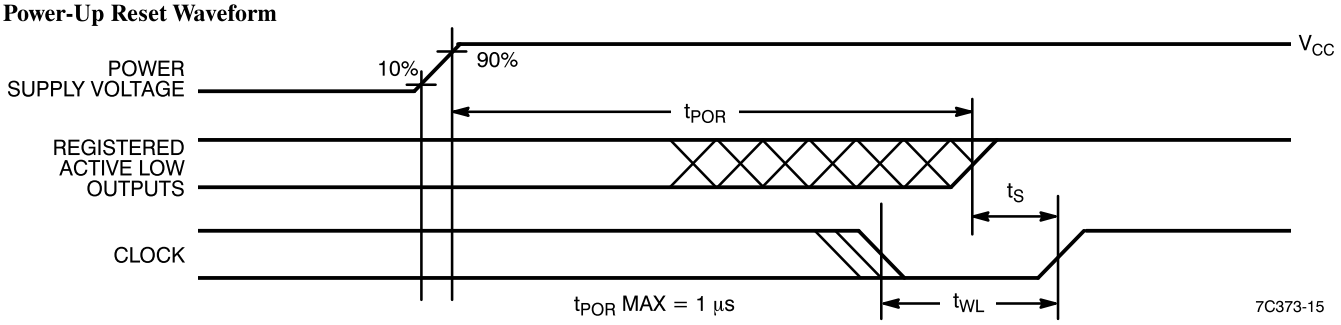


Asynchronous Preset

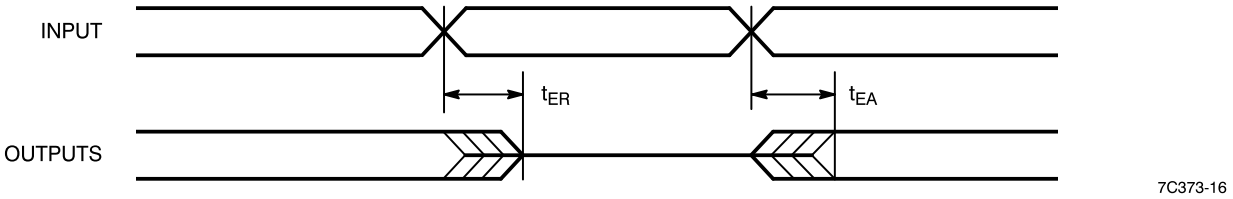


Switching Waveforms (continued)

Power-Up Reset Waveform



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Type	Package Type	Operating Range
125	CY7C373−125AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373−125JC	J83	84-Lead Plastic Leaded Chip Carrier	
100	CY7C373−100AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373−100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C373−83AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373−83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373−83AI	A100	100-Pin Thin Quad Flatpack	Industrial
	CY7C373−83JI	J83	84-Lead Plastic Leaded Chip Carrier	
66	CY7C373−66AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373−66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373−66AI	A100	100-Pin Thin Quad Flatpack	Industrial
	CY7C373−66JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373L−66JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial

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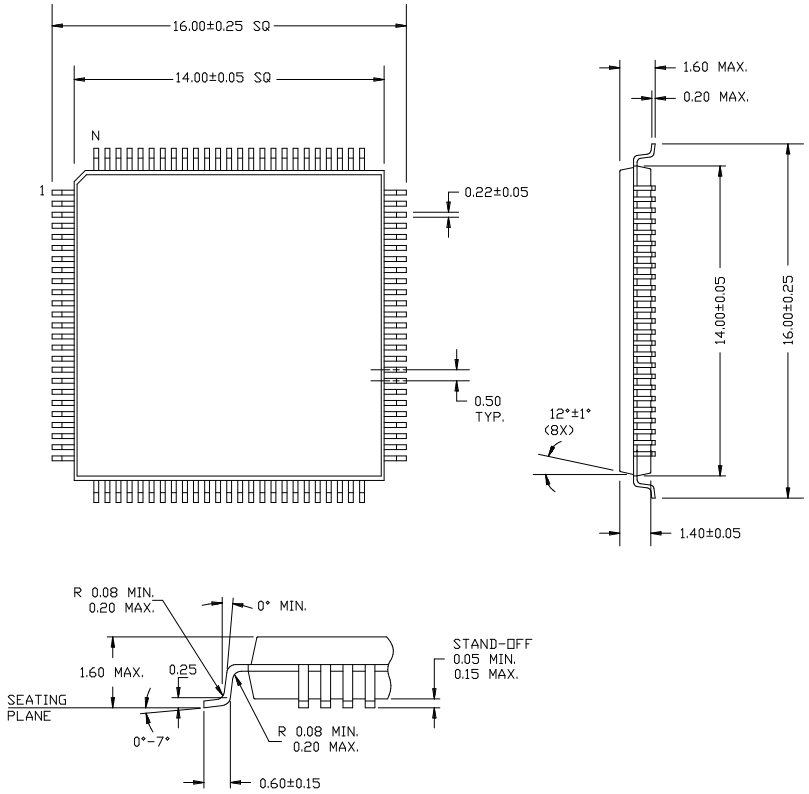
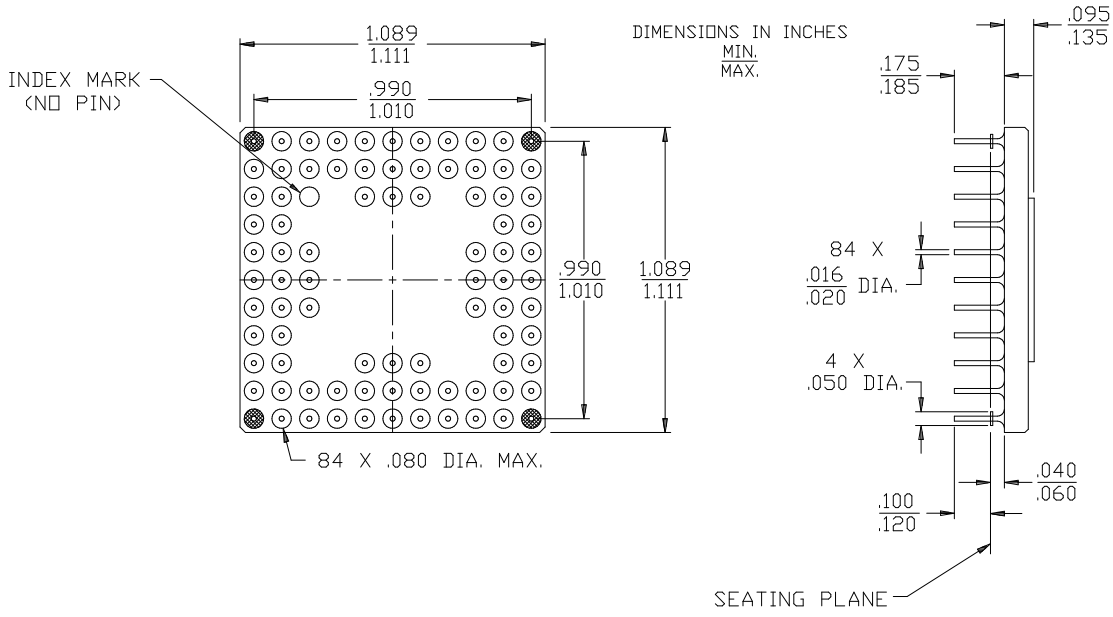
Package Diagrams

100-Pin Thin Quad Flat Pack A100

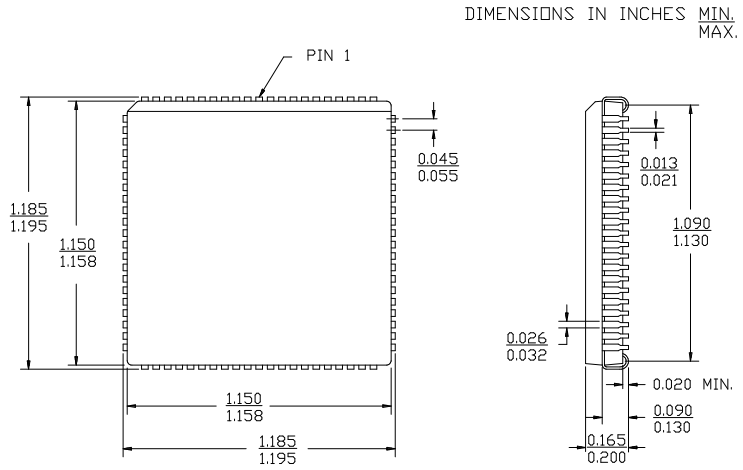


Package Diagrams (continued)

84-Pin Grid Array (Cavity Up) G84



84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84