7C381A: Monday, September 20, 1993
Revision: October 9, 1995

CY7C381P
CY7C382P

UltraLogic™ Very High Speed 1K Gate CMOS FPGA

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 150 MHz**
  - **Chip-to-chip operating frequencies up to 110 MHz**
  - **Input + logic cell + output delays under 6 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **8 x 12 array of 96 logic cells provides 3,000 total available gates**
  - **1,000 typically usable "gate array" gates in 44- and 68-pin PLCC, 69-pin CPGA, 100-pin TQFP packages**
- **Fully PCI compliant inputs and outputs for commercial and industrial temperature ranges**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 150 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 20 mA**
- **Flexible logic cell architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (1.7 ns typical)**
- **Powerful design tools—*Warp3*™**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Extensive 3rd party tool support**
  - **See Development Systems section**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **No hand routing required**
- **32 (CY7C381P) to 56 (CY7C382P) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
  - **Clock skew <0.5 ns**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
- **0.65µ CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**
- **68-pin PLCC is compatible with EPLD 1800 and LCA 2064 industry-standard pinouts**
- **100-pin TQFP is pinout compatible with 2K (C47C384P) and 4K (CY7C385P) devices**
- **68-pin PLCC is pinout compatible with 2K (CY7C383P) devices**

Functional Description

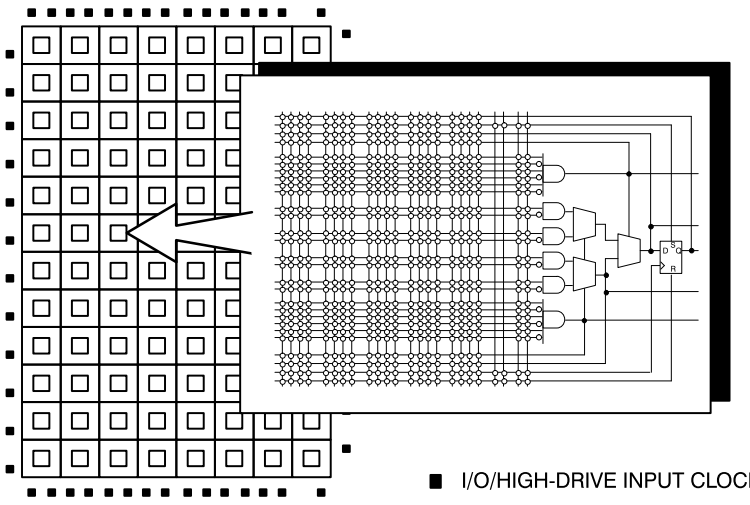
The CY7C381P and CY7C382P are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 96 logic cell field-programmable gate array (FPGA) offers 1,000 typically usable "gate array" gates. This is equivalent to 3,000 EPLD or LCA gates. The CY7C381P is available in a 44-pin PLCC package. The CY7C382P is available in a 68-pin PLCC, 69-pin CPGA and a 100-pin TQFP packages.

The low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input delays under 1.5 ns and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C381P and CY7C382P using Cypress *Warp3* software or one of several third-party tools. See the Development Systems section of the *Programming Logic Databook* for more tools information *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C381P and CY7C382P feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram

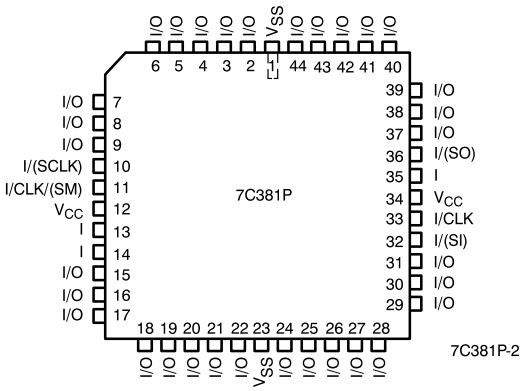


44, 68, 69, or 100 PINS, INCLUDING 56 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS

CY7C381P
CY7C382P

Pin Configurations

PLCC
Top View



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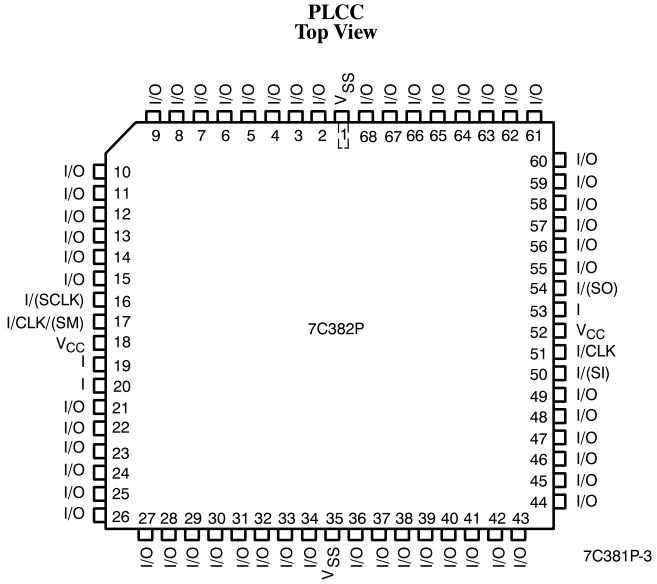
PLCC
Top View



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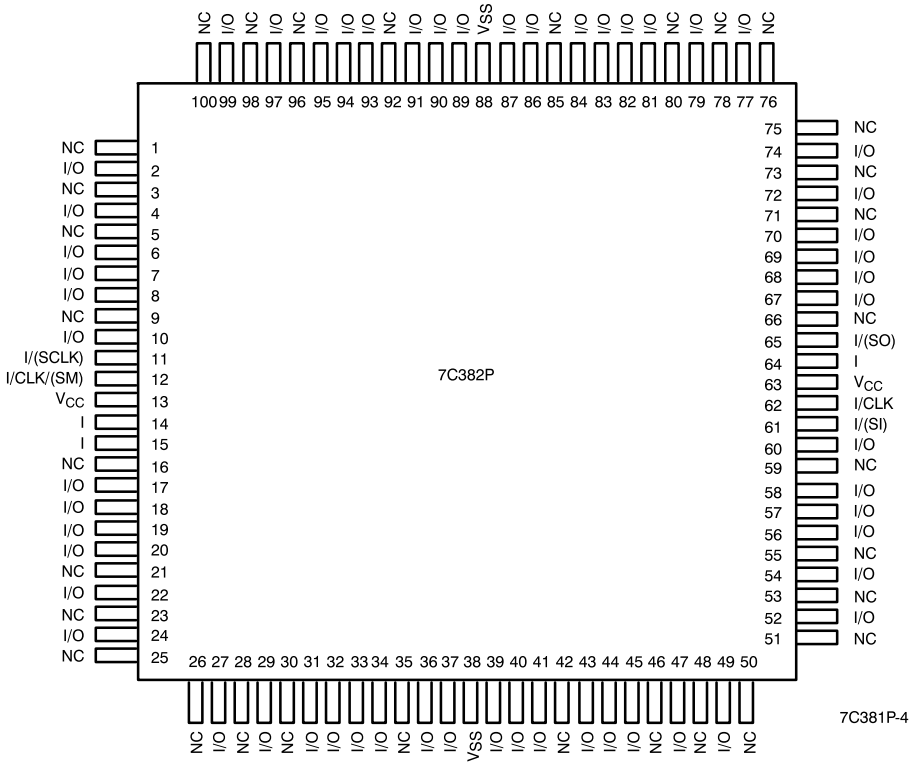
TQFP
Top View



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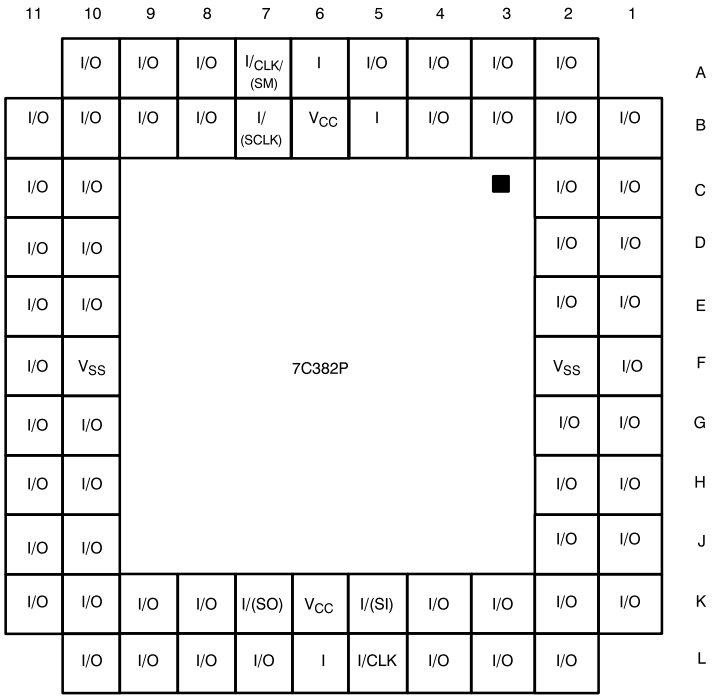
Pin Configurations (continued)

CPGA
Bottom View



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... − 65°C to +150°C
Plastic ..... −40°C to +125°C
Lead Temperature ..... 300°C
Supply Voltage ..... − 0.5V to +7.0V
Input Voltage ..... − 0.5V to V_{CC} +0.5V
ESD Pad Protection ..... ±2000 V
DC Input Voltage ..... −0.5V to 7.0V
DC Input Current ..... ±20 mA
Latch-Up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−X	0.39	3.00	0.4	2.75	0.46	2.55
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.56	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	3.7		V
		I_{OH} = −20 mA	2.4		V
		I_{OH} = −10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 20 mA		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OZ}	Output Leakage Current—Three-State	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OS}	Output Short Circuit Current[1]	V_{OUT} = V_{SS}	−10	− 80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC1}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[2]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
1. Only one output at a time. Duration should not exceed 30 seconds.
2. C_I = 20 pF max. on I/(SI).

Switching Characteristics (At V_{CC}=5 V, T_A=25°C , K=1.00)

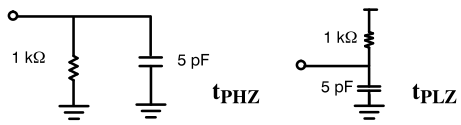
Parameter	Description	Propagation Delays[3] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[4]	1.7	2.1	2.6	3.0	4.8	ns
t_{SU}	Set-Up Time[4]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.3	4.2	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.1	2.6	3.0	4.8	ns
t_{RESET}	Reset Delay	1.5	1.8	2.2	2.5	3.9	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[3] 1	2	3	4	6	8	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.1	2.2	2.3	2.4	2.6	2.9	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	2.1	2.2	2.3	2.5	2.8	3.1	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.8	2.2	2.6	3.4	4.2	ns
t_{GCK}	Clock Buffer Delay[5]	2.7	2.7	2.8	2.9	3.0		ns
t_{GCKHI}	Clock Buffer Min. HIGH[5]	2.0	2.0	2.0	2.0	2.0		ns
t_{GCKLO}	Clock Buffer Min. LOW[5]	2.0	2.0	2.0	2.0	2.0		ns

Parameter	Description	Propagation Delays[3] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[6]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[6]	3.3					ns

Notes:

3. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
4. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC380 logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
5. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
6. The following loads are used for t_{PXZ}:

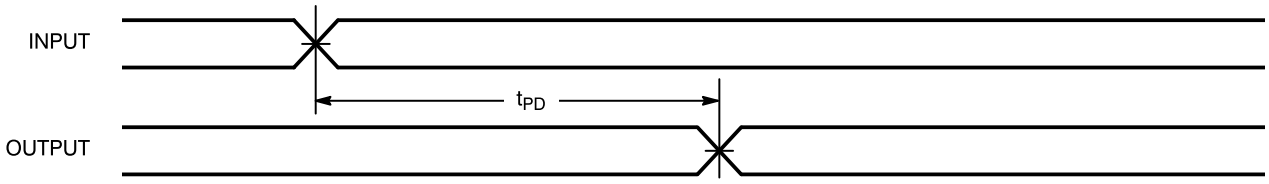


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[3] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	4.0	4.9				ns
		2		3.5	5.0			ns
		3			4.0	4.8	5.6	ns
		4				4.1	4.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	4.2	5.1				ns
		2		3.7	5.2			ns
		3			4.2	5.0	5.8	ns
		4				4.3	5.0	ns

Switching Waveforms

Combinatorial Delay



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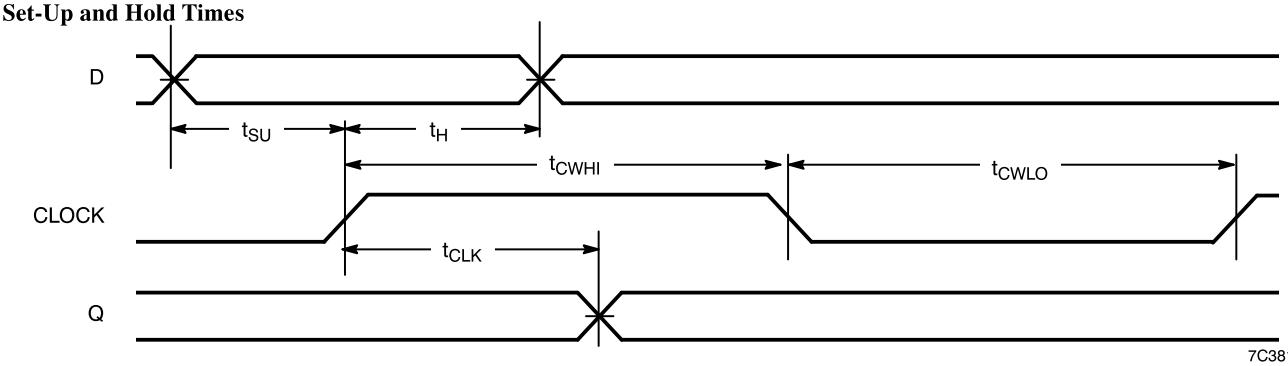
Set-Up and Hold Times



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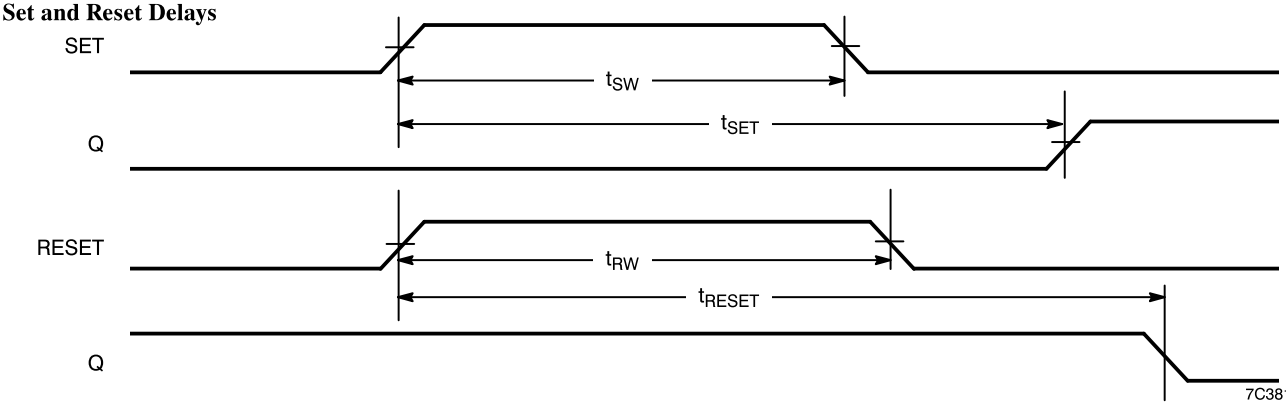
Set and Reset Delays



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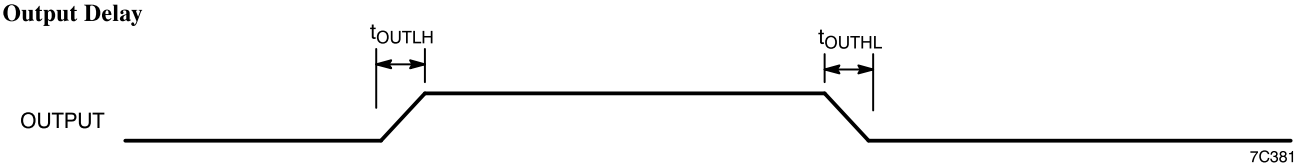
Output Delay



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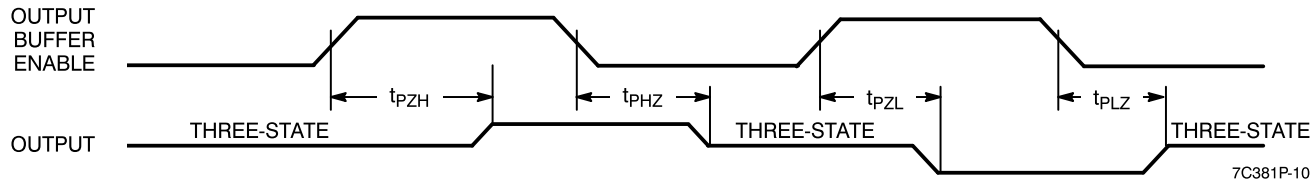
Switching Waveforms (continued)

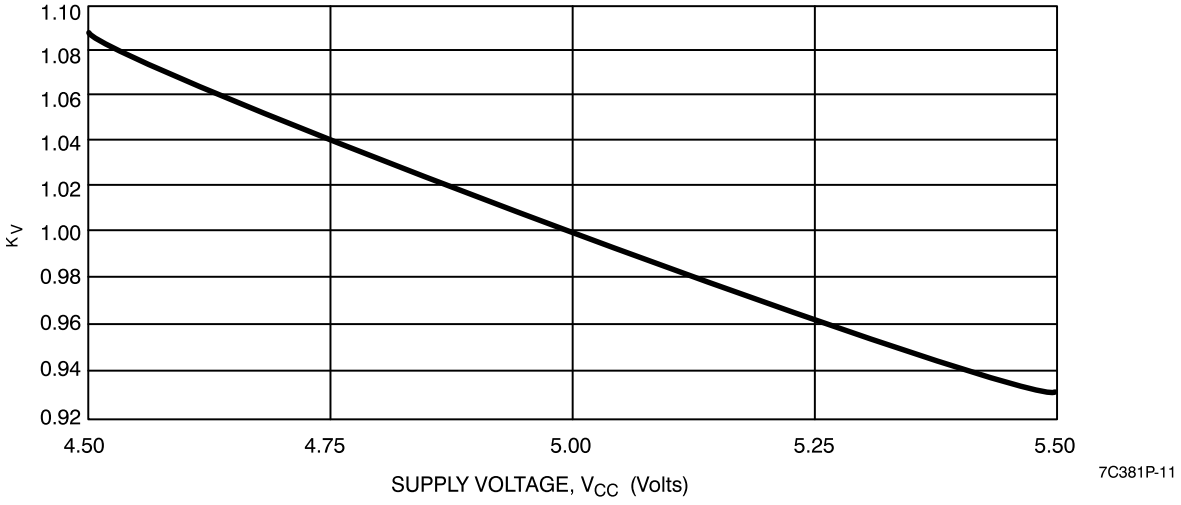
Three-State Delay



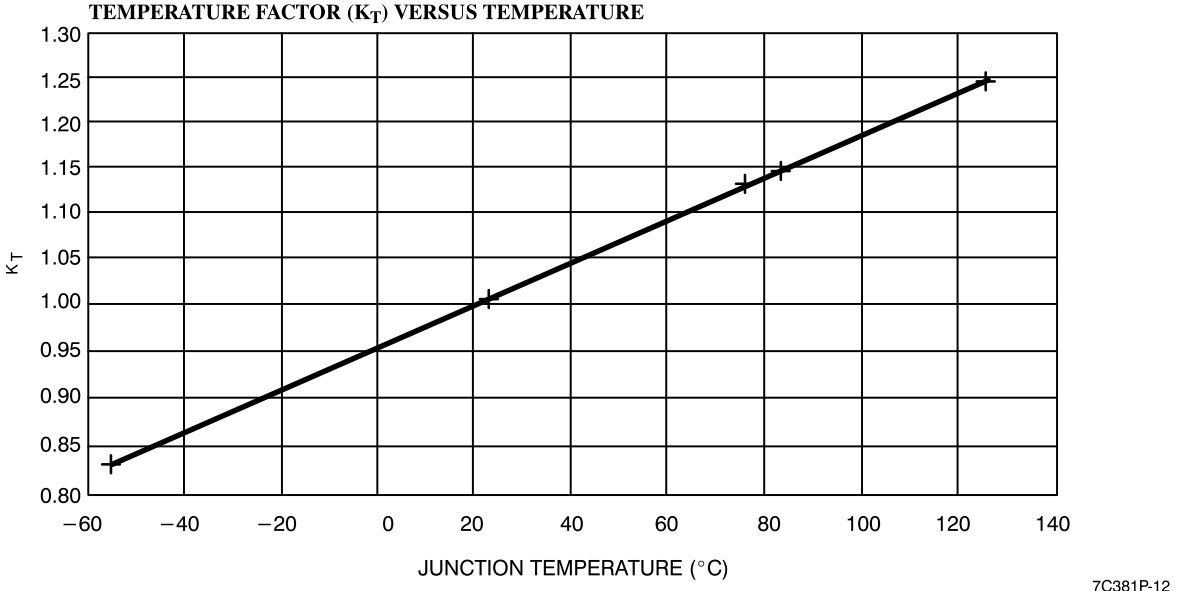
Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})

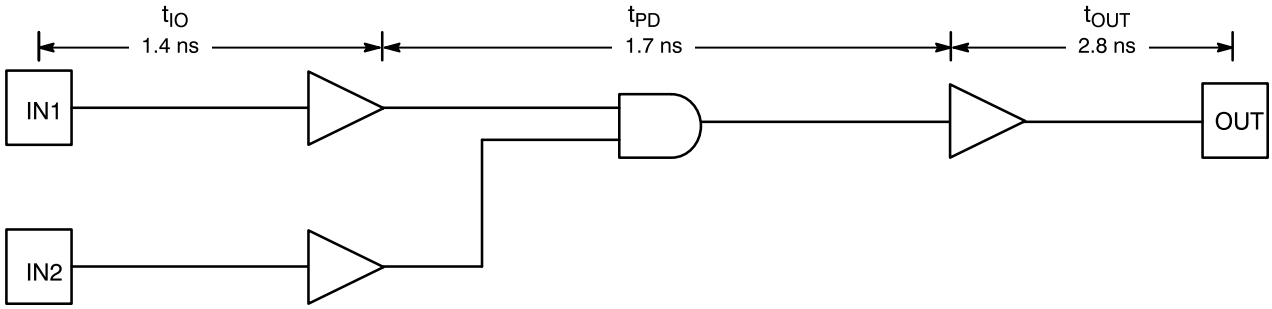


TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



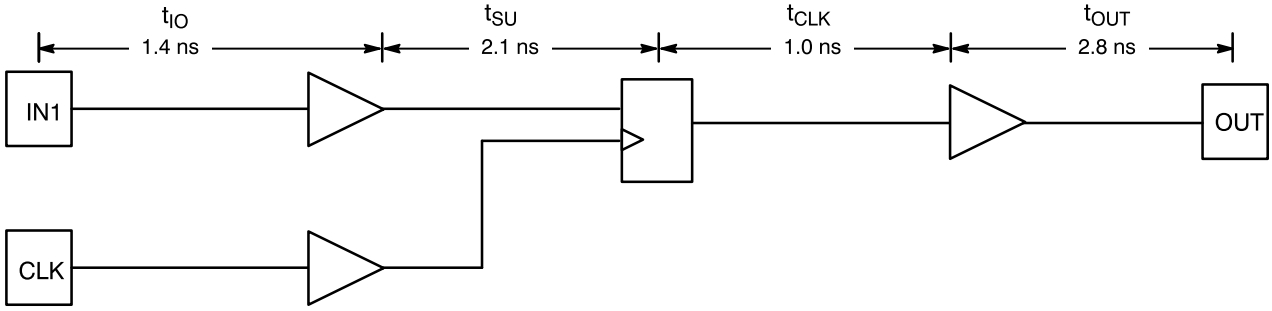
*THETA JA = 45 °C/WATT FOR PLCC

Combinatorial Delay Example (Load = 30 pF, K=1, Fanout=1)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

Sequential Delay Example (Load = 30 pF, K=1, Fanout=1)



INPUT DELAY + REG SET-UP + CLOCK TO Q DELAY + OUTPUT DELAY = 7.3 ns

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C381P−2JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381P−2JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
1	CY7C381P−1JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381P−1JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
0	CY7C381P−0JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381P−0JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
X	CY7C381P−XJC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381P−XJI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C382P−2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382P−2JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382P−2JI	J81	68-Lead Plastic Leaded Chip Carrier	
1	CY7C382P−1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382P−1JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382P−1JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−1GMB	G69	69-Pin Grid Array (Cavity Down)	Military
0	CY7C382P−0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382P−0JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382P−0JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−0GMB	G69	69-Pin Grid Array (Cavity Down)	Military
X	CY7C382P−XAC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382P−XJC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−XAI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382P−XJI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382P−XGMB	G69	69-Pin Grid Array (Cavity Down)	Military

Shaded area contains preliminary information

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_I	1, 2, 3

Switching Characteristics

Parameter	Subgroups
Delay Factor (K)	7, 8, 9, 10, 11

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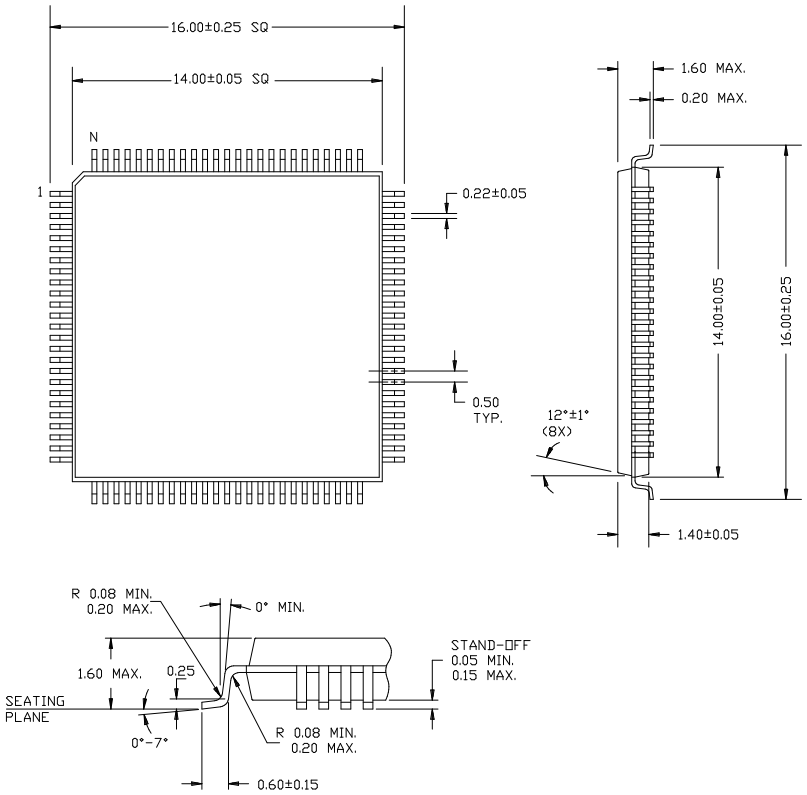
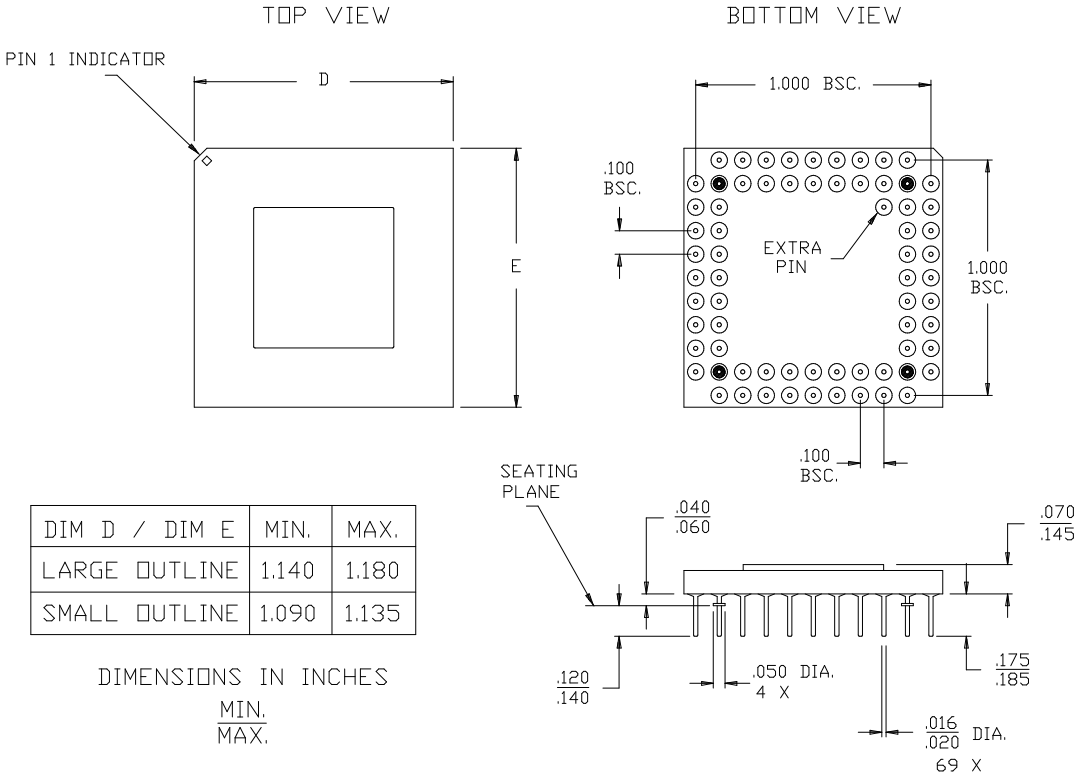
Package Diagrams

100-Pin Thin Quad Flat Pack A100



Package Diagrams (continued)

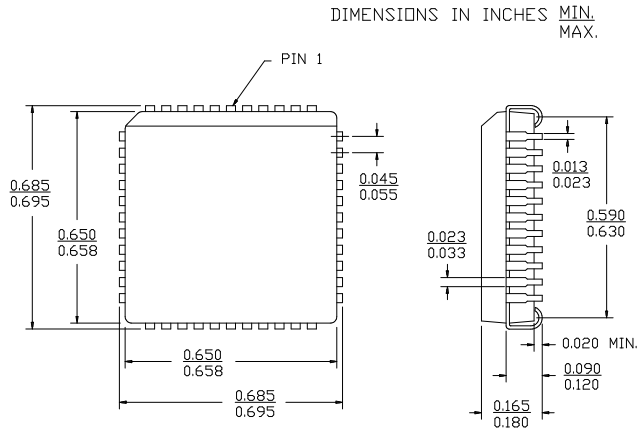
69-Pin Grid Array (Cavity Up) G69



DIM D / DIM E	MIN.	MAX.
LARGE OUTLINE	1.140	1.180
SMALL OUTLINE	1.090	1.135

DIMENSIONS IN INCHES
MIN.
MAX.

44-Lead Plastic Leaded Chip Carrier J67



Package Diagrams (continued)

68-Lead Plastic Leaded Chip Carrier J81