Introduction to Cypress PLDs

Cypress PLD Family Features

Cypress Semiconductor's PLD family offers the user a wide range of programmable logic solutions that incorporate leading-edge circuit design techniques as well as diverse process technology capabilities. This allows Cypress PLD users to select PLDs that best suit the needs of their particular high-performance system, regardless of whether speed, power consumption, density, or device flexibility are the critical requirements imposed by the system.

Cypress offers enhanced-performance industry-standard 20- and 24-pin device architectures as well as proprietary 28-pin application-tailored architectures. The range of technologies offered includes leading-edge 0.65-micron CMOS EPROM for high speed, low power, and high density, 0.65-micron FLASH technology for high speed, low power and electrical alterability.

The reprogrammable memory cells used by Cypress serve the same purpose as the fuse used in most bipolar PLD devices. Before programming, the AND gates or product terms are connected via the reprogrammable memory cell to both the true and complement inputs. When the reprogrammable memory cell is programmed, the inputs from a gate or product term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or product term. This is similar to "blowing" the fuses of BiCMOS or bipolar fusible devices, which disconnects the input gate from the product term. Selective programming of each of these reprogrammable memory cells enables the specific logic function to be implemented by the user.

The programmability of Cypress's PLDs allows the users to customize every device in a number of ways to implement their unique logic requirements. Using PLDs in place of SSI or MSI components results in more effective utilization of board space, reduced cost and increased reliability. The flexibility afforded by these PLDs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The PLD family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output, and product terms to the desired application.

PLD Notation

To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In part (a), an "×" represents an unprogrammed EPROM cell or intact fuse link that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in part (b), which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in part (c).

PLD Circuit Configurations

Cypress PLDs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows designers to select PLDs that best fit their applications. An example of some of the configurations that are available are listed below.

Programmable I/O

Figure 2 illustrates the programmable I/O offered in the Cypress PLD family that allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PLD as an input to the array. This programmable I/O feature allows the PLD to drive the output pin when the three-state output is enabled or, when the three-state output is disabled, the I/O pin can be used as an input to the array.

Registered Outputs with Feedback

Figure 3 illustrates the registered outputs offered on a number of the Cypress PLDs which allow any of these circuits to function as a
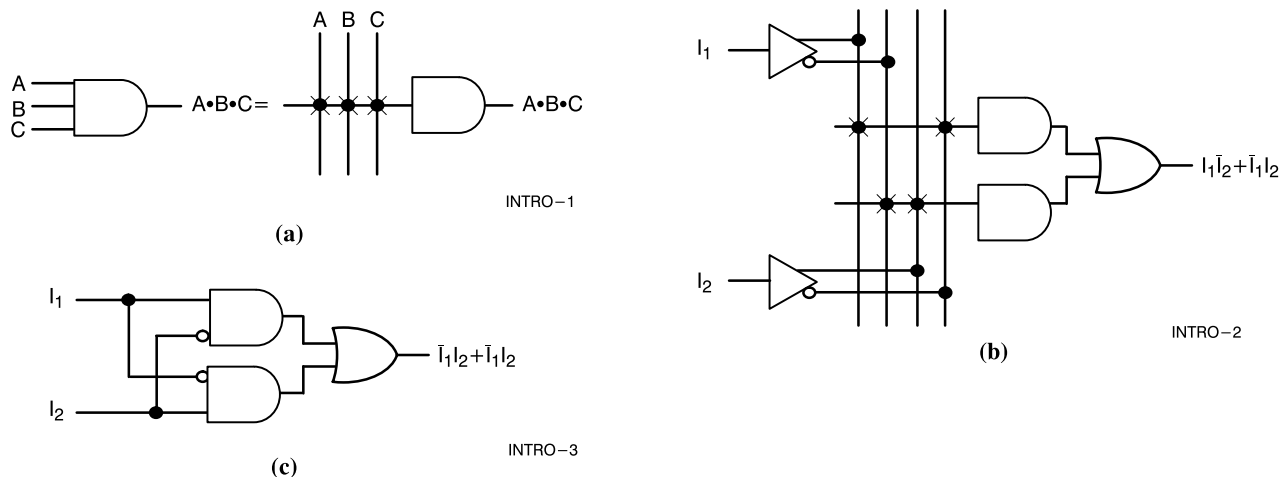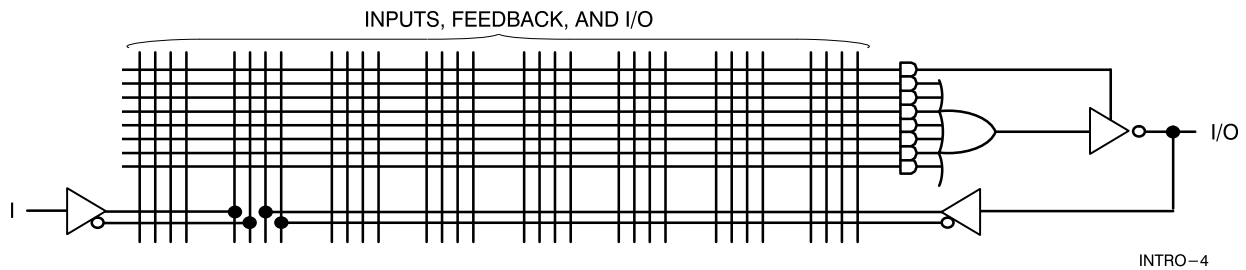

Figure 1. Logic Diagram Conventions

Introduction to Cypress PLDs

INPUTS, FEEDBACK, AND I/O

INTRO−4

Figure 2. Programmable I/O

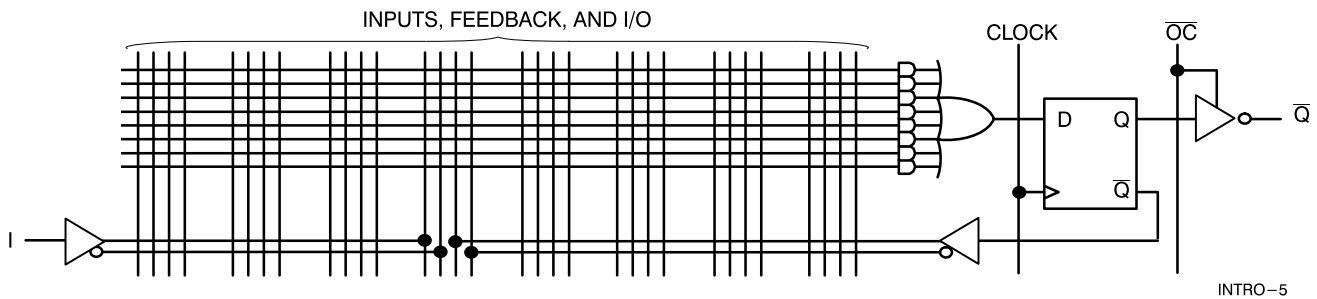INPUTS, FEEDBACK, AND I/O   CLOCK $\overline{OC}$

INTRO−5

Figure 3. Registered Outputs with Feedback

state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PLD to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift, and branch.

Programmable Macrocell

The programmable macrocell, illustrated in *Figure 4*, provides the capability of defining the architecture of each output individually. Each of the potential outputs may be specified to be "registered" or "combinatorial." Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the outputs to be reconfigured as inputs on an individual basis or alternately used as a bidirectional I/O controlled by the programmable array (see *Figure 5*).

Buried Register Feedback

The CY7C331 and CY7C335 PLDs provide registers that may be "buried" or "hidden" by electing feedback of the register output. These buried registers, which are useful in state machines, may be implemented without sacrificing the use of the associated device pin as an input. In previous PLDs, when the feedback path was activated, the input pin-path to the logic array was blocked. The proprietary CY7C335 reprogrammable synchronous state machine macrocell illustrates the shared input multiplexer, which provides an alternative input path for the I/O pin associated with a buried macrocell register (*Figure 6*). Each pair of macrocells shares an input multiplexer, and as long as alternate macrocells are buried, up to six of the twelve output registers can be buried without the loss

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of any I/O pins as inputs. The CY7C335 also contains four dedicated hidden macrocells with no external output that are used as additional state registers for creating high-performance state machines (*Figure 7*).

Asynchronous Register Control

Cypress also offers PLDs that may be used in asynchronous systems in which register clock, set, and reset are controlled by the outputs of the product term array. The clock signal is created by the processing of external inputs and/or internal feedback by the logic of the product term array, which is then routed to the register clock. The register set and reset are similarly controlled by product term outputs and can be triggered at any time independent of the register clock in response to external and/or feedback inputs processed by the logic array. The proprietary CY7C331 Asynchronous Registered PLD, for which the I/O macrocell is illustrated in *Figure 8*, is an example of such a device. The register clock, set, and reset functions of the CY7C331 are all controlled by product terms and are dependent only on input signal timing and combinatorial delay through the device logic array to enable their respective functions.

Input Register Cell

Other Cypress PLDs provide input register cells to capture short duration inputs that would not otherwise be present at the inputs long enough to allow the device to respond. The proprietary CY7C335 Reprogrammable Synchronous State Machine provides these input register cells (*Figure 9*). The clock for the input register may be provided from one of two external clock input pins selectable by a configuration bit, C4, dedicated for this purpose for each input register. This choice of input register clock allows signals to be captured and processed from two independent system sources, each controlled by its own independent clock. These input register cells are provided within I/O macrocells, as well as for dedicated input pins.
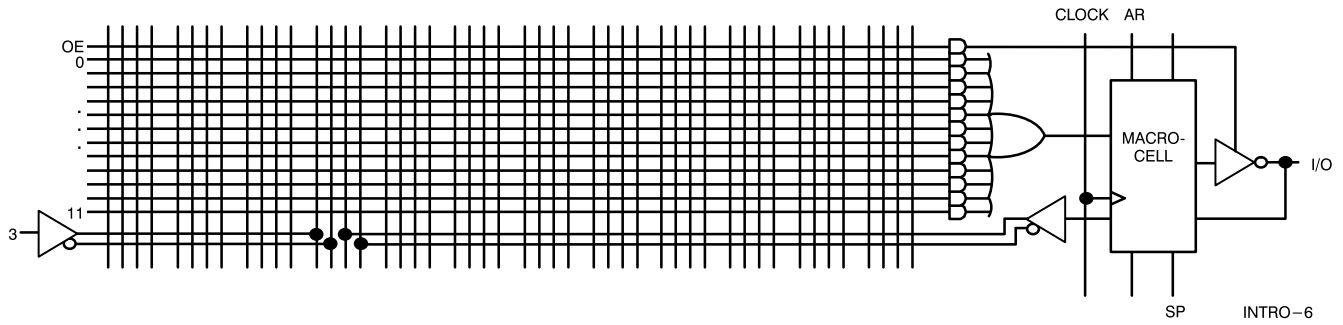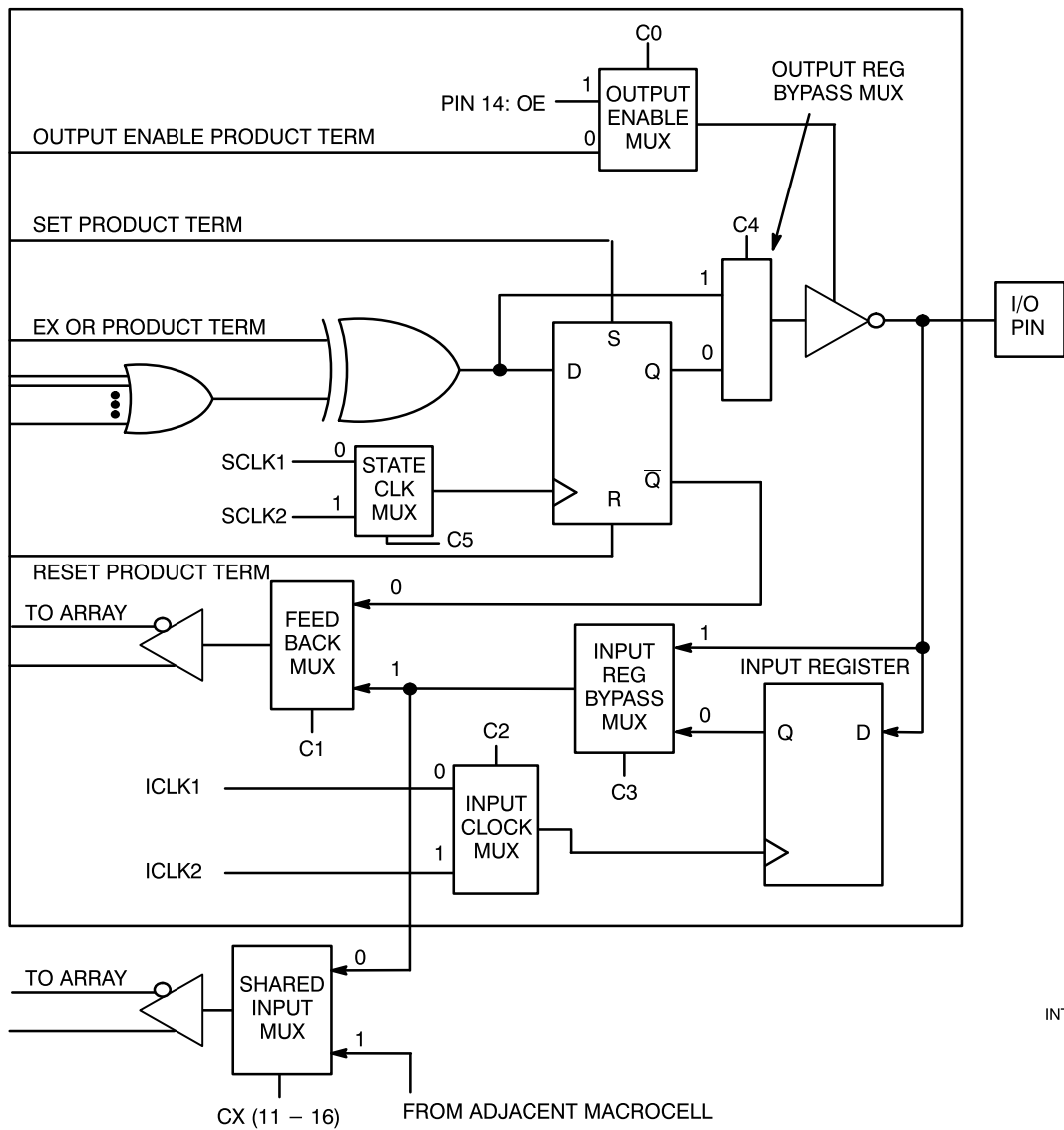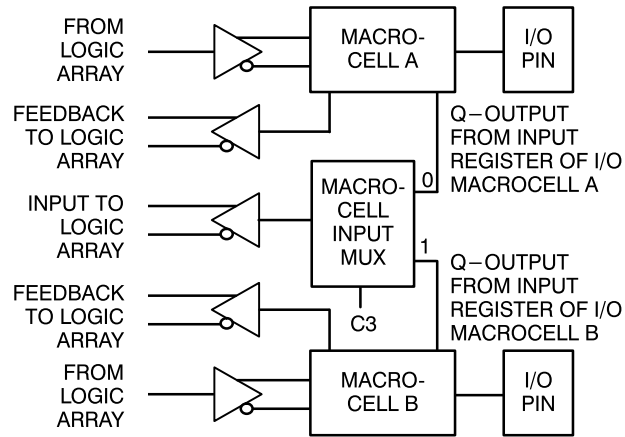
Introduction to Cypress PLDs

Figure 4. Programmable Macrocell

Figure 5. CY7C335 I/O Macrocell

3

Introduction to Cypress PLDs

INTRO−8

Figure 6. CY7C335 I/O Macrocell Pair Shared Input MUX
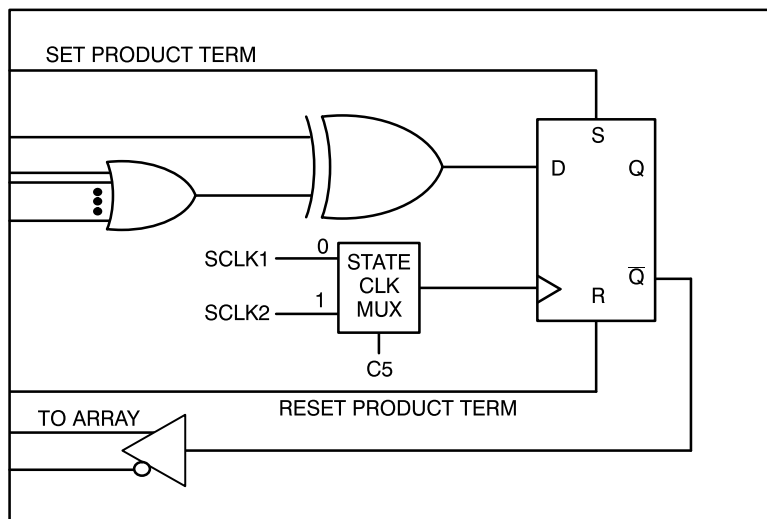
INTRO−9

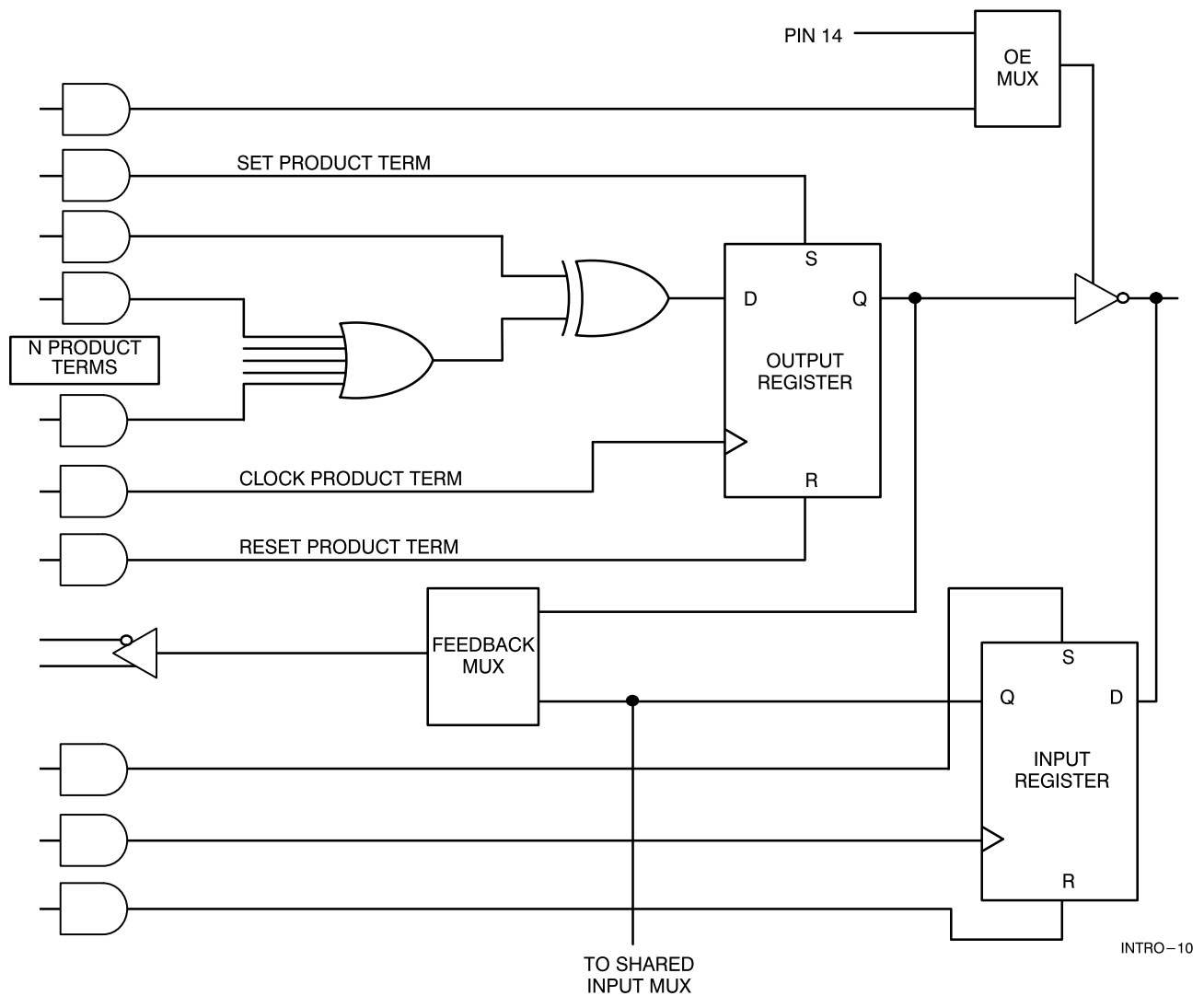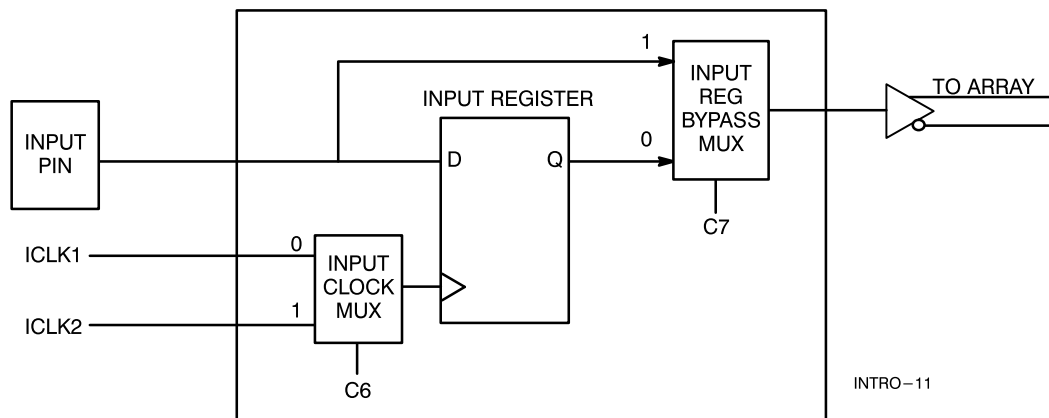**Figure 7. CY7C335 Hidden Macrocell**

Figure 8. CY7C331 Registered Asynchronous Macrocell

Figure 9. CY7C335 Input Macrocell