filename: Tuesday, August 11, 1992
Revision: October 9, 1995

pASIC380 Family

UltraLogic™ Very High Speed CMOS FPGAs

Features

- **Very high speed**
  - **— Loadable counter frequencies greater than 150 MHz**
  - **— Chip-to-chip operating frequencies up to 110 MHz**
  - **— Input + logic cell + output delays under 6 ns**
- **High usable density**
  - **— Up to 8,000 "gate array" gates, equivalent to 24,000 EPLD or LCA gates**
- **Low power, high output drive**
  - **— Standby current typically 2 mA**
  - **— 16-bit counter operating at 100 MHz consumes 50 mA**
  - **— Minimum I_{OL} and I_{OH} of 20mA (1K, 4K, and 8K)**
- **5 V and 3.3 V devices at all densities**
- **Fully PCI Compliant**
  - **— 1K, 4K, and 8K family members**
- **Flexible FPGA logic cell**
  - **— Wide fan-in (up to 14 input gates)**
  - **— Multiple outputs from each cell**
  - **— Very low cell propagation delay (1.7 ns typical)**
- **Powerful *Warp3*™ design tools**
  - **— Designs entered in VHDL, schematics, or both**
  - **— Fast, fully automatic place and route**
  - **— Waveform simulation with back annotated net delays**
  - **— PC and workstation platforms**
- **Extensive third-party tool support**
  - **— See Development Systems section**
- **Robust routing resources**
  - **— Fully automatic place and route of designs using up to 100 percent of logic resources**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **— Built-in scan path permits 100 percent factory testing of logic and I/O cells**
- **0.65µ CMOS process with ViaLink™ programming technology**
  - **— High-speed metal-to-metal link**
  - **— Non-volatile antifuse technology**

Functional Description

The pASIC380™ Family of very high speed CMOS, user-programmable, ASIC devices is based on the first FPGA technology to combine high speed, high density, and low power in a single architecture.

All pASIC380 Family devices are based on an array of highly flexible logic cells that have been optimized for efficient implementation of high-speed arithmetic, counter, data path, state machine, and glue logic functions. Logic cells are configured and interconnected by rows and columns of metal routing lines and ViaLink metal-to-metal programmable-via interconnect elements.

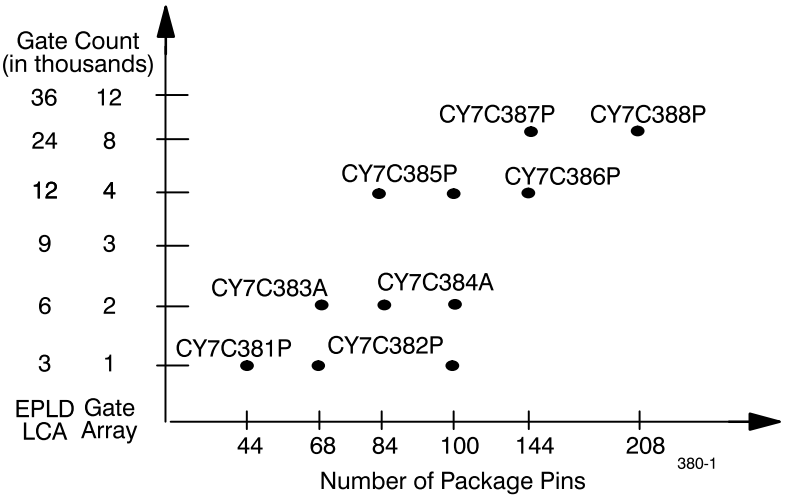
The ViaLink technology provides a non-volatile, permanently programmed custom logic function capable of operating at speeds of over 100 MHz. Internal logic cell delays are under 2 ns and total input to output combinatorial logic delays are under 8 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors, while consuming a fraction of the power and board area of PALs™, GALs™, and discrete logic elements.

pASIC380 Family devices range in density from 1000 "gate array" gates (3,000 EPLD/LCA gates) in 44- and 68-pin packages to 8,000 gates (24,000 EPLD/LCA gates) in 144- and 208-pin packages.

Designs are captured for the pASIC380 Family devices on PC or workstation platforms using Cypress's *Warp3* or third-party, general-purpose design-entry and simulation CAE packages, together with Cypress *Warp2+*™ device-specific place and route tools. Sufficient on-chip routing channels are provided to allow fully automatic place and route of designs using up to 100 percent of the available logic cells.

All the necessary hardware, software, documentation and accessories required to complete a design, from entering a schematic to programming a device are included in *Warp3* and *Impulse3*™, available from Cypress. *Warp3* includes a schematic capture system together with VHDL synthesis and a waveform-based timing simulator. All applications run under Microsoft Windows™ to insure a highly productive and easy-to-use design environment. Sun workstation UNIX and HP platforms are also available.

pASIC380 Family Members



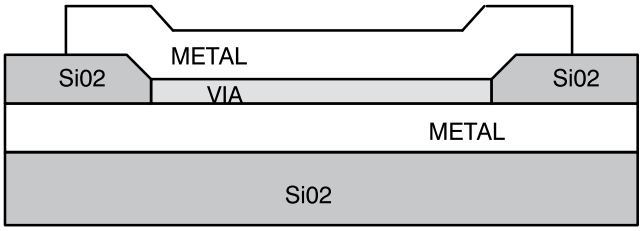


Figure 1. Unprogrammed ViaLink Element

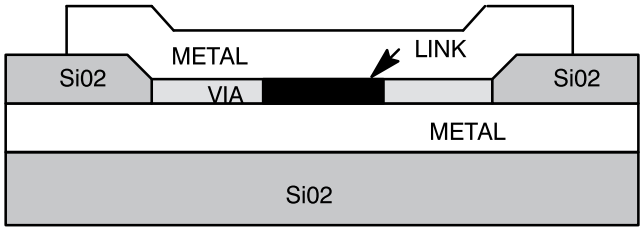


Figure 2. Programmed ViaLink Element

ViaLink Programming Element

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In pASIC380 devices, the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values as a low as 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

Figure 1 shows an unprogrammed ViaLink site. In a custom metal masked ASIC, such as a gate array, the top and bottom layers of metal make direct contact through the via. In a ViaLink programmable ASIC device, the two layers of metal are initially separated by an insulating semiconductor layer with resistance in excess of 1 gigaohm.

A programming pulse applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers, as shown in *Figure 2*. The tight distribution of link resistance is shown in *Figure 3*.

Standard CMOS Process

pASIC380 devices are the first FPGA devices to be fabricated on a conventional high-volume CMOS process. The base technology is a 0.65-micron, n-well CMOS technology with a single polysilicon layer and two layers of metal interconnect. The only deviation from the standard process flow occurs when the ViaLink module is inserted between the metal deposition steps.

As the size of a ViaLink is identical to that of a standard metal interconnect via, programmable elements can be packed very densely. The microphotograph in *Figure 4* shows an array of ViaLink elements. The density is limited only by the minimum dimensions of the metal-line to metal-line pitch.

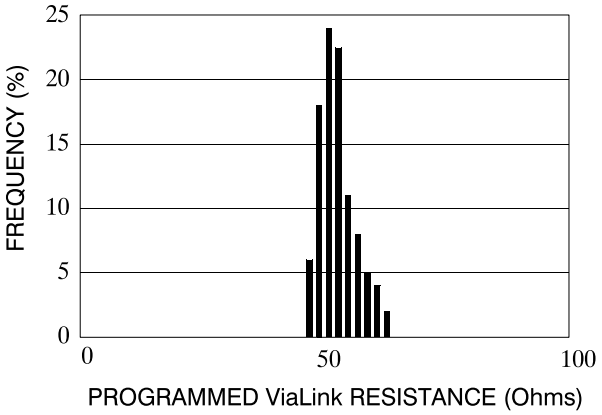


Figure 3. Distribution of Programmed Link Resistance

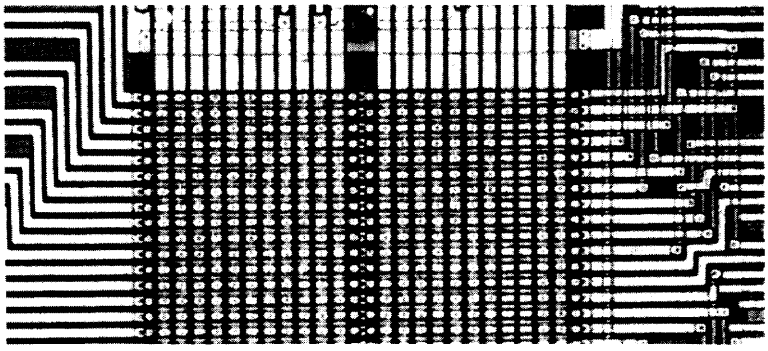


Figure 4. An Array of ViaLink Elements

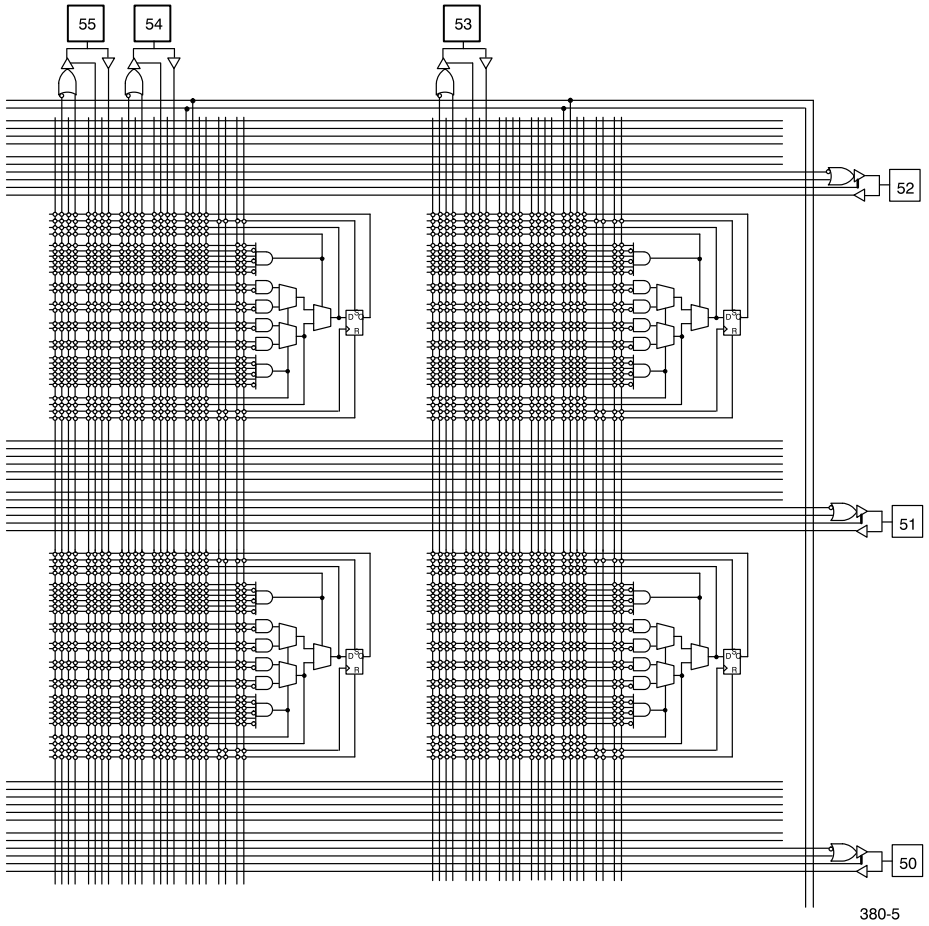


Figure 5. A Matrix of Logic Cells and Wiring Channels

The pASIC380 device architecture consists of an array of user-configurable logic building blocks, called logic cells set in a grid of metal wiring channels. *Figure 5* shows a section of a pASIC380 device containing internal logic cells, input/output cells, and dual-layer vertical and horizontal metal routing channels. The output of any cell may be programmed to connect to the input of any other cell through ViaLink elements located at all the wire intersections.

The regularity and orthogonality of this interconnect, together with the capability to achieve 100 percent routability of logic cells, makes the pASIC380 architecture similiar in structure and performance to a metal-masked gate array. It also makes system operating speed far less sensitive to partitioning and placement decisions. Minor revisions to a logic design result in only small changes in performance. (See *Figure 6.*)

Adequate wiring resources permit 100% automatic placement and routing of designs using up to 100% of the logic cells. This has been demonstrated on designs that require fixed pin placements.

Organization

The pASIC380 Family of very high speed FPGAs contains devices covering a wide spectrum of I/O and density requirements.

The key features of all pASIC380 devices are listed in *Table 1*. See the individual product datasheets for more specific information on each device.

Individual part numbers indicate unique logic cell and I/O cell combinations. For example, the CY7C383A contains 192 logic cells and 56 I/O cells in a 68-pin package. The CY7C384A also contains 192 logic cells, but it has 68 I/O cells and is packaged in 84- and 100-pin packages. Note that at each pASIC380 I/O count there is a density upgrade available in the same package. In other words, the CY7C383A features 2,000 gates in the same pinout as the 1,000-gate CY7C382P. The same applies to the CY7C385P and CY7C384A.

Gate counts for pASIC380 devices are based on the number of usable or “gate array” gates. Each of the internal logic cells has a total logic capacity of up to 30 EPLD or LCA gates. As a typical application will use 10 to 12 of these gates.

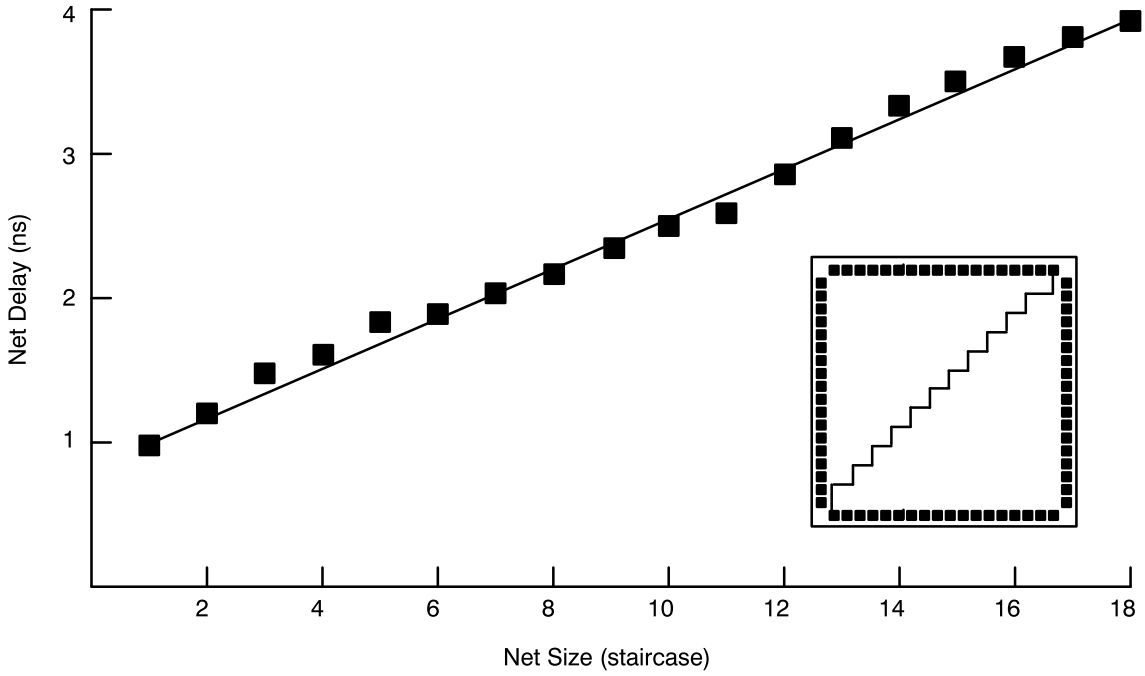


Figure 6. Net Delay vs. Net Size (4 ns “corner to corner”)

Table 1. Key Features of pASIC380 Devices

Device	Logic Cells	I/O Cells	Dedicated Inputs	Usable Gates	EPLD/LCA Gates	Packages
7C381P 7C3381A	96	32	8	1000	3000	44-Pin PLCC
7C382P 7C3382A	96	56	8	1000	3000	68-Pin PLCC 69-Pin CPGA 100-Pin TQFP
7C383A 7C3383A	192	56	8	2000	6000	68-Pin PLCC
7C384A 7C3384A	192	68/80	8	2000	6000	84-Pin PLCC 85-Pin CPGA 100-Pin TQFP
7C385P 7C3385A	384	68/80	8	4000	12000	84-Pin PLCC 100-Pin TQFP
7C386P 7C3386A	384	114	8	4000	12000	144-Pin TQFP 145-Pin CPGA 160-Pin CQFP
7C387P 7C3387P	768	116	8	8000	24000	144-Pin TQFP
7C388P 7C3388P	768	172	8	8000	24000	208-Pin CQFP 208-Pin PQFP 223-Pin CPGA

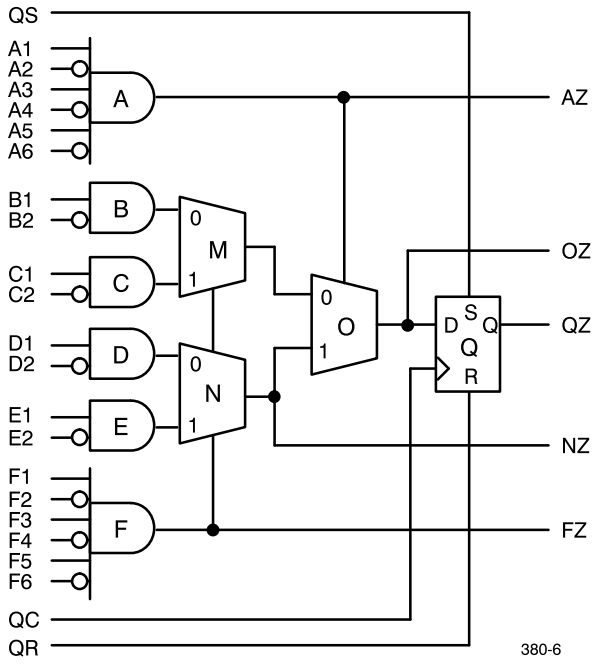


Figure 7. pASIC380 Internal Logic Cell

pASIC380 Internal Logic Cell

The pASIC380 internal logic cell, shown in *Figure 7*, is a general-purpose building block that can implement most TTL and gate array macro library functions. It has been optimized to maintain the inherent speed advantage of the ViaLink technology while ensuring maximum logic flexibility.

The logic cell consists of two 6-input AND gates, four 2-input AND gates, three 2-to-1 multiplexers and a D flip-flop. Each cell represents approximately 30 gate-equivalents of logic capability. The pASIC380 logic cell is unique among FPGA architectures in that it offers up to 14-input-wide gating functions. It can implement all possible Boolean transfer functions of up to three variables as well as many functions of up to 14 variables.

Glitch-free switching of the multiplexer is insured because the internal capacitance of the circuit maintains enough charge to hold the output in a steady state during input transitions. The multiplexer output feeds the D-type flip-flop, which can also be configured to provide JK-, SR-, or T-type functions as well as count with carry-in by using additional logic cell resources. Two independent SET and RESET inputs can be used to asynchronously control the output condition. The combination of wide gating capability and a built-in register makes the pASIC380 logic cell particularly well suited to the design of high-speed state machines, shift registers, encoders, decoders, arbitration and arithmetic logic, as well as a wide variety of counters.

Each pASIC380 logic cell features five separate outputs. The existence of multiple outputs makes it easier to pack independent functions into a single logic cell. For example, if one function requires a single register, both 6-input AND gates (A and F) are available for other uses. Logic packing is accomplished automatically with *Warp3* software.

The function of a logic cell is determined by the logic levels applied to the inputs of the AND gates. ViaLink sites located on signal wires tied to the gate inputs perform the dual role of configuring the logic function of a cell and establishing connections between cells.

A detailed understanding of the logic cell is not necessary to successfully design with pASIC380 devices. CAE tools will automatically translate a conventional logic schematic and/or VHDL source code into a device and provide excellent performance and utilization.

Three types of input and output structures are provided on pASIC380 devices to configure buffering functions at the external pads. They are called the Bidirectional Input/Output (I/O) cell, the Dedicated Input (I) cell, and the Clock/Dedicated Input (CLK/I) cell.

The bidirectional I/O cell, shown in *Figure 8*, consists of a 2-input OR gate connected to a pin buffer driver. The buffer output is controlled by a three-state enable line to allow the pad to also act as an input. The output may be configured as active HIGH, active LOW, or as an open drain inverting buffer.

The output buffers are designed to ensure quiet switching characteristics while maintaining high speed. Measured results show up to 48 outputs switching simultaneously into a 10 pF load with less than ± 1 Volt of output switching noise.

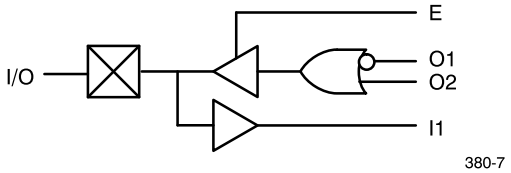


Figure 8. Bidirectional I/O Cell

The Dedicated Input cell, shown in *Figure 9*, conveys true and complement signals from the input pads into the array of logic cells. As these pads have nearly twice the current drive capability of the I/O pads, they are useful for distributing high fanout signals across the device.

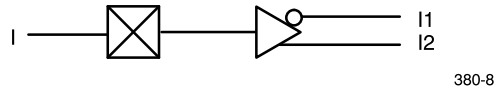


Figure 9. Dedicated Input High-Drive Cell

The Clock/Dedicated Input cell (*Figure 10*) drives a low-skew, fanout-independent clock tree that can connect to the clock, set, or reset inputs of the logic cell flip-flops.

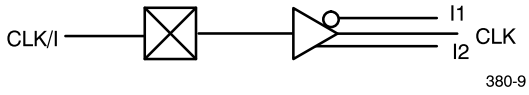


Figure 10. Clock/Dedicated Input Cell

pASIC380 Interconnect Structure

Multiple logic cells are joined together to form a complex logic function by interconnection through the routing channels. To describe the organization of these routing channels, a hypothetical 14-pin device consisting of two logic cells is shown in *Figure 11*. This

device contains the same architectural features as the members of the pASIC380 family.

Active logic functions are performed by the internal logic cells, the I/O cells (pins 2, 3, 7, 9, 10, and 14) and the I cells (pins 4, 6, 11, and 13). These cells are connected with vertical and horizontal wiring channels.

Four types of signal wires are employed: segmented wires, quad wires, express wires, and clock wires. Segmented wires are predominantly used for local connections and have ViaLink elements known as a Cross Link (denoted by the open box symbol), at every crossover point. They may also be connected to the segmented wires of cells above and below through ViaLink elements, called Pass Links (denoted by the X symbol). Express lines are similar to segmented wires except that they are not divided by Pass Links. Quad Lines are a compromise between express and segmented lines. Quad wires are used for local interconnect, but have pass links at every forth logic cell.

Dedicated clock wires are lightly loaded with only three links per cell to distribute high-speed clock edges to the flip-flop CLK, SET, and RESET inputs. Express wires may also be used to deliver clock signals into the multiplexer region of the cell for combinatorial gating. The automatic place and route software allocates signals to the appropriate wires to insure the optimum speed/density combination.

Vertical V_{CC} and GND wires are located close to the logic cell gate inputs to allow any input that is not driven by the output of another cell to be automatically tied to either V_{CC} or GND. All of the vertical wires (segmented, express, quad, clock, and power) considered as a group are called vertical channels. These channels span the full height of the device and run to the left of each column of logic cells.

Horizontal wiring channels, called rows, provide connections, via cross links, to other columns of logic cells and to the periphery of the chip. Appropriate programming of ViaLink elements allows electrical connection to be made from any logic cell output to the input of any other logic or I/O cell.

Ample wires are provided in the channels to permit automatic place and route of designs using up to 100 percent of the device logic cells. Designs can be completed automatically even with a high percentage of fixed user placement of internal cells and pin locations.

This information is presented to provide the user with insight into how a logic function is implemented in pASIC380 devices. However, it is not necessary to develop a detailed understanding of the architecture in order to achieve efficient designs. All routine tasks are fully automatic. No manual wire routing is necessary, nor is it permitted by the software. Fully automatic placement of logic functions is also offered. But if it is necessary to achieve a specific pin configuration or register alignment, for example, manual placement is supported.

Power Consumption

Typical standby power supply current consumption, I_{CC1}, of a pASIC380 device is 2 mA. The worst-case limit for standby current (I_{CC1}) over the full operating range of the pASIC380 devices is 10 mA. Formulas for calculating I_{CC} under AC conditions (I_{CC2}) are provided in the “pASIC380 Family Quick Power Calculation” application note.

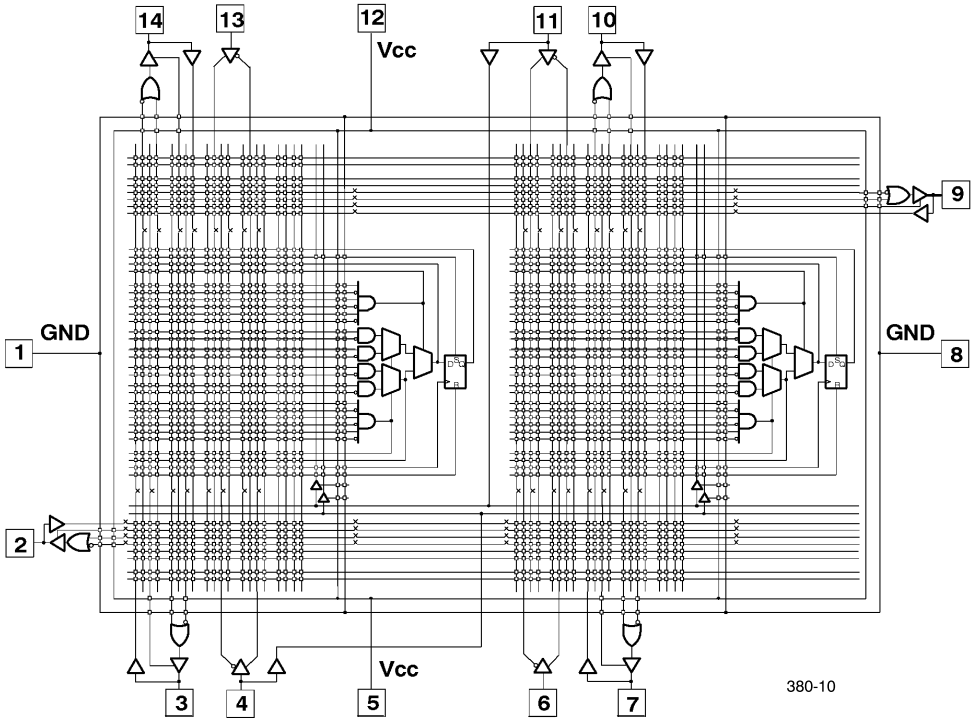


Figure 11. pASIC380 Device Features

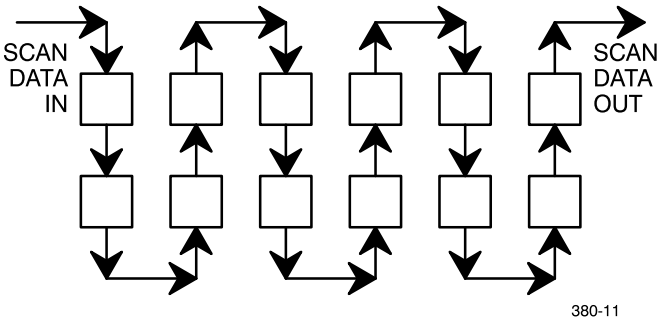


Figure 12. Internal Serial Scan Path

Programming and Testing

pASIC380 devices may be programmed and functionally tested on the Cypress *Impulse3* Programmer and a variety of third party programmers. See the third party tools section.

All pASIC380 devices have a built-in serial scan path linking the logic cell register functions (*Figure 12*). This is provided to improve factory test coverage and to permit testing by the user with automatically generated test vectors following programming.

Reliability

The pASIC380 Family is based on a 0.65-micron high-volume CMOS fabrication process with the VIALink programmable-via antifuse technology inserted between the metal deposition steps. The base CMOS process has been qualified to meet the requirements of MIL-STD-883B, Revision C.

The ViaLink element exists in one of two states: a highly resistive unprogrammed state, OFF, and the low-impedance, conductive state, ON. It is connected between the output of one logic cell and the inputs of other logic cells directly or through other links. No DC current flows through either a programmed or an unprogrammed link during operation as a logic device. An unprogrammed link sees a worst-case voltage equal to V_{CC} biased across its terminals. A programmed link carries AC current caused by charging and discharging of device and interconnect capacitances during switching.

Studies of test structures and complete pASIC380 devices have shown that an unprogrammed link under V_{CC} bias remains in the unprogrammed state over time. Similar tests on programmed links under current bias exhibit the same stability. The long-term reliability of the combined CMOS and ViaLink structure is similar to that of the base gate array process. For further details, see the pASIC380 Family Reliability Report, contained in the reliability section of the Programmable Logic Data Book.

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