pASIC380 Family

Reliability Report

Introduction

The Cypress pASIC380 family of very high speed FPGAs is built by integrating the ViaLink™ metal-to-metal antifuse programming element into a standard high-volume CMOS gate array process.

Reliability testing of pASIC™ devices is part of a continuous process to insure long-term reliability of the product. It consists of industry-established accelerated life tests for basic CMOS devices plus additional stress tests. The addition of two high-voltage life tests stresses the unprogrammed and programmed ViaLink elements beyond conventional CMOS reliability testing.

Results to date, from the evaluation of over 7000 pASIC380 devices from multiple wafer lots, indicate that the addition of the ViaLink element to a well-established CMOS process has no measurable effect on the reliability of the resulting product. There have been no failures related to the ViaLink element in 210 million equivalent device hours of high-temperature operating life. The observed failure rate is 14 FITs, and the failure rate at a 60% confidence level is 19 FITs.

Process Description

The pASIC380 devices are fabricated using a standard, high-volume 0.65-micron CMOS process with twin-well, single-poly, and double-layer metal interconnect. This technology has been qualified to meet MIL−STD−883D.

The ViaLink element is located in an intermetal oxide via between the first and second layers of metal. It is created by depositing a very high resistance silicon film in a standard size metal one to metal two via. The silicon deposition is done at low temperature and causes no change to the properties of the CMOS transistors. When deposited at low temperatures, silicon forms an amorphous structure that can be electrically switched from a high-resistance state ($\cong$5 GΩ) to a low-resistance state ($\cong$50Ω) for an off-to-on ratio of 10^8. Cypress takes advantage of this property to create the ViaLink metal-to-metal antifuse programming element (see *Figure 13*).

The programming voltage of the ViaLink element varies with amorphous silicon thickness. For a desired programming voltage between 10−12 volts, the thickness of the amorphous silicon film is approximately 1000Å. This is ideal for good process control and minimizes the capacitive coupling effect of an unprogrammed element located between the two layers of metal.

Amorphous silicon is deposited with standard semiconductor manufacturing equipment and processing techniques. In addition to antifuse elements, it is used in the high-volume fabrication of image sensors, decode, and drive circuits for flat panel displays, and high-efficiency solar cells.

Failure Mechanisms in the pASIC380 Device

A variety of failure mechanisms exists in CMOS integrated circuits. Since the overall failure rate is composed of various failure mechanisms, each having different temperature dependence and thus varying time-temperature relationships, it is important to understand the characteristics of each contributing failure mechanism. *Table 2* lists nine key failure mechanisms that have been characterized for standard CMOS devices, plus the two mechanisms for the programmed and unprogrammed ViaLink elements.

Various accelerated life tests are used to detect the possible contribution of each mechanism to the overall failure rate of the device. Failure rate data taken at elevated temperature can be translated to a lower temperature through the Arrhenius equation. This equation, in the form of an acceleration factor, A_f, can be written as

$$A_f = \exp[-E_a/k(1/T_s - 1/T_o)] \qquad \text{Eq. 1}$$

where T_s is the stress temperature, T_o is the operating temperature of the device, E_a is the activation energy for that mechanism, and k is the Boltzmann constant.

In *Table 2*,

t_{50} = the mean time to failure,
E = electric field,
E_a = activation energy,
k = Boltzmann constant (8.62×10^{-5} eV/°K),
W = metal width,
t = metal thickness,
J = current density,
g_m = transconductance,
V_T = threshold voltage,
T = absolute temperature,
RH = relative humidity,
D = diffusion constant.
A, m, and p are constants.

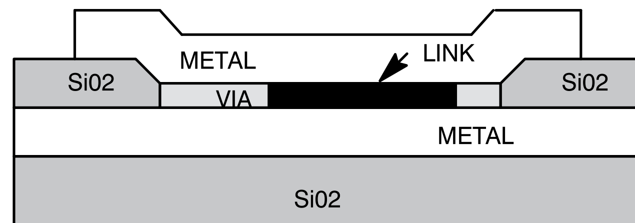

Figure 13. Cross Section of a ViaLink Antifuse

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Table 2. Failure Mechanisms That May Be Operative in pASIC380 Devices

Failure Mechanism	t_{50} Dependence	Activation Energy (E_a)	Detection Tests
Insulator breakdown (leakage, opens)	$\exp(-\beta/E)$ value of β depends on the dielectric and may be temperature dependent	Approx. 0.3 eV for SiO_2 and dependent on E	High-voltage operating life test (HTOL)
Parameter shifts due to contamination (such as Na)	$\exp(E_a/kT)$ (Arrhenius)	1.0 eV	High-temperature bias
Silicon defects (leakage, etc.)	Arrhenius	0.5 eV	High-voltage and guard-banded tests
Metal line opens from electromigration	$\frac{Wt}{J^2}\exp(E_a/kT)$	Approx. 0.7 eV for Al+Cu alloys	HTOL
Masking and assembly defects	$\exp(E_a/kT)$ (Arrhenius)	0.5 eV	High-temperature storage and HTOL
Shorts channel charge trapping (V_T and g_m shifts)	$g_m \cong \exp(-AE)$	Approx. −0.06 eV	Low-temperature, high-voltage operating life test
Stress-induced open metal (operative only on non-clad metal systems)	$W^m t^p \exp(E_a/kT)$ (m and p range from 1.3 to 4.7)	0.6 to 1.4 eV	Temperature cycling
Open metal from electrolytic corrosion	$(\%RH)^{-4.5}\exp(E_a/kT)$	0.3 to 0.6	High-temperature/ high-humidity/bias test
Wire bond failure from excessive gold-aluminum interdiffusion	$1/(Dt)^{1/2}$ where $D = D_0\exp(E_a/kT)$	0.7 eV	HTOL
Parameter shifts due to contamination (such as Na)	Arrhenius	1.0 eV	High temp. bias
Plastic Chemistry of the package	Arrhenius	1.0 eV	High temp./high humidity/bias test
Polarization in the thin film layers	Arrhenius	1.0 eV	High temp./high humidity/bias test
Microcrack in oxides and thin films	Arrhenius	1.3 eV	HTOL/Temp. Cycling
Unprogrammed ViaLink	$\exp(-BE)$	0 eV	High V_{CC} static life test
Programmed ViaLink	$\exp(-PJ)$	0 eV	Low-temperature operating life test

Accelerated Life Tests on pASIC380

The purpose of a life test is to predict the reliability and failure rate of a device. However, a device operating under normal operating conditions would require years of testing to determine its long-term reliability. Methods of accelerating failures developed in the industry allow accurate prediction of a device life time and failure rate in a much shorter time duration. Accelerated stress tests are run at high temperature, high voltages, or a combination of both. *Table 3* contains the results of the tests performed on a programmed pASIC380, where approximately 4% ViaLink elements were programmed and approximately 96% were left unprogrammed. These numbers are typical for a fully utilized device.

All tests were performed with a proprietary reliability pattern that stresses the programmed and unprogrammed ViaLinks. A failure is defined as any change in the DC characteristic beyond the datasheet limits and any measurable change in the AC performance.

The overall reliability of the pASIC380 devices as indicated by the results of the tests shown in *Table 3* is 19 FITs with a 60% confidence.

Details of each of the tests of *Table 3* are given in the following sections. The failure mechanisms specific to the ViaLink antifuse element are described in detail.

Standard CMOS Tests and Results

HTOL is the life test that operates the device at a high V_{CC} and high temperature. This test is used to determine the long-term reliability and failure rate of the device in the customer environment. The specific condition of this test is defined by the MIL−STD−883D Quality Conformance Test. The devices are operated at 5.5V and 125°C for 1000 hours. The acceleration due to temperature can be calculated by using *Equation 1*, assuming an average activation energy of 0.7 eV and an operating temperature of 55°C. The observed failure rate in FITs is

$$\text{Failure Rate} = (\text{failures}) \times \frac{(10^9 \text{ device-hrs})}{(\text{total equivalent device-hrs})} \quad \text{Eq. 2}$$

The generally reported failure rate is a 60% confidence level of the observed FITs. The failure rate at this confidence level is calculated using Poisson statistics since the distribution is valid for a low failure occurrence in a large sample.

The acceleration factor from *Equation 1*, for 55°C and $E_a = 0.7$ eV is 78. Therefore, from the results shown in *Table 4*, the pASIC380 has been operating for more than 210 million equivalent device hours with three failures. One was due to a gate oxide failure and the other was an I_{CC} failure due to an improper test limit at final test. the test limit was corrected before any units were shipped to

customers. The failure in the 7C382 was due to particle at via etch. The particles have been significantly reduced as part of an ongoing quality and yield improvement. The observed failure rate is 14 FITs and the failure rate at a 60% confidence levels is 19 FITs.

There were no failures during the first 500 hrs of life test. The pASIC380 does not have an early life failure problem.

Table 3. Results of Accelerated Life Tests on the pASIC380

Test	Process Qual. Acceptance Requirements	Test Results
HTOL, 1,000 hrs, 125°C, V_{CC} = 5.5V, MIL−STD−883C, Method 1005	≤100 FITs @ 55°C, E_a = 0.7 eV, 60% confidence	3 failures, 14 observed FITs, 19 FITs at a 60% confidence, 2778 units from 41 lots
High-temperature storage, 1,000 hrs., 150°C, unbiased	LTPD=5%	0% failures, 210 units from 6 lots
THB, 1,000 hrs., alternately biased, 85% R.H., 85°C, JEDEC STD 22−B, Method A101 or HAST 50 hrs 85% RH, 100°C, JEDEC STD 22−A110	LTPD=5%	0.51% failures, 791 units from 26 lots
Temperature cycle, 1,000 cycles, −65°C to 150°C, MIL−STD−883D, Method 1010	LTPD=5%	0.12% failures, 854 units from 26 lots
Thermal shock, 100 cycles, −65°C to 150°C, 883C, Method 1011	≤1% cumulative failures per test	0% failures, 854 units from 3 lots
Pressure Pot, 168 hrs., 121°C, 2.0 atm., no bias	LTPD=5%	0% failures, 518 units from 26 lots
High V_{CC} static life, 1,000 hrs., 25°C, V_{CC} = 7.0V, static	<20 FITs due to unprogrammed ViaLink element, A_f = 130	0 observed FITs, 675 units from 12 lots
Low Temperature operating life, 1,000 hrs., −55°C, V_{CC} = 6.0V, 8-15 MHz	<20 FITs due to programmed ViaLink element, A_f = 380	0 observed FITs, 1605 units from 21 lots, 3 failures not related to ViaLink element

Table 4. Results of High-Temperature Operating Life Test
(V_{CC} = 5.5V, Temp. = 125°C, f = 1 MHz)

Package	Fab Lot	Device	Quantity	Failures @ Hours		
				168	500	1,000
68PLCC	18362	7C382	100	0	0	0
68PLCC	19194	7C382	100	0	0	0
68PLCC	19618	7C382	100	0	0	0
68PLCC	20454	7C382	100	0	0	0
68PLCC	20470	7C382	76	0	0	0
68PLCC	20534	7C382	82	0	0	0
68PLCC	21786	7C382	76	0	0	0
68PLCC	33669	7C382	70	0	0	0
68PLCC	34515	7C382	100	0	0	0
68PLCC	35421	7C382	100	0	0	0
68PLCC	34267	7C382A	100	0	0	0
68PLCC	36129	7C382A	100	0	0	0
68PLCC	40673	7C382A	51	0	0	0
68PLCC	1346945	7C382A	100	0	0	0
68PLCC	1351104	7C382A	100	0	0	0
68PLCC	1409354	7C382A	100	0	0	1
84PLCC	20762	7C384	100	0	0	0
84PLCC	22164	7C384	100	0	0	1

Table 4. Results of High-Temperature Operating Life Test (continued)
(V_{CC} = 5.5V, Temp. = 125°C, f = 1 MHz)

Package	Fab Lot	Device	Quantity	Failures @ Hours		
				168	500	1,000
84PLCC	23001	7C384	100	0	0	1
84PLCC	23093	7C384	36	0	0	0
84PLCC	22988	7C384	32	0	0	0
84PLCC	23091	7C384	38	0	0	0
84PLCC	35284	7C384	100	0	0	0
84PLCC	36935	7C384	100	0	0	0
84PLCC	36936	7C384	98	0	0	0
84PLCC	37448	7C384	65	0	0	0
84PLCC	37449	7C384	74	0	0	0
84PLCC	39068	7C384	54	0	0	0
84PLCC	40670	7C384	50	0	0	0
84PLCC	40672	7C384	50	0	0	0
84PLCC	1415570	7C384A	67	0	0	0
84PLCC	1418672	7C384A	73	0	0	0
84PLCC	1328491	7C385A	2	0	0	0
84PLCC	1337713	7C385A	22	0	0	0
84PLCC	1337739	7C385A	19	0	0	0
84PLCC	1407324	7C385A	20	0	0	0
84PLCC	1407325	7C385A	38	0	0	0
84PLCC	1413492	7C385A	6	0	0	0
84PLCC	5–6	7C385A	24	0	0	0
84PLCC	15–18	7C385A	46	0	0	0
84PLCC	various	7C385A	9	0	0	0
TOTAL			2778	0	0	3

High-Temperature Storage

High-temperature storage test is a 150°C, 1,000-hour, unbiased bake. This test accelerates failures due to mobile charge, thermal instabilities, and bond ball intermetallic formation. The results in *Table 5* demonstrate the stability of the programmed and unprogrammed ViaLink element and the long-term shelf life of pASIC380.

Table 5. Results of High-Temperature Storage Test
(No Bias, Temp. = 150°C)

Package	Fab Lot	Device	Quantity	Failures @ Hours		
				168	500	1,000
68PLCC	18362	7C382	35	0	0	0
68PLCC	19194	7C382	35	0	0	0
68PLCC	19390	7C382	35	0	0	0
68PLCC	34515	7C382	35	0	0	0
68PLCC	35421	7C382	35	0	0	0
68PLCC	35422	7C382	35	0	0	0
TOTAL			210	0	0	0

Temperature, Humidity, and Bias (85/85)

The temperature, humidity, and bias test is performed under severe environmental conditions. The device is exposed to a temperature of 85°C and a relative humidity of 85% for 1,000 hours, while the pins are alternately biased between 0 and 5.5 volts (JEDEC STD 22−B). An alternate temperature, humidity and bias test is HAST, a Highly Accelerated Stress Test. This test is similiar to the 85°C/85% relative humidy test except that the test is done at 130°C and 85% relative humidity. The vapor pressure at this test condition is 33.5 psia. The pins are bias alternatively at 5.5 volts for 50 hours (JEDEC STD 22-A110). Some parts were stressed more at a more stringent condition, 140°C for 128 hours.

These two tests are effective at detecting corrosion problems, while also stressing the package and bonding wires. *Table 6* shows that the pASIC380 had three failures from the total 482 units in 85/85 and one failure in HAST. The first failure was an I_{CC} failure caused by a power supply surge. The second failure was a short due to a particle under metal 2. The third failure was and I_{CC} failure due to the same improper test limit which caused a failure in HTOL. The limit was corrected before units were shipped to customers. The one HAST failure in the 7C384 was due to a metal short. The ongoing quality and yield improvement effort has reduced the defect level.

Table 6. Results of Temperature, Humidity, and Bias Test
(85% R.H., Temp. = 85°C, pins alternately biased at 5.5V)

Package	Fab Lot	Device	Quantity	Failures @ Hours		
				168	500	1,000
68PLCC	19194	7C382	100	0	0	0
68PLCC	19168	7C382	100	0	0	0
68PLCC	19454	7C382	100	0	0	0
68PLCC	34515	7C382	35	1	0	0
68PLCC	35421	7C382	35	1	0	0
68PLCC	35422	7C382	35	0	0	0
84PLCC	20762	7C384	29	0	0	0
84PLCC	23000	7C384	24	1	0	0
84PLCC	23001	7C384	24	0	0	0
TOTAL			482	3	0	0

(HAST, Temp. =130°C, 85% R.H., pins alternately biased at 5.5V)

Package	Fab Lot	Device	Quantity	Failures @ Hours	
				50@ 130°C	128@ 140°C
100TQFP	36936	7C384	15	0	−
100TQFP	37447	7C384	13	0	−
100TQFP	37448	7C384	17	−	−
68PLCC	1409354	7C382A	25	−	0
68PLCC	1409353	7C382A	20	−	0
84PLCC	1402176	7C385A	30	−	0
84PLCC	1402177	7C385A	15	−	0
84PLCC	1410389	7C385A	15	−	0
84PLCC	1408334	7C385A	16	−	0
84PLCC	1450263	7C385A	14	−	0
84PLCC	1417657	7C385A	22	−	0
144TQFP	10885	7C385A	2	−	0
144TQFP	1412454	7C385A	14	0	−
144TQFP	1413492	7C385A	15	1	−
144TQFP	49403007	7C385A	16	0	−
144TQFP	1411431	7C385A	15	0	−
144TQFP	1417657	7C385A	45	0	−
TOTAL			309	1	0

Temperature Cycle Tests

The temperature cycle test stresses the packaged part from −65°C to 150°C for 1,000 cycles. The air-to-air cycling follows the MIL−STD−883D Quality Conformance Test. This test checks for any problems due to thermal expansion stresses. The plastic package, lead frame, silicon die, and die materials expand and contract at different rates. This mismatch can lead to cracking, peeling, or delamination of the high-stress layers. The results in *Table 7* show that the pASIC380 devices had one failure due to a lifted bond.

Table 7. Results of Temperature Cycle Test
(Air-to-air 65°C to 150°C)

Package	Fab Lot	Device	Quantity	Failures @ Cycles		
				250	500	1,000
68PLCC	18362	7C382	35	0	0	0
68PLCC	19194	7C382	35	0	0	0
68PLCC	19618	7C382	35	0	0	0
68PLCC	34515	7C382	35	0	0	0
68PLCC	35421	7C382	35	0	0	0
68PLCC	35422	7C382	35	0	0	0
68PLCC	39017	7C382A	38	0	0	0
84PLCC	20762	7C384	29	0	0	0
84PLCC	22999	7C384	24	0	0	0
84PLCC	23000	7C384	24	0	0	0
84PLCC	39068	7C384	85	0	0	1
84PLCC	38980	7C384	37	0	0	0
84PLCC	38979	7C384	65	0	0	0
100TQFP	36934	7C382A	30	0	0	0
100TQFP	36128	7C382A	30	0	0	0
100TQFP	36129	7C382A	30	0	0	0
100TQFP	37447	7C384	30	0	0	0
100TQFP	37448	7C384	30	0	0	0
100TQFP	36936	7C384	30	0	0	0
84PLCC	1409378	7C384A	30	0	–	0
84PLCC	1417657	7C384A	31	0	–	0
84PLCC	1416600	7C385A	16	0	–	0
144TQFP	1342851	7C386A	25	0	–	0
144TQFP	1405263	7C386A	15	0	–	0
144TQFP	1351123	7C386A	15	0	–	0
144TQFP	1417657	7C386A	30	0	–	0
TOTAL			854	0	0	1

Thermal Shock Tests

The thermal shock test cycles the packaged part through the same temperatures as the temperature cycle test except that the cycling is done from liquid to liquid. The temperature change is nearly instantaneous in this case. The rapid temperature change can result in higher stresses in the package and lead frame. The results in *Table 8* show that the pASIC380 devices had no failures.

Table 8. Results of Thermal Shock Test
(Liquid to Liquid, −65°C to 150°C, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Cycle
		100
18362	35	0
19194	35	0
19618	35	0

Pressure Pot Tests

The pressure pot test is performed at 121°C at 2.0 atmospheres of saturated steam with devices in an unbiased state. This test forces moisture into the plastic package and tests for corrosion in the bonding pads and wires that are not protected by passivation. Corrosion can also occur in passivated areas where there are micro cracks or poor step coverage. pASIC380 devices had no failures, as shown in *Table 9*.

Table 9. Results of Pressure Pot Test
(Pressure = 2.0 atm., Temp. = 121°C, no bias)

Package	Fab Lot	Device	Quantity	Failures @ Hours		
				48	96	168
68PLCC	18362	7C382	35	0	0	0
68PLCC	19194	7C382	35	0	0	0
68PLCC	19390	7C382	35	0	0	0
68PLCC	34515	7C382	35	0	0	0
68PLCC	35421	7C382	35	0	0	0
68PLCC	35422	7C382	35	0	0	0
84PLCC	20762	7C384	28	0	0	0
84PLCC	22999	7C384	25	0	0	0
84PLCC	23000	7C384	24	–	–	0
100TQFP	36936	7C384	15	–	–	0
100TQFP	37447	7C384	15	–	–	0
100TQFP	37448	7C384	15	–	–	0
68PLCC	1346945	7C382A	15	–	–	0
68PLCC	1350096	7C382A	15	–	–	0
68PLCC	1350104	7C382A	15	–	–	0
84PLCC	1417657	7C385A	30	–	–	0
84PLCC	1416600	7C385A	15	–	–	0
84PLCC	1409360	7C385A	36	–	–	0
84PLCC	1410389	7C385A	15	–	–	0
84PLCC	1350093	7C385A	15	–	–	0
84PLCC	1403209	7C385A	15	–	–	0
84PLCC	1402177	7C385A	15	–	–	0
144TQFP	1342851	7C385A	15	–	–	0
144TQFP	1405263	7C385A	15	–	–	0
144TQFP	1351123	7C385A	15	–	–	0
144TQFP	1417657	7C385A	30	–	–	0
TOTAL			518	0	0	0

ViaLink Element Reliability Tests and Results

The ViaLink antifuse is a one-time programmable device. In the unprogrammed state it has a resistance of greater than one gigaohm and capacitance of less than one femtofarad.

The application of a programming voltage above a critical level across the antifuse structure, causes the device to undergo a switching transition through a negative resistance region into a low-resistance state. The magnitude of the current allowed to flow in the low-resistance state, the programming current, is predetermined by design. A link of tungsten, titanium, and silicon alloy is formed between metal one and metal two during the programming process.

The link has a metallic-like resistivity of the order of 500 micro-ohms-cm and is responsible for the low 50-ohm resistance that is a unique characteristic of the ViaLink antifuse.

The link forms a permanent, bidirectional connection between two metal lines. The size of the link, and hence the resistance, depends on the magnitude of the programming current. *Figure 6* shows the

relationship between programming current and programmed link resistance. *Figure 15* shows the distribution of link resistance for a fixed programming current.

Unprogrammed ViaLink Element Reliability

Reliability studies on an antifuse that can exist in two stable resistance states, must focus on the ability of an unprogrammed and a programmed device under stress to remain in the desired state. In the context of standard IC testing, the antifuse should be stressed under conditions similar to those for a dielectric (in the unprogrammed state) and for a conductor (in the programmed state).

For ViaLink elements in the unprogrammed state, the tests must determine their ability to withstand applied voltages over the range of operating conditions without changing resistance or becoming programmed. Amorphous materials might be expected to show gradual changes in resistance as a result of relaxation or annealing. Reliability studies have been designed to explore these effects.

When a ViaLink element is stressed at high electric fields, its resistance can decrease from the initial 1 GΩ value. The reliability testing program examined the time for the resistance to reach 50 MΩ at different stress fields. *Figures 17* and *16* illustrate that because of time constraints (≅ 500 years), it is impossible to detect this effect at normal operating fields in systems.

The pASIC380 device is designed to operate with resistance of the unprogrammed ViaLink element from 50 MΩ to greater than 1 GΩ at 20°C, and remain within the guaranteed speed and standby I_{CC} specifications.

Figure 16 shows the time required for a ViaLink element to reach 50 MΩ under various applied electric fields at different temperatures. The time required for the change is not accelerated by temperature over the studied range of electric fields. The activation energy, E_a, for this process is zero.

Figure 17 shows the time required for a ViaLink element to reach 50 MΩ under various electric field stresses. A range of amorphous silicon thicknesses have been included in this chart. The data can be modeled using the equation

$$t_{50M\Omega} = t_0 \exp(-BE) \qquad \text{Eq. 3}$$

where the time to 50 MΩ decreases exponentially with increasing applied electric field. The constant t_0 is $3x10^{15}$ seconds and the field acceleration factor, B, is 20 cm/MV. The model is valid for electric fields, E, below 1.5 MV/cm. Above this field, the amorphous silicon antifuse programs. The electric field for 5.0 volt V_{CC} operation with a typical amorphous silicon thickness is 0.61 MV/cm, which extrapolates $t_{50M\Omega}$ to $1.5x10^{10}$ seconds, or 500 years. The time to 50 MΩ for the worst-case amorphous silicon thickness and operating at worst-case V_{CC} is in excess of 30 years.

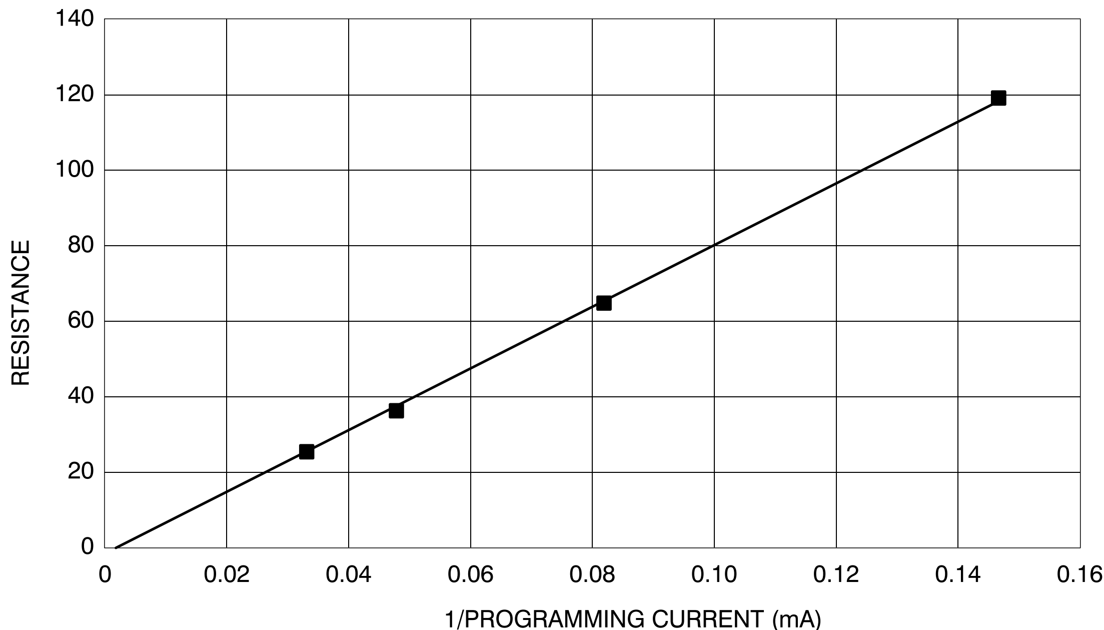

Figure 14. Resistance Versus 1/Programming Current
($R = 0.810/I_P$)

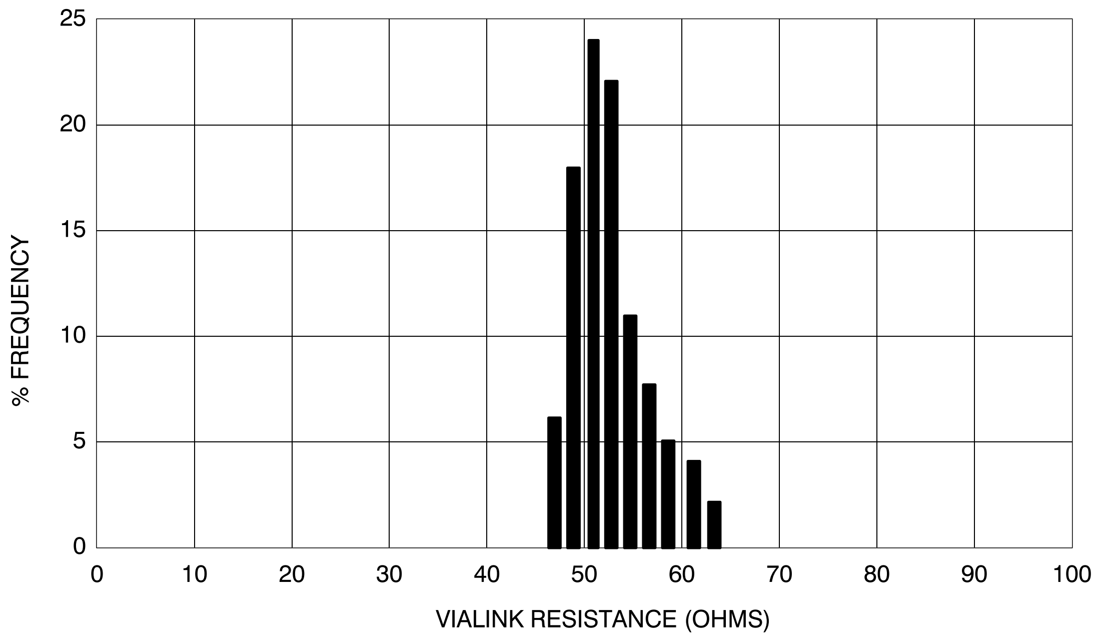

Figure 15. Distribution of ViaLink Resistance at I_P = 15 mA
(Average = 52.3 Ohms, Satndard Deviation = 3.69)

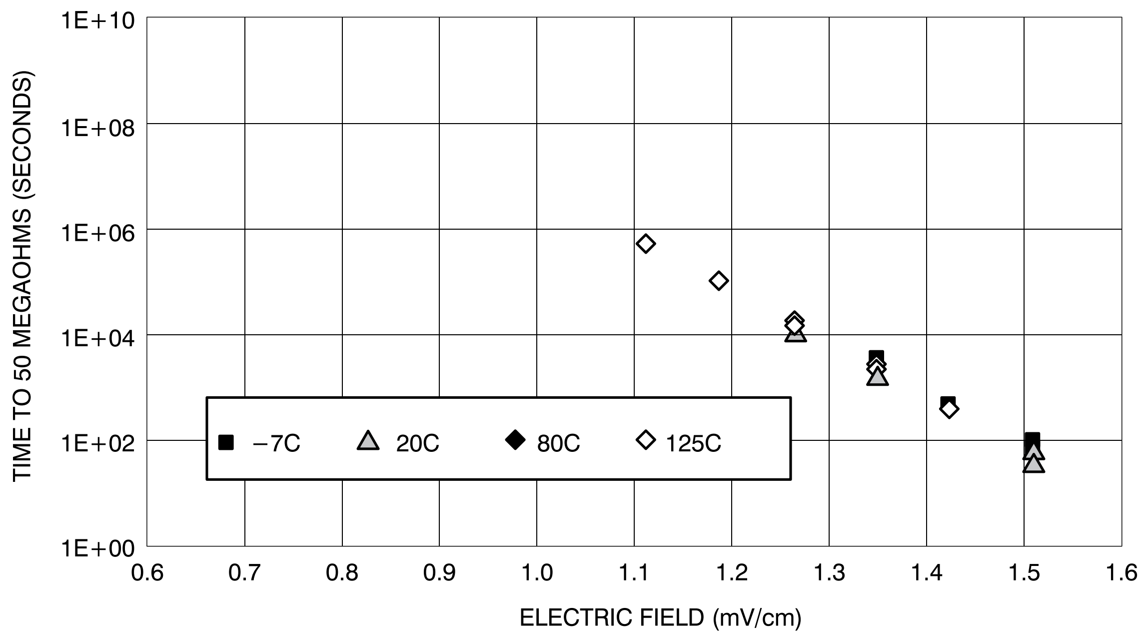

Figure 16. Temperature Dependence of Time to 50 Megaohms (Lot 617, Wafer 8)

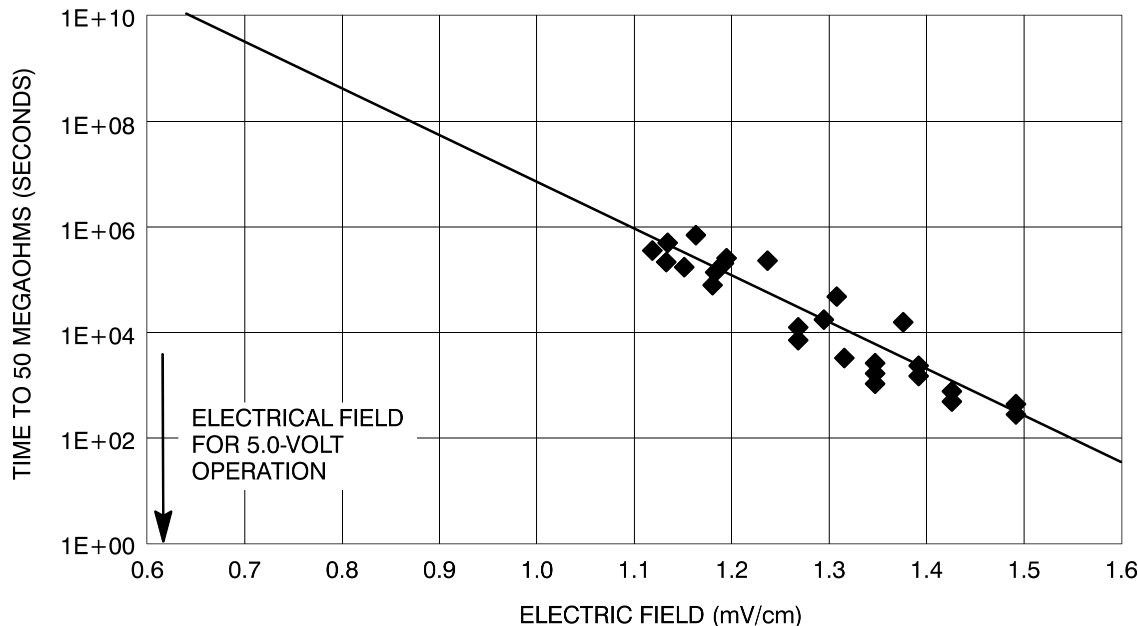

Figure 17. Electric Field Acceleration of Unprogrammed ViaLink Element

The high field effect is both predicable and reproducible, and reversible. This effect is inherent in the amorphous silicon in the ViaLink element. The pASIC380 device has been designed to operate where the effect is minimized and has no impact on the reliability of the pASIC380 device. The pASIC380 device lifetime extrpolations are based on the average unprogrammed ViaLink element since the effect on the increaased ICC of the pASIC380 is the sum of the leakages through the unprogrammed ViaLink elements. The time dependent resistance of the ViaLink elements does not degrade the functionality or AC performance of the pASIC380.

Accelerated Stress Tests for Unprogrammed ViaLink Elements

The high field effect is created in the packaged pASIC380 device through a high V_{CC} static life test. This test stresses the unprogrammed ViaLink element with a V_{CC} = 7.0 volts for 1000 hours. Over 600 pASIC380 devices from four lots have been tested. This condition stresses over 20,000 unprogrammed ViaLink elements in each pASIC380. The failure criteria for the pASIC380 device for this test is the same as that of the previous tests, with emphasis placed on the standby I_{CC}, which increases as the resistance of the unprogrammed ViaLink element decreases. The acceleration factor for this stress is calculated by using *Equation 3* to find the ratio of the t_{50M} for E = 0.61 MV/cm at 5 volts and E = 0.85 MV/cm at 7 volts. This test has an acceleration factor = 130 for the unprogrammed ViaLink element. The test results in *Table 10* show that no device has failed this stress in more than 220 million equivalent device hours. Four lots have 6000 hours of test which is equivalent to over 80 years of operation. The reliability stresses of the unprogrammed ViaLink for the 0.65 micron process was done on test structures where the ViaLink could be stressed independently from the CMOS.

Table 10. Results of High V_{CC} Static Life Test
(V_{CC} = 7.0V Static, Temp. = 25°C)

Package	Fab Lot	Device	Qty	Total Hrs	Failures	Equiv. Dev. Hrs
68PLCC	16558	7C382	14	3650	0	6.6E+06
68PLCC	18362	7C382	38	1907	0	9.4E+06
68PLCC	19194	7C382	110	1756	0	2.5E+06
68PLCC	19618	7C382	101	1464	0	1.9E+07
68PLCC	20454	7C382	100	2800	0	3.6E+07
68PLCC	34515	7C382	37	1000	0	4.8E+06
68PLCC	35421	7C382	36	1000	0	4.7E+06
68PLCC	35422	7C382	33	1000	0	4.3E+06

Table 10. Results of High V_{CC} Static Life Test (continued)
(V_{CC} = 7.0V Static, Temp. = 25°C)

Package	Fab Lot	Device	Qty	Total Hrs	Failures	Equiv. Dev. Hrs
68PLCC	33403	7C382A	100	1000	0	1.3E+07
68PLCC	34515	7C382A	36	6000	0	2.8E+07
68PLCC	35421	7C382A	34	6000	0	2.7E+07
68PLCC	35422	7C382A	36	6000	0	2.8E+07
TOTAL			675		0	2.2E+08

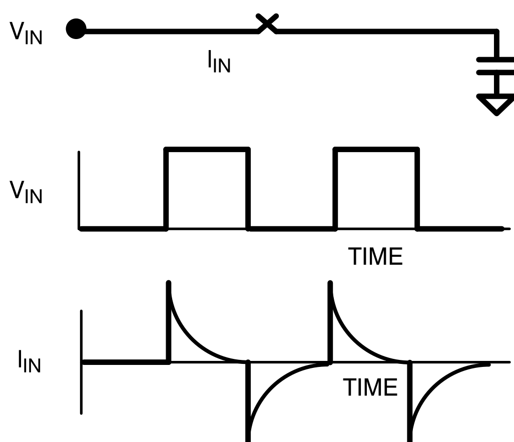

Figure 18. Switching of Programmed ViaLink Antifuse

Programmed ViaLink Element Reliability

The reliability tests on the programmed ViaLink element must demonstrate the stability of the link resistance in the programmed state. While an increase in resistance of the programmed device may not be catastrophic, a higher resistance can affect the device operating speed. Because the programmed ViaLink element has become part of the on-chip interconnect, reliability tests should be similar to those that are normally used to validate the integrity of metal interconnects.

In operation, the programmed ViaLink elements are subjected to capacitive switching current of the interconnect network. They do not experience any DC current or voltage (see *Figure 18*). Each switching pulse forces a capacitive charging current to flow through programmed ViaLink elements into the network on the rising edge, and an opposite, or discharging current, to flow on the falling edge. Each cycle is analogous to a read pulse for a memory device. A 10% change in resistance was set as the read disturb criteria for the ViaLink element. The typical impedance of a network is about 500Ω with the programmed ViaLink element contributing 50Ω. A 10% increase in the ViaLink resistance will increase the network impedance by approximately 5Ω, or 1%. This increase in resistance will increase a network delay in the pASIC380 device by about the same proportion.

Programmed ViaLink elements were stressed under severe capacitive currents. AC stresses rather than DC stresses were used to accelerate the failures for closer correlation with actual operation. The mean number of read cycles to disturb, N_{50}, for 25°C and 250°C were found to be identical. The absence of temperature dependence indicates an $E_a \cong 0$. *Figure 19* shows the acceleration of the read disturb at high AC current densities through the programmed ViaLink element. Thus, the number of cycles to disturb can be modeled as

$$N_{50} = N_0 \exp(-PJ) \qquad \text{Eq. 4}$$

where $N_0 = 7x10_{41}$ cycles is a constant, $P = 1.2\ cm^2/mA$ is the current density acceleration factor, and J is the peak AC current density through the link.

The pASIC380 is designed to operate at worst-case AC current density of $35x10^6\ A/cm^2$. The N_{50} for this condition is $4x10^{23}$ cycles. The failure rate can be calculated using the cumulative density F(t),

$$F(t) = \phi \ln [N/N_{50}/\sigma] \qquad \text{Eq. 5}$$

The failure distribution can be determined by plotting the data on a log normal probability scale versus the log of the number of cycles to failure (see *Figure 20*). The shape parameter, σ, is $\ln(N_{50}/N_{16})$ = 2.5. The shape parameter is relatively large because it includes the measurement tolerances of the current density.

High AC current density occurs at low frequencies where there is sufficient time for the network to be fully charged or discharged. At frequencies above 50 MHz, AC current through a ViaLink element decreases due to incomplete charging and discharging cycle. The worst-case pattern in a programmed pASIC380 has less than 150 ViaLink elements operating at $35x10^6\ A/cm^2$. Most of the programmed ViaLink elements operate at much lower current densities. Using *Equation 5*, the cumulative failure rate for the ViaLink element operating at $35x10^6\ A/cm^2$ for $1.6x10^{16}$ read cycles (equivalent to continuous operation at 50 MHz for 10 years) is less than 0.1 parts per million. The failure rate of the programmed ViaLink element contributes less than 0.01 FIT to the overall failure rate of the pASIC380 device.

Accelerate Stress Tests for Programmed ViaLink Elements

The low temperature operating life test stresses the pASIC380 devices with V_{CC} = 6.0 volts at 15MHz for 1000 hours at −55°C. The lack of an ambient temperature dependence on read disturb allow Cypress to stress at any temperature without changing the deprogramming cycle dependence. Cold temperature operation was chosen because it accelerates the stress by increasing the drive current of the CMOS devices. This test stresses the programmed ViaLink elements at $40x10^6\ A/cm^2$ for $5.4x10^{13}$ cycles. The acceleration factor, calculated from *Equation 4*, is 380. This test is equivalent to $2.0x10^{16}$ switching cycles, or continous operation under worst case condition at 50 MHz for 12 years at the worst case density of $35x10^6\ A/cm^2$. Over 1000 pASIC380 devices from 13 lots have been stressed. The failure criteria is the same as previously described, with emphasis placed on careful monitoring of AC performance. Test results in *Table 10* show that there have been no failure of the programmed ViaLink.

The Low Temperature Operating Life test stresses the programmed ViaLinks at $40x10^6\ A/cm^2$. The acceleration factor for

this test is 380. The results in *Table 10* show no failure on programmed ViaLink elements in over 110 million equivalent device hours. There were three failures unrelated to the ViaLink element. The first was a metal one to metal two short. The other two devices shorted when a power supply surged during the test.

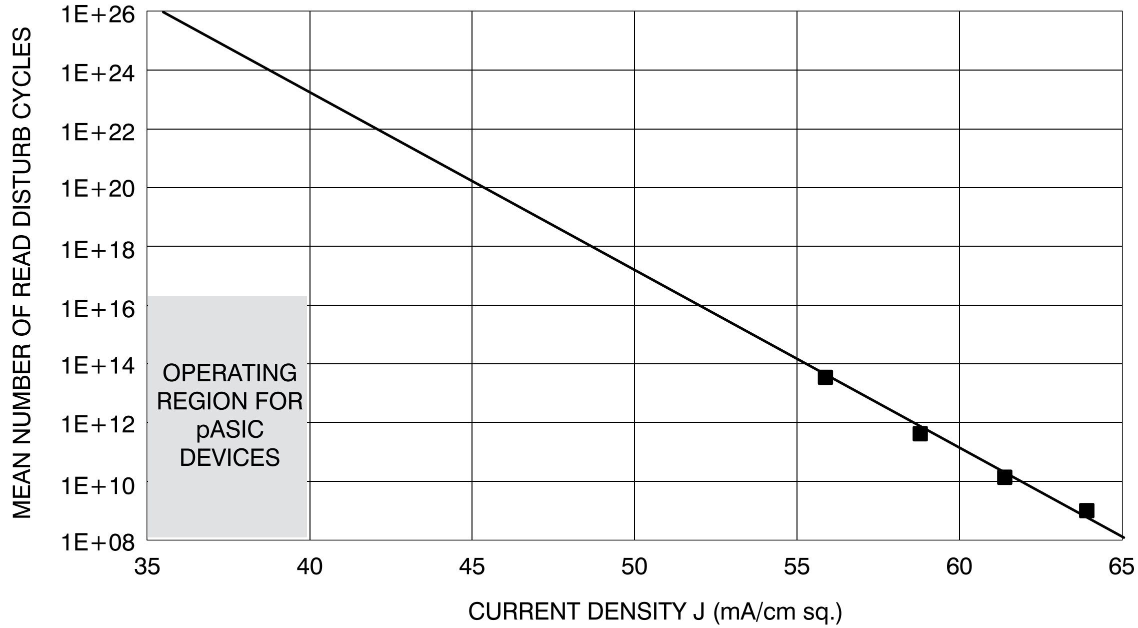

Figure 19. Acceleration of Read Disturb for Programmed ViaLink Element

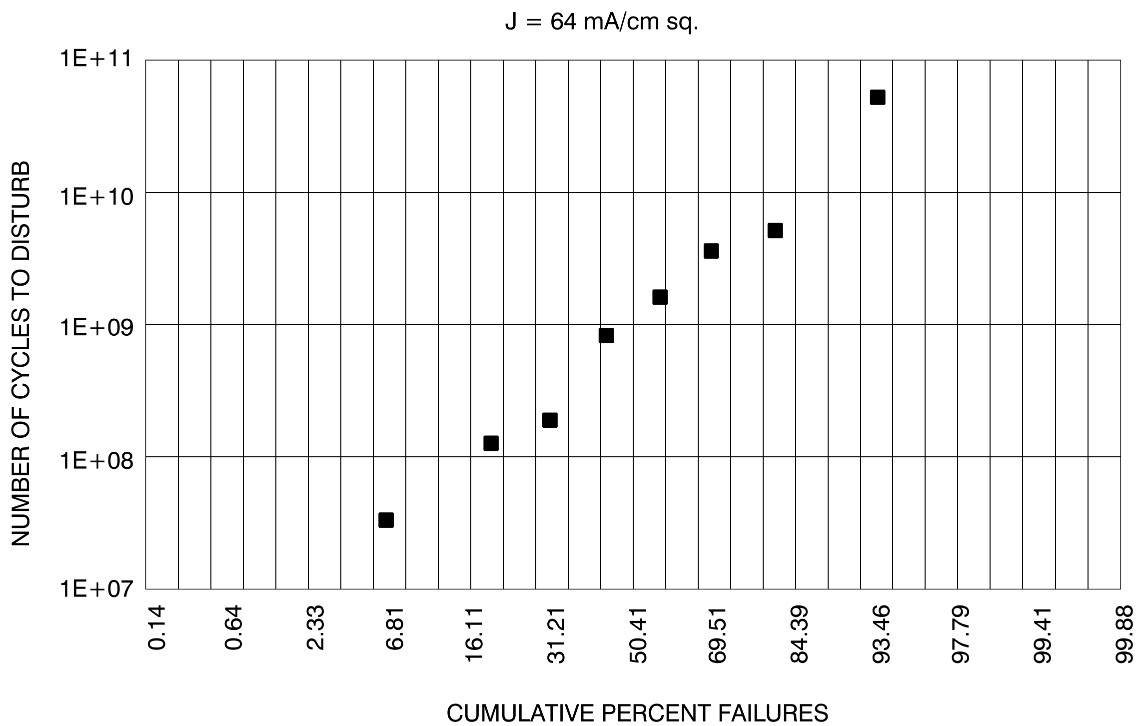

Figure 20. Distribution of Read Disturb on Programmed ViaLink Elements

Table 11. Results of Low Temperature Operating Life Test
(V_{CC} = 6.0V, Dynamic, f =15 MHz, Temp=−55˚C)

Package	Fab Lot	Device	Quantity	Failures @ Cycles		
				250	500	1,000
68PLCC	34267	7C382A	100	0	0	0
68PLCC	36128	7C382A	100	0	0	0
68PLCC	36129	7C382A	150	0	0	0
68PLCC	36934	7C382A	70	0	0	0
84PLCC	20762	7C384	100	0	0	0
84PLCC	22999	7C384	100	0	0	0
68PLCC	23001	7C384	100	1	0	0
84PLCC	36935	7C384	100	0	0	0
84PLCC	36936	7C384	100	2	0	0
84PLCC	38713	7C384	50	0	0	0
84PLCC	1323368	7C385A	4	0	0	0
84PLCC	1337713	7C385A	10	0	0	0
84PLCC	1337739	7C385A	20	0	0	0
84PLCC	1409353	7C385A	150	0	0	0
84PLCC	1409354	7C382A	150	0	0	0
84PLCC	1409390	7C382A	200	0	0	0
84PLCC	1409360	7C385A	40	0	0	0
84PLCC	1410389	7C385A	33	0	0	0
84PLCC	404333	7C385A	66	0	0	0
84PLCC	404788	7C385A	1	0	0	0
TOTAL			1604	3	0	0

Conclusion on Life Tests

The testing reported here establishes the reliability of pASIC380. No failures have been observed in 210 million equivalent device hours14 FITs and the failure rate with a 60% confidence is 19 FITs with no early life failures. The acceleration factors that can lead to the degradation of the programmed and unprogrammed ViaLink elements were studied. The pASIC380 devices are designed to operate at voltages and currents where the failure rate of the ViaLink element does not measurably increase the failure rate of the pASIC380 device above that of normal CMOS products.

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