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# PLD Programming Information

## Introduction

PLDs, or programmable logic devices, provide an attractive alternative to logic implemented with discrete devices. Cypress Semiconductor is in the enviable position of being able to offer PLDs in several different process technologies, thus assuring our customers of a wide range of options for leading-edge speed as well as very low power consumption. Cypress optimizes the mix of technology and device architecture to insure that the programmable logic requirements of today's highest-performance electronics systems can be fully supported by a single PLD vendor.

Cypress offers a wide variety of PLDs based on our leading-edge CMOS EPROM process technology. This technology facilitates the lowest power consumption and the highest logic density of any nonvolatile PLD technology on the market today, at speeds that are as fast as state-of-the-art bipolar technology would provide. Furthermore, these devices offer the user the option of device erasure and reprogrammability in windowed packages. Cypress also offers a number of PLDs based on our state-of-the-art BiCMOS and bipolar technologies. These PLDs are targeted at applications where power consumption and density are not as critical as leading-edge speed. Cypress offers PLDs based on CMOS Flash technology. The ViaLink™ Technology provides OTP FPGAs with high-speed and routability. Thus Cypress offers solutions for state-of-the-art systems regardless of what the optimal balance is between speed, power, and density for any particular system.

## Programmable Technology

### EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation, permanently turning off the transistor. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

### Two Transistor Cells

Cypress uses a two-transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor biasing it off.

### BiCMOS and Bipolar Process Technology

In addition to CMOS, Cypress offers BiCMOS TTL and bipolar ECL I/O-compatible PLDs. The BiCMOS devices offer the advantages of CMOS (high density and low power) and bipolar (high speed). Both the BiCMOS and bipolar devices are one-time fuse programmable. The fuses are Ti-W and are connected directly to first metal. First metal is a reliable composite of Ti-TiW-AlSi-Ti to ensure excellent electromigration resistance, eliminate contact spiking, and minimize hillocking.

### Flash Process Technology

The Flash cell is programmed in the same manner as the EPROM cell, and is electrically erased via Fowler-Nordheim tunneling. This next-generation PLD technology will combine a number of key advantages for future Cypress PLDs. The principal advantages will be leading-edge speed, low CMOS power consumption, and electrical alterability for simplified inventory management. In addition, Flash technology offers two inherent advantages for PLDs over the commonly used full-features EE CMOS technology. One is its superior migratability to higher logic densities, due to the smaller Flash cell size. The second is superior reliability, due to the Flash cell's higher immunity to voltage transients and the accompanying risk of data corruption.

### pASIC™ Process Technology

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In pASIC380 devices, the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values as low as 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

In a ViaLink programmable ASIC device, the two layers of metal are initially separated by an insulating semiconductor layer with resistance in excess of 1 gigaohm. A programming pulse of 10 to 12 volts applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers.

## Programming Algorithm—EPROM, BiCMOS and Flash Technology

### Byte Addressing and Programming

Most Cypress programmable logic devices are addressed and programmed on a byte or extended byte basis where an extended byte is a filed that is as wide as the output path of the device. Each device or family of devices has a unique address map that is available in the product datasheet. Each byte or extended byte is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a 1 or HIGH is placed on the input pin and a 0 or LOW is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A 1 or HIGH during program verify operation indicates an unprogrammed cell, while a 0 or LOW indicates that the cell accessed has been programmed.

### Blank Check

Before programming, all programmable logic devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a 1 or HIGH output indicates that the addressed

cell is unprogrammed, while a 0 or LOW indicates a programmed cell.

**Programming the Data Array**

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a read/write pin in the programming mode. This signal causes a write operation when switched to a supervoltage and a read operation when switched to a logic 0 or LOW. In the logic HIGH or 1 state, the device is in a program inhibit condition and the output pins are in a high-impedance state. During a write operation, the data on the output pins is written into the addressed array location. In a read operation, the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins and writing it into the addressed location. Verification of data is accomplished by examining the information on the output pins during a read operation.

The timing for actual programming is supplied in the unique programming specification for each device.

**Phantom Operating Modes**

All Cypress programmable logic devices on the EPROM and BiCMOS technology contain a Phantom array for post assembly testing. This array is accessed, programmed, and operated in a special Phantom mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the Phantom array is connected. In normal operation the Phantom array is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging and, if desired, by the user before programming and use. The Phantom modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific datasheets for details.

**Special Features**

Cypress programmable logic devices, depending on the device, have several special features. For example, the security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access. In advanced devices such as the PALC22V10, PLDC20G10, and CY7C330, the macrocells are programmable through the use of the architecture bits. This allows users to more effectively tailor the device architecture to their unique system requirements. Specific programming is detailed in the device datasheet.

## Programming Algorithm—pASIC380 Family

The metal interconnections of pASIC devices can be considered as a vertical and horizontal grid of metal lines. Both ends of the metal line grids are connected to internal shift registers which control the connection of the end of the wire to the programming voltage, ground, or an open. Non-contiguous wires are connected for programming purposes by pass transistors, which are also controlled by the shift registers.

Individual ViaLink fuses can be "addressed" by turning on various pass transistors and (from the shift registers) driving the wires that connect to both sides of the fuse to be programmed. Applying a programming voltage ($V_{PP}$) to the device, the shift register contents directs the voltage to the ViaLink fuse, which becomes programmed.

Once a fuse is programmed, it has shorted two wires of the wire grid. This can cause other fuses to become "unaddressable." For this reason, fuses must be programmed in a specific order. This ordering is determined by the development tool. Programming is achieved by loading the internal shift registers with the required data and then applying the programming pulse for the fuse(s) to be programmed. The programming pulse is required to meet specific timing and current limit specifications.

Entering the programming mode is accomplished by applying supervoltages on specific pins. The shift registers are accessed in a variety of modes which permit rapid programming as well as specific internal test features. These test modes allow complete testing of devices during manufacture.

The unprogrammed device has all internal logic cell input gates in the unconnected state. Consequently, applying $V_{CC}$ to an unprogrammed device will cause large currents to flow which can cause irreparable damage to the device. Under no circumstances should $V_{CC}$ be applied to an unprogrammed pASIC.

After the device is programmed, the test modes can also be used to verify the device programming. The development tools provide automatic test vector generation (ATVG). These vectors can be used with appropriately equipped programmers to provide post program testing.

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