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ADVANCED INFORMATION

Ultra338005

UltraLogic™ Very High Speed 5K Gate 3.3V CMOS FPGA

Features

- **Full 3.3V operation**
- **Very high speed**
  - **— Loadable counter frequencies greater than 100 MHz**
  - **— Chip-to-chip operating frequencies up to 85 MHz**
  - **— Input + logic cell + output delays under 7 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **— 20 x 16 array of 320 logic cells provides 15,000 total available gates**
  - **— 5,000 typically usable "gate array" gates**
- **Available in 84-pin PLCC, 144-pin TQFP, and 208-pin PQFP**
- **Fully PCI compliant inputs & outputs**
- **Low power, high output drive**
  - **— Standby current typically 100 μA**
  - **— 16-bit counter operating at 100 MHz consumes 25 mA**
- **Flexible logic cell architecture**
  - **— Wide fan-in (up to 14 input gates)**
  - **— Multiple outputs in each cell**
  - **— Very low cell propagation delay (1.4 ns typical)**
- **Robust routing resources**
  - **— Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **— No hand routing required**
- **148 bidirectional input/output pins**
- **4 dedicated input/high-drive pins**
- **4 fanout-independent low-skew clock nets**
  - **— 2 fast clocks driven from dedicated inputs**
  - **— 2 global clocks driven from any pin or internal logic**
- **Input registers**
  - **— Set-up time <2 ns**
- **Two primary clock/dedicated input pins with fanout-independent, low-skew nets**
  - **— Clock skew <0.5 ns**
- **Input hysteresis provides high noise immunity**
- **Full JTAG testability**
- **0.65μ triple layer metal CMOS process with ViaLink™ programming technology**
  - **— High-speed metal-to-metal link**
  - **— Non-volatile antifuse technology**
- **Powerful design tools—*Warp3*™**
  - **— Designs entered in VHDL, schematics, or mixed**
  - **— Fast, fully automatic place and route**
  - **— Waveform simulation with back annotated net delays**
  - **— PC and workstation platforms**
- **Extensive third party tools support**
  - **— See Development Systems section**

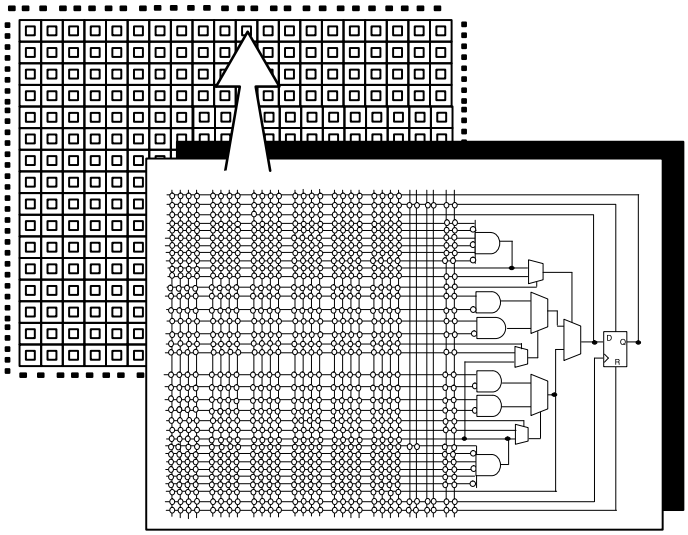
Functional Description

The Ultra338005 is a very high speed, 3.3V, CMOS, user-programmable ASIC device. The 320 logic cell field-programmable gate array (FPGA) offers 5,000 typically usable "gate array" gates. This is equivalent to 15,000 EPLD or LCA gates. The Ultra338005 is available in 84-pin PLCC, 144-pin TQFP, and 208-pin PQFP.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz with input delays under 4 ns and output delays under 5.5 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

For detailed information about the Ultra38000™ architecture, see the Ultra38000 Family datasheet.

Logic Block Diagram



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84, 144, and 208 PINS, 148 I/O CELLS, 4 INPUT HIGH DRIVE CELLS, 4 INPUT/CLK (HIGH DRIVE) CELLS

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