Ultra3800: October 13, 1995
Revision: October 25, 1995

PRELIMINARY

Ultra38000™ Family

UltraLogic™ Very High Speed CMOS FPGAs

Features

- **Very high speed**
  - **— Loadable counter frequencies greater than 185 MHz**
  - **— Data Path frequencies at greater than 200 MHz**
  - **— Chip-to-chip operating frequencies up to 135 MHz**
  - **— Input + logic cell + output delays under 5.5 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **— Density from 9,000 to 60,000 total available gates**
  - **— 3,000 to 20,000 typically usable "gate array" gates**
- **Fully PCI compliant inputs & outputs**
  - **— Full 33 MHz system performance**
- **Low power, high output drive**
  - **— Standby current typically 2 mA**
  - **— 16-bit counter operating at 100 MHz consumes 50 mA**
  - **— Minimum I_{OL} and I_{OH} of 24 mA**
- **Flexible logic cell architecture**
  - **— Wide fan-in (up to 16 input gates)**
  - **— Multiple outputs in each cell**
  - **— Very low cell propagation delay (1.4 ns typical)**
  - **— Fragments into five fine-grained functions for the worlds most efficient synthesis**
- **Robust routing resources**
  - **— Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **— No hand routing required**
- **Dedicated clock input pins with fan-out-independent low-skew clock nets**
  - **— Fast clocks driven from dedicated inputs**
  - **— Global clocks driven from dedicated inputs, any I/O pins or internal logic**
  - **— Clock skew < 0.5 ns**
- **Input registers**
  - **— Set-up time <2 ns**
- **Input hysteresis provides high noise immunity**
- **Full JTAG testability**
  - **— IEEE standard 1149.1.6**
- **0.65μ triple layer metal CMOS process with ViaLink™ programming technology**
  - **— High-speed metal-to-metal link**
  - **— Non-volatile antifuse technology**
- **Powerful design tools—*Warp3*™**
  - **— Designs entered in IEEE1164 VHDL, schematics, or mixed**
  - **— Fast, fully automatic place and route**
  - **— Waveform simulation with back annotated net delays**
  - **— PC and workstation platforms**

Functional Description

The Ultra38000™ Family of very-high-speed CMOS user-programmable ASIC devices is based on Cypress's ViaLink FPGA technology to combine high speed, high density, and low power in a single architecture.

All Ultra38000 Family devices are based on an array of highly flexible logic cells which have been optimized for efficient implementation of high-speed arithmetic, counter, datapath, state machine, random and glue logic functions. The logic cell was also designed to be fragmented into five fine-grained functions for the most efficient synthesis available. Logic cells are configured and interconnected by rows and columns of routing metal and ViaLink metal-to-metal programmable-via interconnect elements.

ViaLink technology provides a nonvolatile, permanently programmed customer logic function capable of operating at counter speeds of over 175 MHz. Internal logic cell nominal delays are under 2 ns and total input to output combinatorial delays are under 6 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors, while consuming a fraction of the power and board area of PAL, GAL, and discrete logic solutions.

Ultra38000 Family devices range in density from 3000 gates in an 84-pin package, to 20,000 gates in a 352-pin package. See *Table 1*. Devices share a common architecture to allow easy migration of designs from one density to another.

Designs are captured for the Ultra38000 using Cypress *Warp3* software or one of several third-party tools. See the Development Systems section for more information. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The Ultra38000 family features ample on-chip routing channels for fast, fully automatic place and route of 100% gate utilization designs.

Ultra3800 Family Members

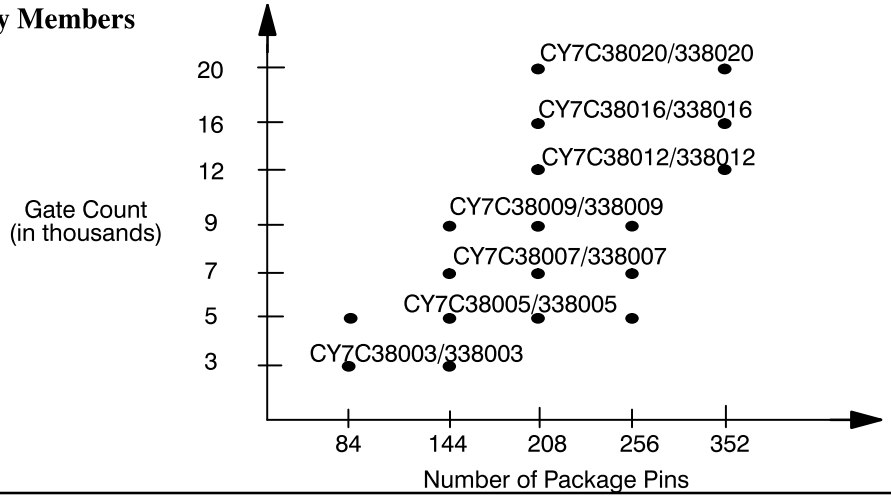

Table 1. Key Features of Ultra3800 Devices

Device	Logic Cells	I/O Cells	Usable Gates	Packages
CY7C38003 CY7C338003	192	120	3K	84 PLCC, 144 TQFP
CY7C38005 CY7C338005	320	156	5K	84 PLCC, 144 TQFP, 208 PQFP, 256 PBGA
CY7C38007 CY7C338007	480	192	7K	144 TQFP, 208 PQFP, 256 PBGA
CY7C38009 CY7C338009	672	228	9K	144 TQFP, 208 PQFP, 256 PBGA
CY7C38012 CY7C338012	896	264	12K	208 PQFP, 352 PBGA
CY7C38016 CY7C338016	1152	300	16K	208 PQFP, 352 PBGA
CY7C38020 CY7C338020	1440	336	20K	208 PQFP, 352 PBGA

Organization

The Ultra380000 Family of very-high-speed FPGAs contains devices covering a wide spectrum of I/O and density requirements. The seven members range from 3,000 gates in an 84-pin package to 20,000 gates in an 352-pin package and are shown in *Table 1.*

Device part numbers are derived from the usable gate count. Each of the internal logic cells has the logic capacity of more than 30 “gate array gates.” A typical application will use 12 to 15 gates from each logic cell.

ViaLink Programming Element

Programmable devices implement custom logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In Ultra38000 devices the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS gate array process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values below 50Ω. This is less than five percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of any programmed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

In a custom metal masked ASIC, such as a gate array, the top and bottom layers of metal make direct contact through the via. In an Ultra38000 FPGA, the two layers of metal are initially separated by an insulating silicon layer with resistance in excess of 1 gigaohm.

A programming voltage pulse applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers.

Cypress Ultra38000 devices are fabricated on a conventional high-volume CMOS gate array process. The base technology is a 0.65 micron, n-well CMOS technology with a single polysilicon layer and three layers of metal interconnect as shown in *Figure 1*. The only deviation from the standard process flow occurs when the ViaLink module is inserted between the metal deposition steps.

The size of a ViaLink via is identical to that of a standard metal interconnect via. Therefore the programmable elements can be packed very densely. The structure of *Figure 1* shows an array of

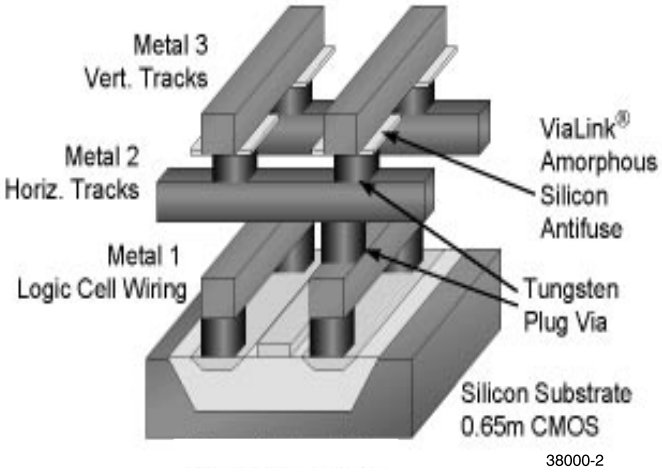

Figure 1. Three Layer Metal ViaLink Structure

ViaLink elements. The density is limited only by the minimum dimensions of the metal-line to metal-line pitch.

The Ultra38000 device architecture consists of an array of user-configurable logic building blocks, called logic cells, set in a grid of metal wiring channels similar to those of a gate array. Through ViaLink elements located at the wire intersections, the output of any cell may be programmed to connect to the input of any other cell.

This regular and orthogonal interconnect makes the Ultra38000 architecture similar in structure and performance to a metal masked gate array. It also makes system operating speed far less sensitive to partitioning and placement decisions, as minor revisions to a logic design result only in small changes in performance.

Adequate wiring resources permit 100% automatic placement and routing of designs using up to 100% of the logic cells. This has been demonstrated on designs that include a high percentage of fixed pin placements.

Ultra38000 Logic Cell

The Ultra38000 internal logic cell, shown in *Figure 3*, is a general purpose building block that can implement most TTL and gate array macro library functions. It has been optimized to maintain the inherent speed advantage of the ViaLink technology while ensuring maximum logic flexibility.

The complete Ultra38000 logic cell consists of two 6-input AND gates, four 2-input AND gates, six 2-to-1 multiplexers and one D flip-flip with asynchronous preset and clear controls. Each cell represents approximately 13 usable gate-equivalents of logic capacity. The total fan-in of the cell is 29 (including register control lines) and allows a wide range of functions with up to 16 simultaneous inputs. The high logic capacity and fan-in of the Ultra38000 logic cell accommodate many user functions with a single level of logic delay while other architectures require two or more levels of delay. Examples of combinatorial functions that can be implemented with a single logic cell: one 16-input AND gate, two 6-input AND gates plus two 4-input AND gates, two 6-input AND gates plus two 2:1 or one 4:1 multiplexers, one 5-input XOR gate, one 3-input XOR and one 2-input XOR, and numerous sum-of-products functions with up to 16 inputs or 16 product terms.

The multiplexer output feeds the D-type flip-flop which can also be configured to provide J-K, S-R, or T-type functions as well as count with carry-in. Two independent SET and RESET inputs can be used to asynchronously control the output condition. The combination of wide gating capability and a built-in sequential function makes the Ultra38000 logic cell particularly well suited to the design of high-speed state machines, shift registers, encoders, decoders, arbitration and arithmetic logic, as well as a wide variety of counters.

Figure 5 shows some of the possible configurations of the logic cell. Since all connections within the cell are hard-wired, the various functions are available in parallel. Thus very wide, complex functions are implemented with the same cell speed (about 2 ns) as the much smaller "fragment" functions. Related and unrelated functions can be packed into the same logic cell, increasing effective density and gate utilization.

This level of flexibility is especially important for designs synthesized from HDLs such as VHDL or Verilog. Typically, synthesis tools prefer "gate array-like" fine-grained architectures; however, fine-grained FPGA architectures generally yield very poor performance due to the long delays resulting from building functions with multiple levels of gates and slow interconnect elements. The Ultra38000 family gives logic synthesis tools the needed degrees of freedom for the high logic utilization benefits of a fine-grained architecture without sacrificing the high performance benefits of a large-grained, high fan-in architecture.

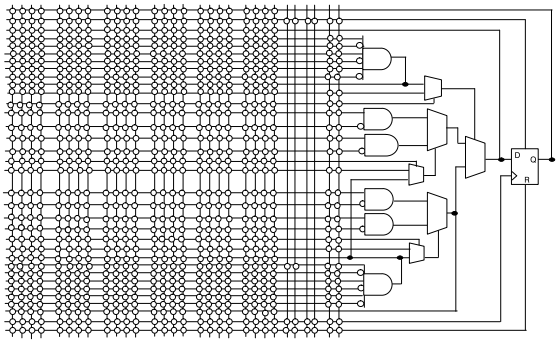

Figure 3. Logic Cell 38000-4

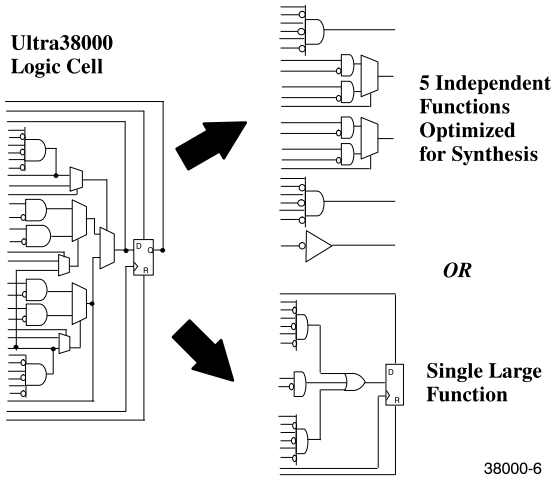

Figure 5. Logic Cell Fragmentation

The function of a logic cell is determined by the logic levels applied to the inputs of the AND gates. ViaLink sites located on signal wires tied to the gate inputs perform the dual role of configuring the logic function of a cell and establishing connections between cells.

A detailed understanding of the logic cell is therefore not necessary to design successfully with Ultra38000 devices. CAE tools will automatically translate a conventional logic schematic into a device and provide excellent performance and utilization.

I/O Cell

The Ultra38000 family features enhanced I/O cells with fast set-up time input registers featuring individually controlled synchronous clock enables. Each I/O pin has an individually controlled output enable signal as well. See *Figure* 7. All of the outputs are slew-controlled to minimize ground bounce, yet feature full PCI 2.1 output drive compliance. The family has a wide range of I/O counts available up to 336 for the largest device. Members of the family are available in multiple package types, including PLCC, TQFP, PQFP, and BGA. Different devices offered in the same packages are pin-compatible with each other, making it easy for designers who need more features to migrate to a higher density device.

Three types of input and output structures are provided on Ultra38000 devices to configure buffering functions at the external pads. They are the Bidirectional Input/Output (I/O) cell, the Dedicated Input (I) cell, and the Clock Input cell (I/CLK).

The bidirectional I/O cell consists of a 2-input OR gate connected to a pin buffer driver. The buffer output is controlled by a three-state enable line to allow the pad to also act as an input. The output may be configured as active HIGH, active LOW, or as an open drain inverting buffer.

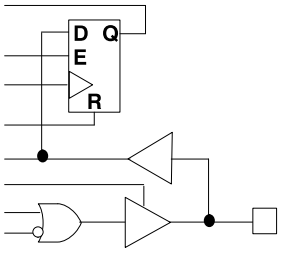

Figure 7. I/O Cell 38000-8

The output buffers (I_{OL}/I_{OH} of 24 mA) are designed to ensure quiet switching characteristics while maintaining high speed. Measured results show up to 48 outputs switching simultaneously into a 10 pF load with less than ±1 volt of output switching noise.

Routing Wires

Five types of signal wires are employed on the 3K, 5K, 7K, and 9K: segmented, dual, express, clock, and quad wires. A sixth wire type is added to the 12K, 16K, and 20K– the hex wire. Segmented wires are predominantly used for local connections and have a ViaLink element referred to as a cross link, at every intersection. They may also be connected to the segmented wires of cells above and below through ViaLink elements, called pass links. Express wires are similar to segmented wires except that they are not divided by pass links. Quad wires are similar to segmented wires in that they are employed for local interconnect, but instead of having pass links above and below each cell, they have pass links every fourth logic cell. The hex wire has pass links every six logic cells. This hierarchical routing structure is designed for optimal performance and density.

Dedicated Clock wires are lightly loaded with only three links per cell to distribute high-speed clock edges to the flip-flop CLK, SET, and RESET pins. Express wires may also be used to deliver clock signals into the multiplexer region of the cell for combinatorial gating.

Horizontal wiring channels provide connections via cross links to other columns of logic cells and to the periphery of the chip. Appropriate programming of ViaLink elements allows electrical connection to be made from any logic cell output to the input of any other logic or I/O cell. Ample wires are provided in the channels to permit automatic place and route of designs using up to 100% of the logic cells. Designs can be completed automatically even with a high percentage of fixed user placement of internal cells and pin locations.

The automatic place and route software allocates signals to the appropriate wire to ensure the optimum speed/density combination.

Reliability

The Ultra380000 Family is based on a 0.65-micron, high-volume CMOS fabrication process with the ViaLink programmable-via antifuse technology inserted between the metal deposition steps. Devices from this base CMOS process have been qualified to meet the requirements of MIL-STD-883D, Revision B.

The ViaLink element exists in one of the two states: a highly resistive unprogrammed, OFF, state and the low impedance, conductive, ON, state. It is connected between the output of one logic cell and inputs of other logic cell directly or through other links. No DC current flows through either a programmed or an unprogrammed link during operation as a logic device. An unprogrammed link sees a worst case voltage equal to V_{CC} biased across its terminals. A programmed link carries AC current caused by charging and discharging of device and interconnect capacitances during switching.

Studies of test structures and complete Ultra38000 devices have shown that an unprogrammed link under V_{CC} bias remains in the unprogrammed state over time. Similar tests on programmed links under current bias exhibit the same stability. These tests indicate that the long term reliability of the combined CMOS and ViaLink structure is similar to that of the base gate array process. See the Antifuse Reliability report for more information.

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