7c3807: Tuesday, July 25, 1995
Rev date: October 25, 1995

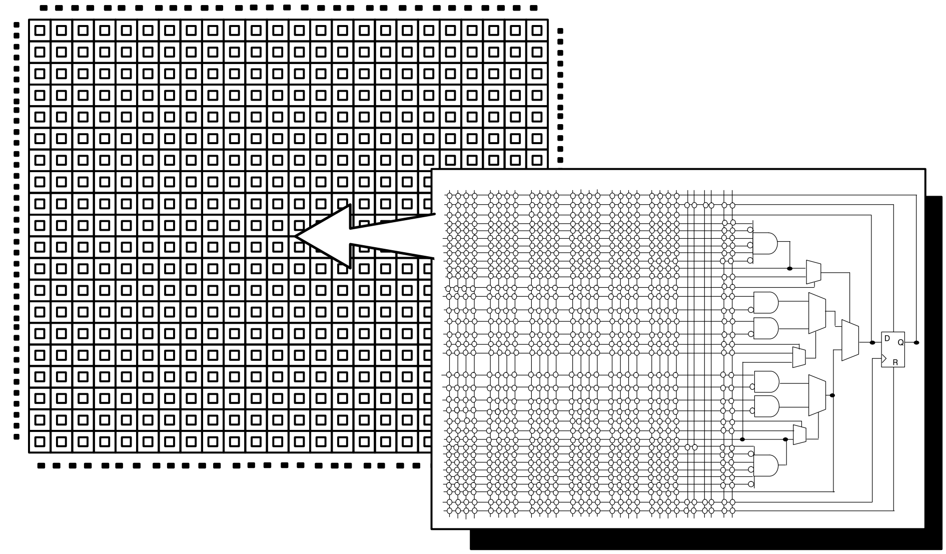
PRELIMINARY **Ultra38007**

UltraLogic™ Very High Speed 7K Gate CMOS FPGA

Features

- **Very high speed**
  - **— Loadable counter frequencies greater than 185 MHz**
  - **— Chip-to-chip operating frequencies up to 135 MHz**
  - **— Input + logic cell + output delays under 5.5 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **— 24 x 20 array of 480 logic cells provides 21,000 total available gates**
  - **— 7,000 typically usable “gate array” gates**
- **Available in 144-pin TQFP, 208-pin PQFP, and 256-pin BGA**
- **Fully PCI compliant inputs & outputs**
- **Low power, high output drive**
  - **— Standby current typically 2 mA**
  - **— 16-bit counter operating at 100 MHz consumes 50 mA**
  - **— Minimum I_{OL} and I_{OH} of 24 mA**
- **Flexible logic cell architecture**
  - **— Wide fan-in (up to 16 input gates)**
  - **— Multiple outputs in each cell**
  - **— Very low cell propagation delay (1.4 ns typical)**
- **Robust routing resources**
  - **— Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **— No hand routing required**
- **184 bidirectional input/output pins**
- **4 dedicated input/high-drive pins**
- **4 clock dedicated input pins with fan-out-independent low-skew clock nets**
  - **— 2 fast clocks driven from dedicated inputs**
  - **— 2 global clocks driven from dedicated inputs, any I/O pins or internal logic**
  - **— Clock skew < 0.5 ns**
- **Input registers**
  - **— Set-up time <2 ns**
- **Input hysteresis provides high noise immunity**
- **Full JTAG testability**
- **0.65µ triple layer metal CMOS process with ViaLink™ programming technology**
  - **— High-speed metal-to-metal link**
  - **— Non-volatile antifuse technology**
- **Powerful design tools—*Warp3*™**
  - **— Designs entered in IEEE1164 VHDL, schematics, or mixed**
  - **— Fast, fully automatic place and route**
  - **— Waveform simulation with back annotated net delays**
  - **— PC and workstation platforms**

Logic Block Diagram



256, 208, and 144 PINS, 184 I/O CELLS, 4 INPUT HIGH DRIVE CELLS, 4 INPUT/CLK (HIGH DRIVE) CELLS

7C38007-1

UltraLogic, *Warp3,* and Ultra3800 are trademarks of Cypress Semiconductor Corporation
ViaLink and pASIC are trademarks of QuickLogic Corporation.

Cypress Semiconductor Corporation • 3901 North First Street • San Jose • CA 95134 • 408−943−2600
October 1995

Functional Description

The Ultra38007 is a very high speed, CMOS, user-programmable ASIC device. The 480 logic cell field-programmable gate array (FPGA) offers 7,000 typically usable "gate array" gates. This is equivalent to 21,000 EPLD or LCA gates. The Ultra38007 is available in a 144-pin TQFP, 208-pin PQFP, and 256-pin BGA.

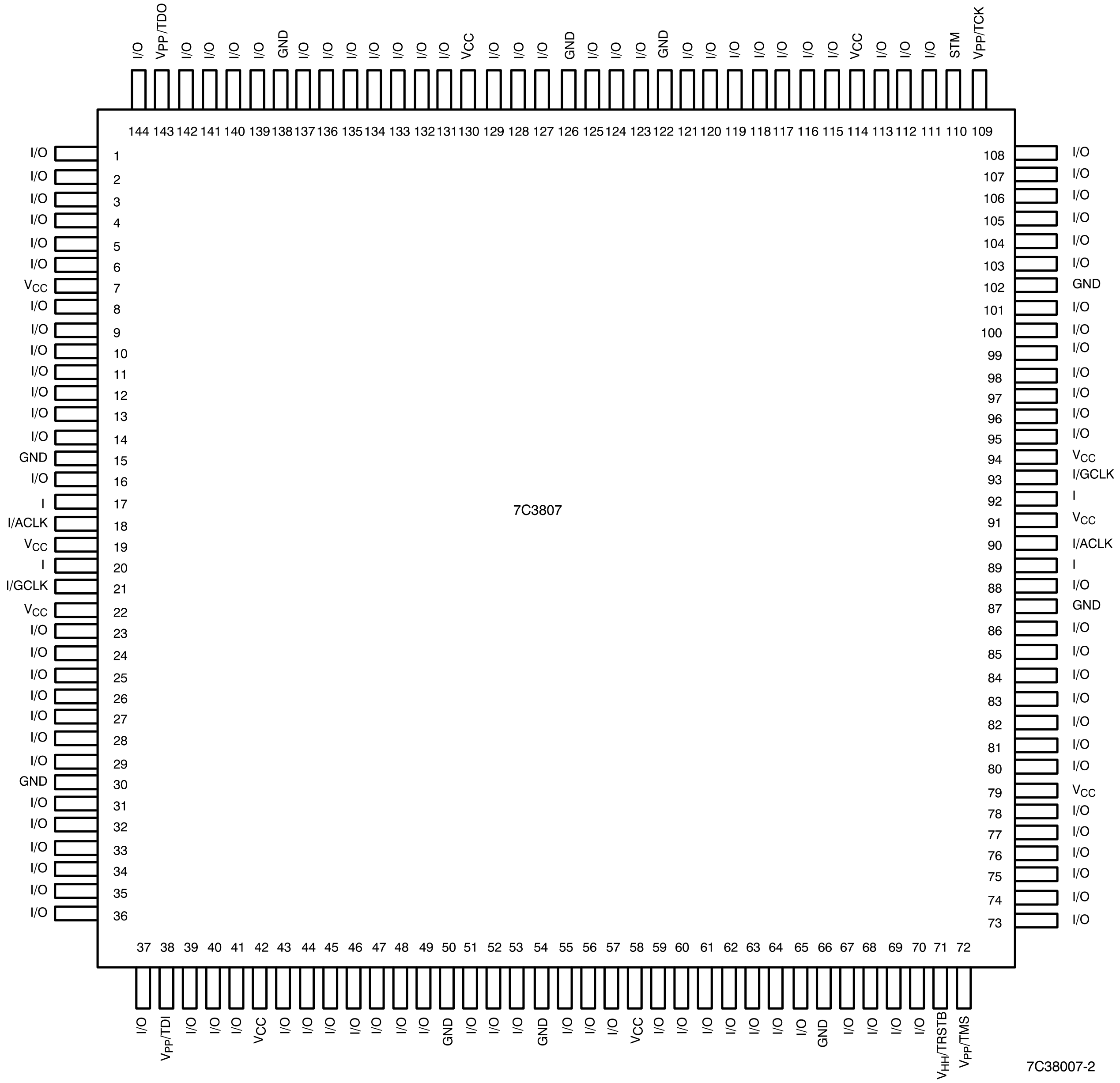
Low-impedance, metal-to-metal ViaLink™ interconnect technology provides non-volatile custom logic capable of operating at speeds above 185 MHz with input delays under 2 ns and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the Ultra38007 using Cypress *Warp3*™ software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The Ultra38007 features ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the Ultra3800™ architecture, see the Ultra3800 Family datasheet.

Pin Configurations

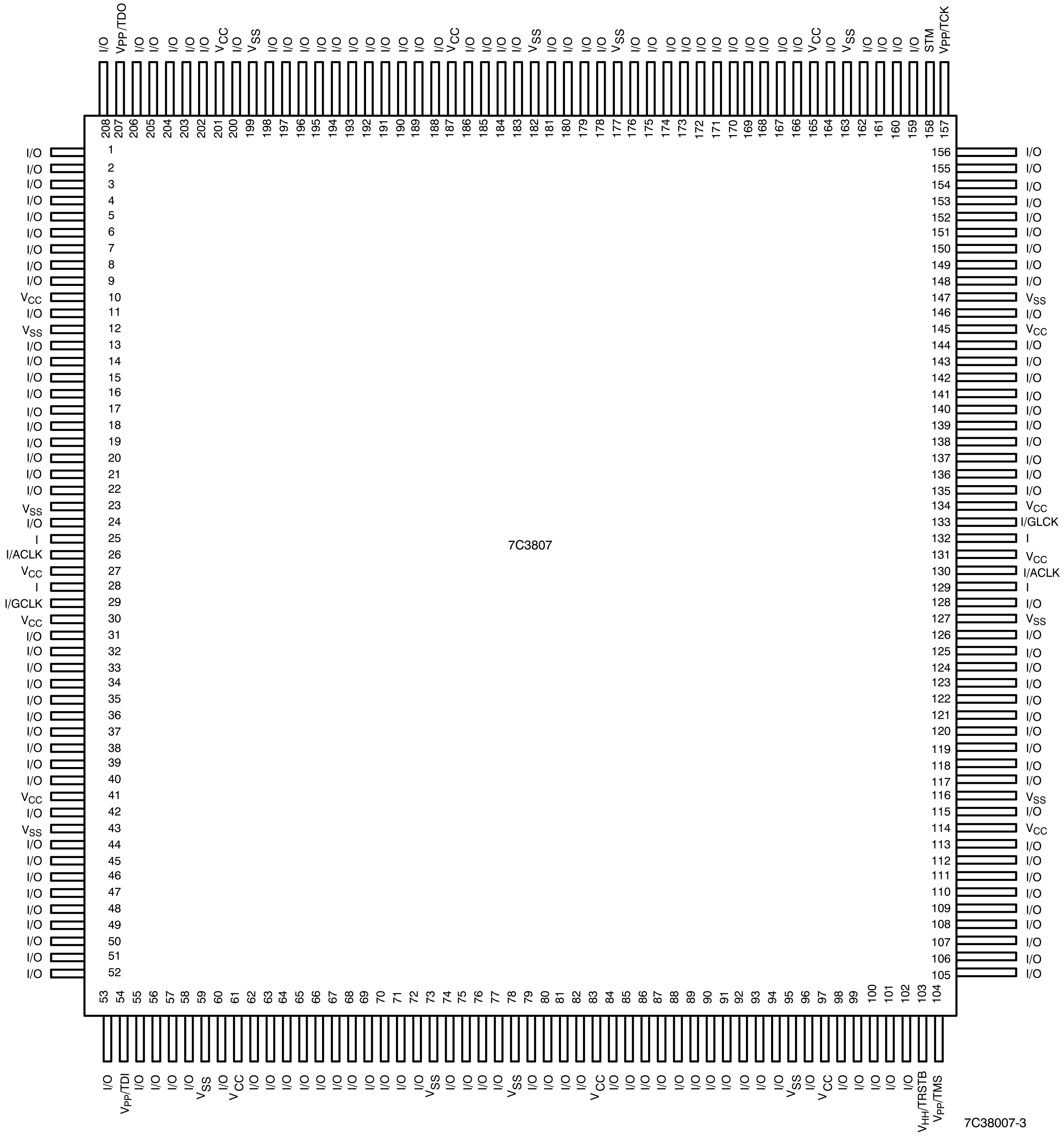
144-Pin Thin-Quad Flat Pack (TQFP)



7C38007-2

Pin Configurations (continued)

208-Pin Plastic Quad Flat Pack (PQFP)
Top View



7C38007-3

Pin Descriptions

Pins	Description
V_{PP}/TDI	A high voltage supply pin during programming. If JTAG is used, Test Data In. It should be held HIGH when it is not in JTAG mode.
V_{HH}/TRSTB	A high voltage pin during programming. Active low reset for JTAG. It must be held HIGH during normal operation.
V_{PP}/TMS	A high voltage supply pin during programming. Test mode select for JTAG. It should be held HIGH or LOW during normal operation.
V_{PP}/TCK	A high voltage supply pin during programming Test clock for JTAG. It should be held HIGH or LOW during normal operation.
STM	Must be grounded during normal operation.
V_{PP}/TDO	High voltage supply pin during programming. Test data out for JTAG. It should be held HIGH or LOW during normal operation.
I/ACLK	Can be configured as either an input or as the highest performance clock for the array.
I/GCLK	Can be configured as either an input, high-performance global clock (array input registers) or an output enable.
I	Input
I/O	Can be configured as an input and/or output.
V_{CC}	All power supply pins must be connected.
V_{SS}	All ground pins must be connected.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	
Ceramic	−65°C to +150°C
Plastic	−40°C to +125°C
Lead Temperature	300°C
Supply Voltage	−0.5V to +7.0V
Input Voltage	−0.5V to V_{CC} +0.5V
ESD Pad Protection	±2000 V
DC Input Voltage	−0.5V to 7.0V
Latch-Up Current	±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Commercial		Industrial	
	Min.	Max.	Min.	Max.
−X	0.46	2.55	0.4	2.75
−0	0.46	1.85	0.4	2.00
−1	0.46	1.50	0.4	1.60
−2	0.46	1.25	0.4	1.35

Shaded area contains advanced information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = +4.0 mA	3.7		V
		I_{OH} = 24.0 mA	2.4		V
		I_{OH} = − 10.0 μA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 24.0 mA		0.4	V
		I_{OL} = 10.0 μA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	− 10	+10	μA
I_{OZ}	Three-State Output Leakage Current	V_{IN} = V_{CC} or V_{SS}	− 10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{OUT} = V_{SS}	−10	− 90	mA
		V_{OUT} = V_{CC}	40	160	mA
I_{CC1}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Switching Characteristics (V_{CC}=5V, Ta=25°C, K = 1.00)

Parameter	Description	Propagation Delays[3] with Fanout of					Unit
		1	2	3	4	8	
LOGIC CELLS							
t_{PD}	Combinatorial Delay[4]	1.4	1.8	2.2	2.6	4.4	ns
t_{SU}	Set-Up Time[4]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	0.8	1.2	1.5	2.2	3.9	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.4	1.8	2.2	2.6	4.4	ns
t_{RESET}	Reset Delay	1.2	1.5	1.8	2.2	3.7	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Notes:

1. One output at a time. Duration should not exceed 30 seconds.
2. Capacitance is sample tested.
3. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
4. These limits are derived from worst-case values for a representative selection of the slowest paths through the Ultra38007 logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.

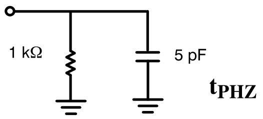
Switching Characteristics (V_{CC}=5V, Ta=25°C, K = 1.00) (continued)

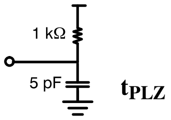
Parameter	Description	Propagation Delays[3] with Fanout of 1	2	3	4	8	10	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.5	2.6	2.6	2.7	3.5	4.1	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	2.6	2.7	2.8	2.9	3.7	4.2	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.1	1.5	1.8	2.4	3.8	4.6	ns
t_{ACK}[5]	Global Clock Buffer Delay[6]	2.2	2.3	2.3	2.4	2.5	2.6	ns
t_{CKHI}	Clock Buffer Min. HIGH[6]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{CKLO}	Clock Buffer Min. LOW[6]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKP}	Global Clock Pin Delay	1.2	1.2	1.2	1.2	1.2	1.2	ns
t_{GCKB}	Global Clock Buffer Delay	1.5	1.6	1.6	1.7	1.8	1.9	ns
t_{ISU}	Input register set-up time	1.0	1.0	1.0	1.0	1.0	1.0	ns
t_{IH}	Input register hold time	0.0	0.0	0.0	0.0	0.0	0.0	ns
t_{ICLK}	Input register clock to Q	0.8	1.2	1.5	2.1	3.5	4.3	ns
t_{IRESET}	Input register reset delay	0.7	1.1	1.4	2.0	3.4	4.2	ns
t_{IESU}	Input register clock enable set-up time	4.1	4.1	4.1	4.1	4.1	4.1	ns
t_{IEH}	Input resiger clock enable hold time	0.0	0.0	0.0	0.0	0.0	0.0	ns

Parameter	Description	Propagation Delays[3] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.3	3.8	4.3	5.4	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.6	4.5	5.3	6.9	ns
t_{PZH}	Output Delay Three-State to HIGH	2.1	2.6	3.1	3.7	4.8	ns
t_{PZL}	Output Delay Three-State to LOW	2.6	3.3	4.1	9.9	6.5	ns
t_{PHZ}	Output Delay HIGH to Three-State[7]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[7]	3.3					ns

Notes:

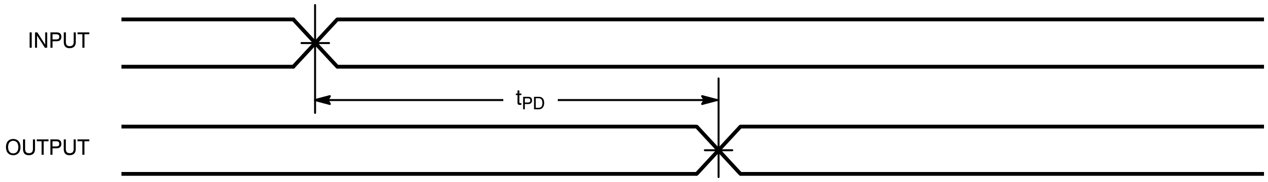
5. t_{ACK} include pin delay.
6. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock
7. The following loads are used for t_{PXZ}:buffer delay.





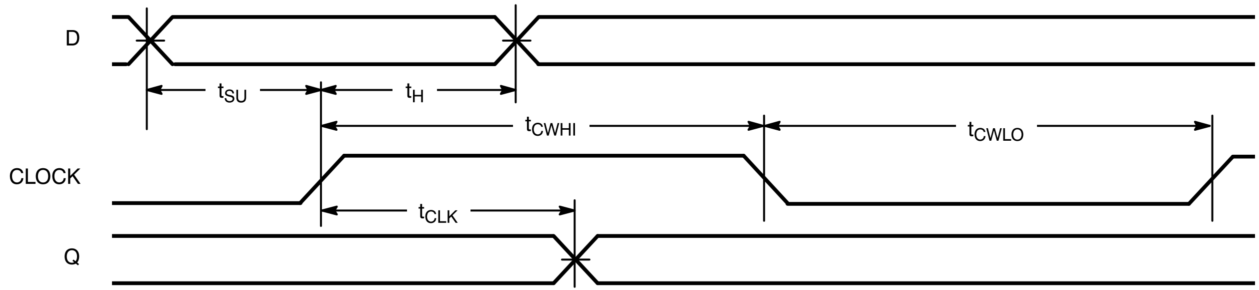
Switching Waveforms

Combinatorial Delay



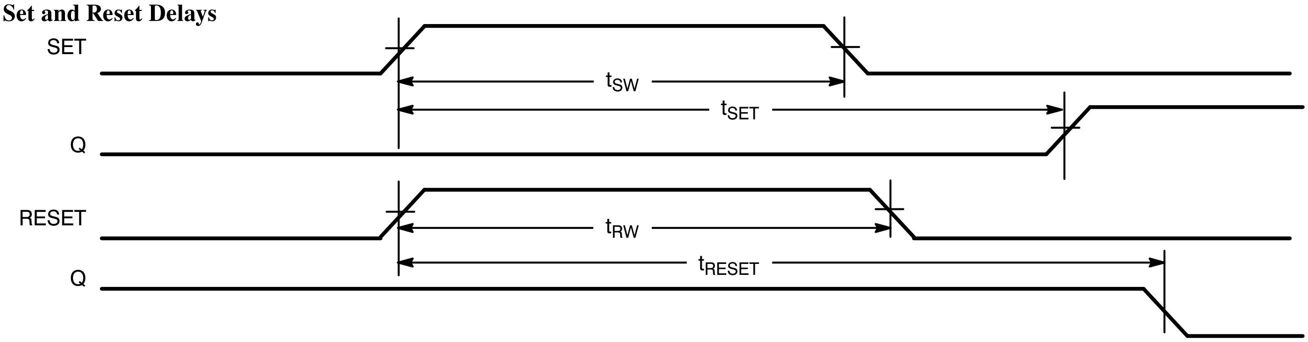
7C38007-4

Set-Up and Hold Times



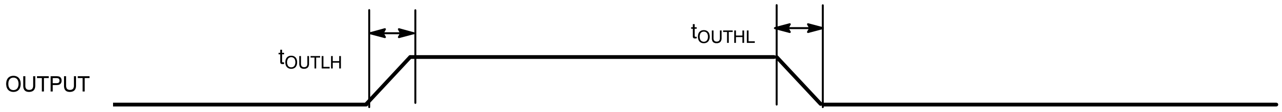
7C38007-5

Set and Reset Delays



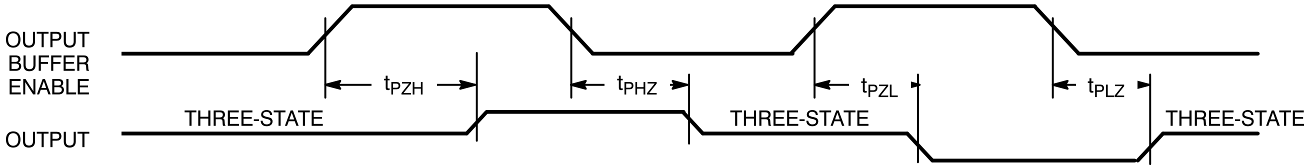
7C38007-6

Output Delay



7C38007-7

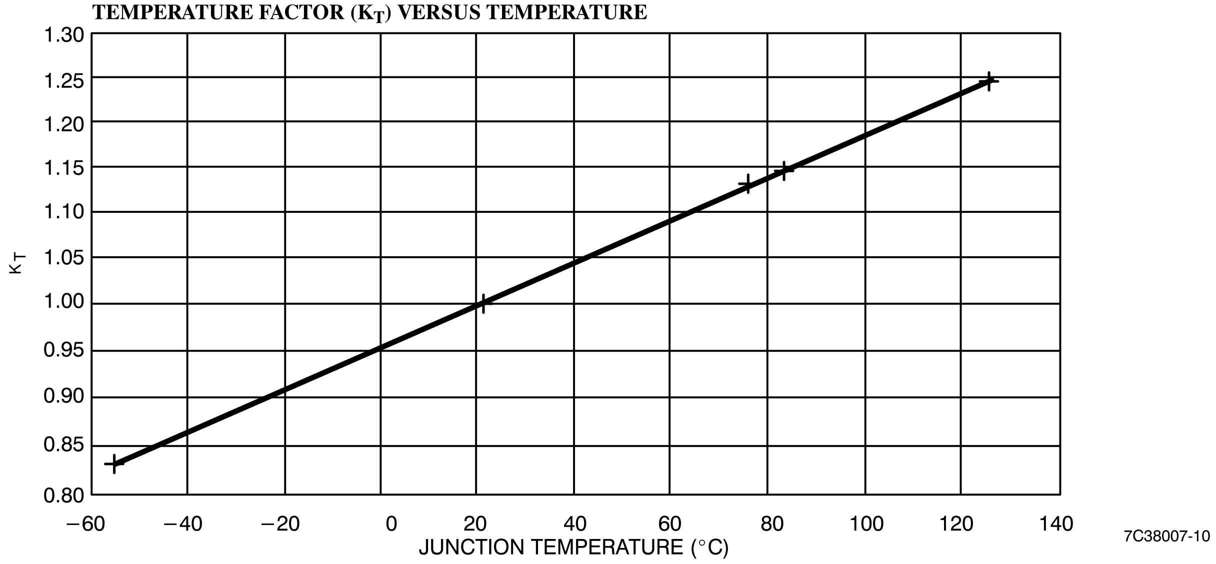
Three-State Delay



7C38007-8

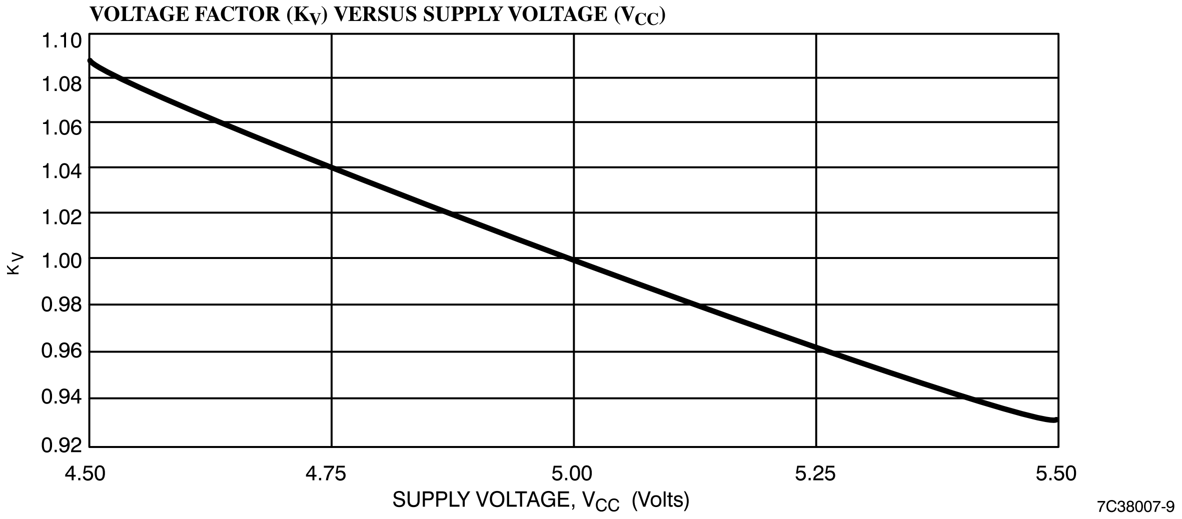
Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

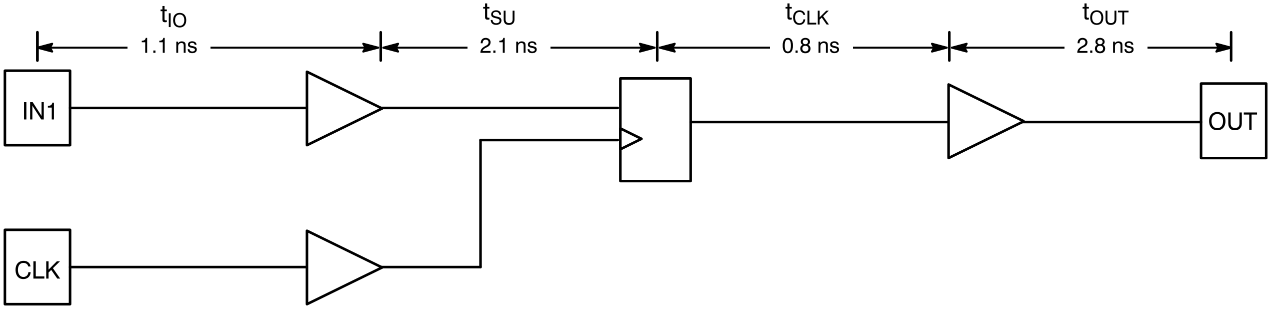


*THETA JA = 45 °C/WATT FOR PLCC

Sequential Delay Example using a



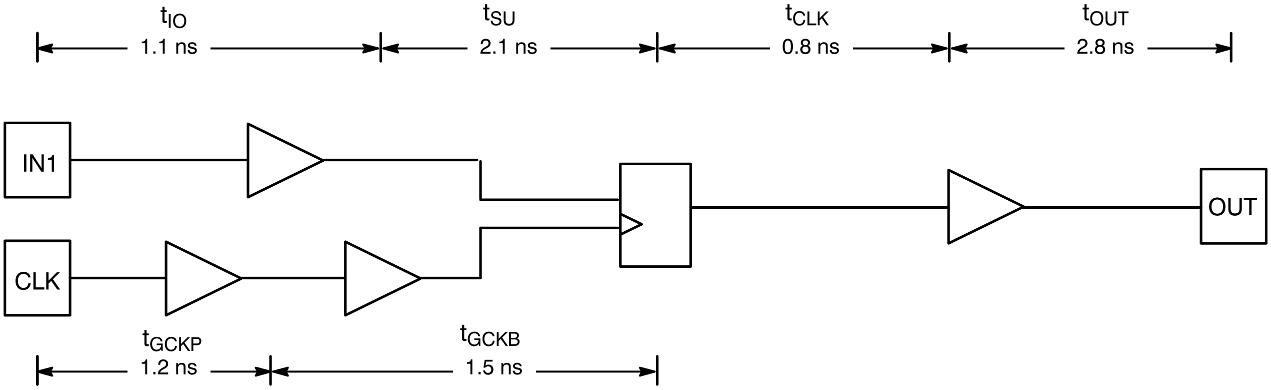
Sequential Delay Example Using Array Clock (Load = 30 pF, Fanout = 1, K = 1.0)



INPUT DELAY + REG SET-UP + CLOCK TO Q DELAY+ OUTPUT DELAY = 6.8 ns

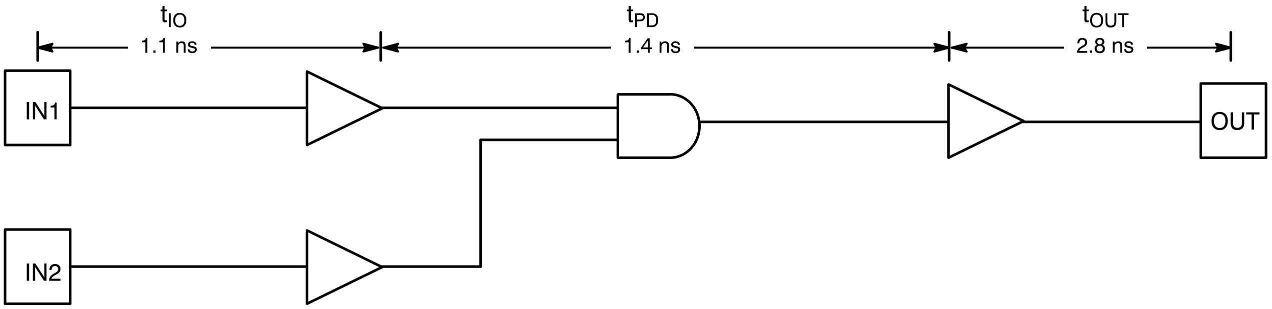
7C38007-11

Sequential Delay Example Using Global Clock (Load = 30 pF, Fanout = 1, K = 1.0)



7C38007-12

Combinatorial Delay Example (Load = 30 pF, Fanout = 1, K = 1.0)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.3 ns

7C38007-13

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY38007P144−2AC	A144	144-Pin Thin Plastic Quad Flat Pack	Commercial
	CY38007P144−2AI	A144	144-Pin Thin Plastic Quad Flat Pack	Industrial
	CY38007P256−2BGC	BG256	256-Pad Ball Grid Array	Commercial
	CY38007P208−2NC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY38007P208−2NI	N208	208-Pin Plastic Quad Flat Pack	Industrial
1	CY38007P144−1AC	A144	144-Pin Thin Plastic Quad Flat Pack	Commercial
	CY38007P144−1AI	A144	144-Pin Thin Plastic Quad Flat Pack	Industrial
	CY38007P256−1BGC	BG256	256-Pad Ball Grid Array	Commercial
	CY38007P208−1NC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY38007P208−1NI	N208	208-Pin Plastic Quad Flat Pack	Industrial
0	CY38007P144−0AC	A144	144-Pin Thin Plastic Quad Flat Pack	Commercial
	CY38007P144−0AI	A144	144-Pin Thin Plastic Quad Flat Pack	Industrial
	CY38007P256−0BGC	BG256	256-Pad Ball Grid Array	Commercial
	CY38007P208−0NC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY38007P208−0NI	N208	208-Pin Plastic Quad Flat Pack	Industrial
X	CY38007P144−XAC	A144	144-Pin Thin Plastic Quad Flat Pack	Commercial
	CY38007P144−XAI	A144	144-Pin Thin Plastic Quad Flat Pack	Commercial
	CY38007P256−XBGC	BG256	256-Pad Ball Grid Array	Industrial
	CY38007P208−XNC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY38007P208−XNI	N208	208-Pin Plastic Quad Flat Pack	Industrial

Shaded area contains advanced information.

Military Specifications
Group A Subgroup Testing

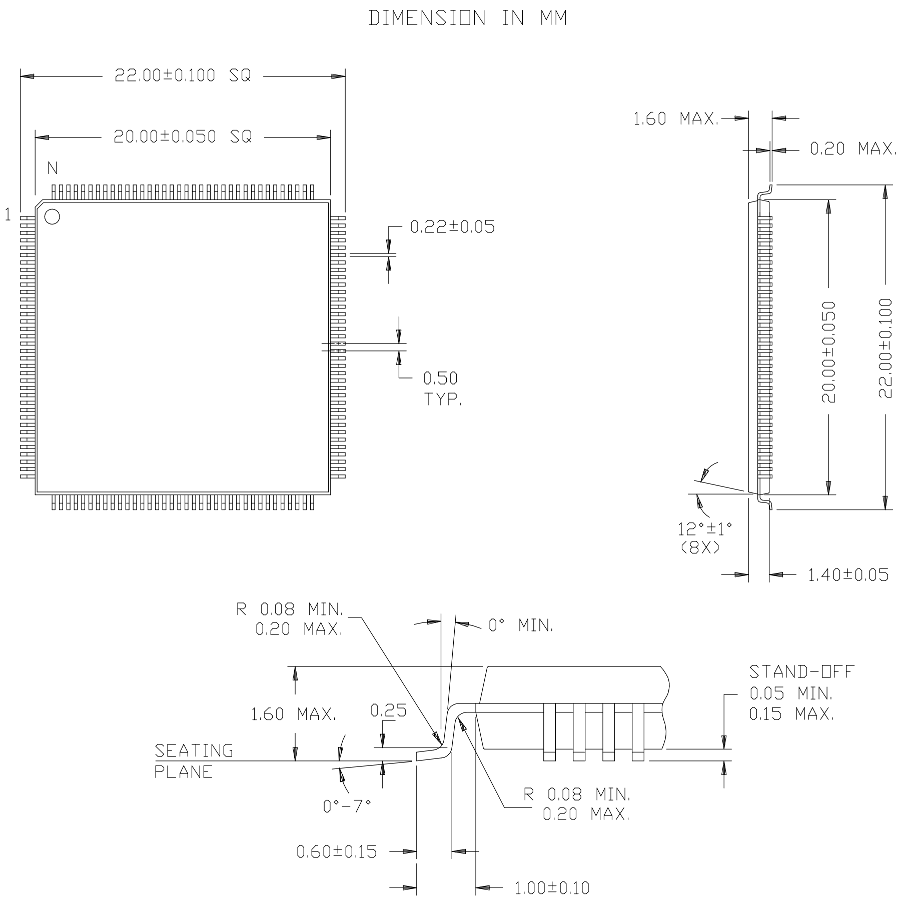
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Document #: 38−00429

Package Diagrams

144-Pin Thin Quad Flat Pack A144



Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208