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ADVANCED INFORMATION **Ultra39000™**

UltraLogic™ High-Density CPLD Family

Features

- **High density**
  - **— 192−512 macrocells**
  - **— 64−224 I/O pins**
  - **— Multiple input/clock pins**
- **High performance**
  - **— 125−100 MHz performance**
  - **— 10−12 ns t_{PD}**
  - **— 5−6 ns t_S**
  - **— 5.5−6.5 ns t_{CO}**
- **In-System Reprogrammable (ISR™)**
- **Fast CMOS technology**
- **Fully PCI compliant**
- **Full JTAG compatibility**
- **3.3V or 5V operation**
- **Programmable speed/power options**
- **Simple timing model**
- **No hidden delays**
- **Packages**
  - **— 84 to 304 pins**
  - **— PLCC, TQFP, and PQFP**
- **Programmable security bit**
- ***Warp3*™ CAE development system**
  - **— VHDL input**
  - **— ViewLogic™ graphical user interface**
  - **— Schematic capture (ViewDraw™)**
  - **— Available on Sun, HP, and Windows™ platforms**
- ***Warp2*™/*Warp2+*™ VHDL Compiler**
  - **— VHDL input**
  - **— Functional simulator**
  - **— Available on Sun, HP, and Windows platforms**

Functional Description

The Ultra39000™ family of high-density, high-performance Complex Programmable Logic Devices (CPLDs) provide an in-system reprogrammable solution complete with full Joint Test Action Group (JTAG IEEE1149.1) compatability. Each member of the Ultra39000 Family of fast, reconfigurable CPLDs has been designed to bring the high performance and the ease of use of 22V10s to ultra high-density PLDs. And since they are designed and fabricated with Cypress's state-of-the-art electrically-alterable Flash technology, users can program the devices in-circuit, which simplifies both the development and manufacturing processes. This, in turn, speeds time to market and reduces product inventory costs. The entire family will operate at 3.3V or 5V and is fully compliant with the PCI Local Bus Specification. It will operate with speeds of up to 125 MHz.

All of the macrocells in each of the Ultra39000 Family members are distributed among a number of distinct logic blocks. For example the Ultra39192 has 12 logic blocks, while the Ultra39512 has 32. Each logic block contains 16 macrocells along with a product term array and a fast, intelligent product term matrix. Each logic block in the Ultra39000 architecture is connected through a Programmable Interconnect that produces extremely fast and predictable paths through the device

All members of the Ultra39000 Family feature an abundant number of I/O resources with 64 to 224 I/O pins as well as four dedicated inputs/clocks and provide both fast synchronous and asynchronous clocking capabilities. Each member is also both upwardly and downwardly pin-compatible with the other family members, providing a built-in upgrade path.

Additionally, the Ultra39000 Family features a programmable speed/power option that allows users to optimize designs for either ultra-fast performance or ultra-low power. The family also provides slew rate control for each of the outputs that reduces switching noise. And finally, the Ultra39000 Family features a very simple timing model that results in parameters that are not dependent on the device resources utilized or the type of application being implemented.

Development support for the entire family of Cypress Programmable Logic Devices including Ultra39000 is provided through all of Cypress's state-of-the-art VHDL-based tools as well as a vast array of third party solutions. *Warp3* is a sophisticated design tool based on ViewLogic's CAE design environment, which integrates Cypress's IEEE1164-compliant VHDL synthesis engine, full schematic capture capability (ViewDraw™), a VHDL waveform simulator, VHDL debugger, and a full-function timing simulator. This integrated tool features mixed-mode entry allowing designs to be entered textually, schematically, or in a combination of both. It is supported on PCs running Windows, and on Sun and Hewlett Packard workstations. In addition, both *Warp2* and *Warp2+* are low-cost VHDL compilers offering VHDL synthesis capability and a functional simulator. See the separate software and third party data sheets for further information.

Ultra39000 Selection Guide

Device	Macrocells	Pin Count	Max. I/O Pins	f_{MAX} (MHz)	t_{PD} (ns)	ts (ns)	t_{CO} (ns)
39192	192	84/160	64/128	125	10	5	5.5
39256	256	160/208	128/160	125	10	5	5.5
39320	320	208/240	160/192	125	10	5	5.5
39384	384	240	192	100	12	6	6.5
39448	448	240/304	192/224	100	12	6	6.5
39512	512	304	224	100	12	6	6.5

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