**CMOS TECHNOLOGY**

**Author Name- Sneha P. Funde, Saloni Charde- AVBIT, PAWANAR.**

Piyush C. Kulkarni-SDCOE, SELUKATE, WARDHA

Abstract: **Complementary metal–oxide–semiconductor** (**CMOS**). CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS).[[1]](http://www.rediffmail.com/cgi-bin/red.cgi?red=http%3A%2F%2Fen%2Ewikipedia%2Eorg%2Fwiki%2FCMOS%23cite%5Fnote%2D1&isImage=0&BlockImage=0&rediffng=0) Integrating circuits are constructed using this technology. Now this is technical edge we use microprocessor, microcontroller, static RAM etc. more often. This device is also use this CMOS technology. In communication field also CMOS Technology play important role as well.CMOS technology firstly patented by “Frank Wanlass” in 1967. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. CMOS technology is also used in analog applications. CMOS operational amplifier ICs available in the market. CMOS technology is also widely used for RF circuits all the way to microwave frequencies, in mixed-signal (analog+digital) applications.

Keywords: CMOS,Semiconductor, Ic

**1. Introduction**

The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. High noise immunity and low static power consumption are two important characteristics of CMOS devices. CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes [3]. CMOS circuits use a combination of p-channel and n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates.[4]

**2. Introduction (Background)**

**CMOS Technology:**

Indispensible for our human society.All the human activities are controlled by CMOS living, production, financing, telecommunication,transportation, medical care, education,entertainment, etc.

**Without CMOS**:

World economical activities immediately stop. Cellarer phone dose not exists..Advantages are more in CMOS. Using this we are continuing towards invention of new advance aged. Basic of this CMOS Technology coved in this paper.

**Why CMOS Technology?**

 Comparison  of  BJT and MOSFET technology from an analog viewpoint:

Feature                                                     BJT                                                                   MOSFET

Cutoff Frequency(*fT*)                             100 GHz                                                     50 GHz (0.25μm)

Noise (thermal about the same)              Less 1/f                                                             More 1/f

DC Range of Operation                  9 decades of exponential                                 2-3 decades of square law

                                                             current versus *vBE*                                                behavior

Small Signal Output Resistance           Slightly larger                                             Smaller for short channel

Switch Implementation                                  Poor                                                                 Good

Capacitor Implementation                       Voltage dependent                                             Reasonably good

Therefore,

• Almost every comparison favors the BJT, *however* a similar comparison made from a digital viewpoint would come up on the side of CMOS.

• Therefore, since large-volume technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

Other factors:

• The potential for technology improvement for CMOS is greater than for BJT

• Performance generally increases with decreasing channel length

**BASIC CMOS TECHNOLOGY**

**FUNDAMENTAL PROCESSING STEPS:**

**Basic steps**

• Oxide growth

• Thermal diffusion

• Ion implantation

• Deposition

• Etching

• Epitaxy

**Photolithography**

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

**Oxidation**

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

**Diffusion**

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

**Ion Implantation**

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

**Deposition**

Deposition is the means by which various materials are deposited on the silicon wafer.

**Etching**

Etching is the process of selectively removing a layer of material.

**Epitaxy**

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

The complexity of a process can be measured in the terms of the number of masking

steps or masks required to implement the process.

• Major CMOS Processing Steps:

1.) Well definition

2.) Definition of active areas and substrate/well contacts (SiNi3)

3.) Thick field oxide (FOX)

4.) Thin field oxide and polysilicon

5.) Diffusion of the source and drains (includes the LDD)

6.) Dielectric layer/Contacts

7.) Metallization

8.) Dielectric layer/Vias

9.) Metallization

10.) Passivation

11.) Bond pad openings

CMOS technology has a reasonably good lateral BJT, Other considerations in CMOS technology include:

Latch-up

ESD protection

Temperature influence

Noise influence

• Design rules are used to preserve the integrity of the technology

**3. Previous Work (Literature Survey)**

 From the rigorous review of related work and published literature, it is observed that many researchers have designed Phase Locked Loop (PLL) by applying different techniques like analog and digital simulation applying mathematical/logical relations. Researchers have undertaken different systems, processes or phenomena with regard to design and analyze PLL and attempted to find the unknown parameters. Since in the real world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing PLL with CMOS/VLSI technology. From the continuous survey it is observed that foundry of technology and supply voltage range is continuously decreases with the advancement of technology. Phase-lock loop with 0.35- m CMOS technology at a supply voltage of 1.8 V has been designed in 2002.Chen and Sheen presented a phase-locked loop for clock generation that consists of a phase/frequency detector, charge pump, loop filter, range-programmable voltage-controlled ring oscillator, and programmable divider. Circuits as having low power dissipation, is widely adopted. The modified phase detector and charge pump have been extensively used to enhance the performance of the PLL. By applying the TSMC 0.35- m CMOS technology, the proposed phase-locked loop that uses the power-switch scheme can yield clock signals ranging from 103 MHz to 1.02 GHz at a supply voltage of 1.8 V. Moreover, power dissipation that is proportional to the number of paralleled inverter rings is measured with 1.32 to 4.59 mW. By using the TSMC 0.35- m CMOS technology, the designed PLL using the power-switch scheme can generate clock

frequencies ranging from 103 MHz to 1.02 GHz with a power dissipation ranging from 1.32 to 4.59 mW, at a supply voltage of 1.8 V.

**4. RESULTS and discussion**

Using CMOS today we have latest “electronics” available for living advanced lifestyles. This is actually get possible because of silicon revaluation in electronics. And now more efficient and reliable technology we have with us that is CMOS.

**5. CONCLUSIONS**

Electronics is usually depends upon semiconductor and electronics circuits. CMOS Belongs to SEMICONDUCTOR technology and using this type of technology we can archive highest peak of accuracy, low cost, and advance technology.

**6. ACKNOWLEDGEMENTS**

  We would like to thank my H.O.D. Sujay Surekha sir, Prof. Miss.Manisha Waghamare. and my friends whose great support gave me courage to present our work in National Level Conference.

**7 References**

**[1]** *COS-MOS* was an RCA trademark, which forced other manufacturers to find another name —CMOS

 **[2]** [Intel 45nm Hi-k Silicon Technology](http://www.rediffmail.com/cgi-bin/red.cgi?red=http%3A%2F%2Fwww%2Eintel%2Ecom%2Ftechnology%2F45nm%2Findex%2Ehtm&isImage=0&BlockImage=0&rediffng=0)

**[3]** Baker, R. Jacob (2008). *CMOS: circuit design, layout, and simulation* (Second ed.). Wiley-IEEE. p. xxix. [ISBN](http://www.rediffmail.com/cgi-bin/red.cgi?red=http%3A%2F%2Fen%2Ewikipedia%2Eorg%2Fwiki%2FInternational%5FStandard%5FBook%5FNumber&isImage=0&BlockImage=0&rediffng=0) [978-0-470-22941-5](http://www.rediffmail.com/cgi-bin/red.cgi?red=http%3A%2F%2Fen%2Ewikipedia%2Eorg%2Fwiki%2FSpecial%3ABookSources%2F978%2D0%2D470%2D22941%2D5&isImage=0&BlockImage=0&rediffng=0).

**[4]** P.E.Allon-2002-CMOS Analog circuit Design