**IMPLEMENTATION AND SIMULATION OF MULTIPLIER USING VEDIC MATHEMATICS**

Amey Makhe, Rajlaxmi Mukherjee, Rohini Padole, Mayur Tekade

Department of Electronics Engineering

K D K College of Engineering, Nagpur

Email Id’s- [ameymakhe1806@gmail.com](mailto:ameymakhe1806@gmail.com)

[Mukherjee.rajkrishna@gmail.com](mailto:Mukherjee.rajkrishna@gmail.com)

**ABSTRACT:**

Vedic mathematics is the ancient methodology of Indian mathematics which has a unique technique of calculations based on 16 sutras (formulae) .The idea for designing the multiplier and adder/subtractor unit is adopted from ancient Indian mathematics “Vedas”. On account of those formulas, the partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB. The work has proved the efficiency of Urdhva Triyakbhyam– Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels. Urdhva Tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of numbers. In this paper, a 4 X 4 binary multiplier is designed using this sutra. This multiplier can be used in applications such as digital signal processing, encryption and decryption algorithms in cryptography, and in other logical computations. This design is simulated using VHDL.