

TRAFFIC DENSITY CONTROL WITH SWITCHING SYSTEM

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Abstract – Traffic management is the critical issue of the road. These traffic lights are not capable to count the number of vehicles and the priority of the vehicles on Traffic. The vehicles like Ambulance and Fire Brigade are also struggles in traffic and waste their valuable time. The purpose of the system provides quality of service to Emergency vehicles using DTMF and GSM Technology

Keywords- DTMF, GSM, embedded system

I. INTRODUCTION

This particular project is designed for the cities with heavy traffic and emergency services. In Mumbai the roads are full jammed every time. Most of the time the traffic will be at least for 50meters .In this distance the traffics police and public can't hear the siren form the ambulance. Then the ambulance has to wait till the traffic is cleared. Some times to free the traffic it takes at least 15 minutes .So by this time anything can happen to the patient .So this project avoid these disadvantages.

I. INTRODUCTION TO FRONT-END

This project is design for any critical issue happed

On traffic or road. If any emergency on the road then the traffic police or anyone can press the switch which is placed on traffic, when the switch is pressed then the circuit will be on the call and message transfer to the nearest hospital and police station. Then the ambulance will move towards the destination. In that case due to heavy traffic ambulance will faces many traffic problems on the way. this system can help to the ambulance to reach the destination as early as possible . the ambulance driver or any person can easily control the traffic signal by the mobile. And reach to the destination point within a time and save the life.

A. WORKING / LOGIC

GSM is one of the upcoming technologies and is used in this project too. It possesses a smart modem which easily combines with embedded systems methodology. Once this system is implemented using GSM, remote Access is obtained. The CM8870/70C decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

II. FEATURES AND INTERFACING

Features of GSM kit:-

- *This GSM modem is a highly flexible plug and play quad band GSM modem*
- *integration to RS232*
- *Use AC – DC Power Adaptor with following ratings*
- *DC Voltage : 12V /1A*
- *Current Consumption in normal operation 250mA, can rise up to 1Amp while transmission.*
- *Supports features like Voice, Data/Fax, SMS, GPRS and integrated TCP/IP stack.*

Features of 89c51

- 128x8 internal ram
- Two 16 bit timer/counter
- Six interrupt source
- 32 programable i/o lines

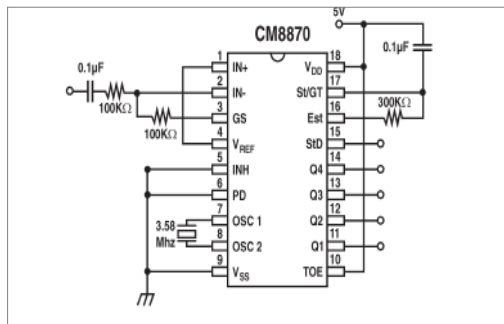
Features of DTMF

- Full dtmf receiver
- Less than 35mW power consumption
- Uses quartz crystal or ceramic resonator
- Power down mode

Interfacing:-

- RS-232 through D-TYPE 9 pin connector,USB.
- Serial port baud rate adjustable 1200 to115200 bps.
- BRK connector for MIC & SPK, SIM card holder.
- Power supply through DC socket.
- LED status of GSM / GPRS module

II. DATASHEETS



F _{LOW}	F _{HIGH}	KEY	TOW	Q ₄	Q ₃	Q ₂	Q ₁
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1209	0	H	1	0	1	0
941	1336	.	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = Logic Low, H = Logic High, Z = High Impedance

Functional Description

The CAMD CM8870/70C DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC, or 20-pin PLCC package configuration. The CM8870/70C's internal architecture consists of a bandsplit filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency

and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high gain comparators. These comparators are provided with a Hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The CM8870/70C decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver

checks for a valid signal duration (referred to as "characterrecognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes VC (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (tGTP), VC reaches the threshold (VTSt) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch.

At this point, the GT output is activated and drives VC to VDD. GT continues to drive high as long as ESt remains high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as

rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \gg 0.67 RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μ F is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guardtimes for tone-present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure.

Input Configuration

The input arrangement of the CM8870/70C provides a differential input operational amplifier as well as a bias source (VREF) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 1, with the op-amp connected for unity gain and VREF biasing the input at $\frac{1}{2} V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

Clock Circuit

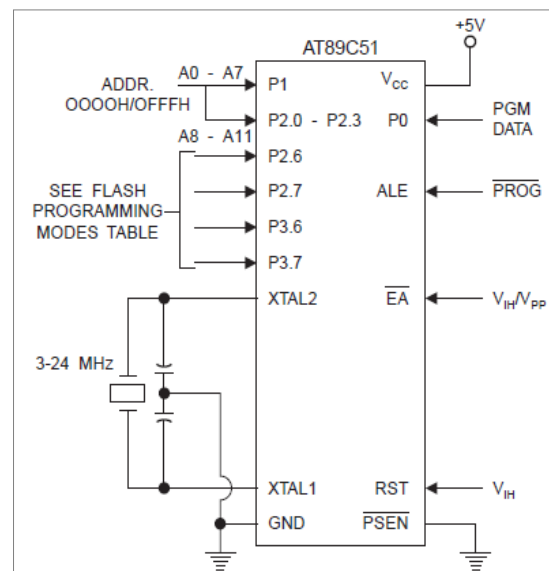
The internal clock circuit is completed with the addition of a standard television color burst crystal or ceramic resonator having a resonant frequency of 3.579545 MHz. The CM8870C in a PLCC package has a buffered oscillator output (OSC3) that can be used to drive clock inputs of other devices such as a microprocessor or other CM887X's as shown in Figure 7. Multiple CM8870/70Cs can be connected as shown in figure 8 such that only one crystal or resonator is required.

89C51:-

The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes.

The Idle Mode

stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 may also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pullups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being

pulled low will source current (IIL) because of the pullups. Port 3 also serves the functions of various special features of the AT89C51 as listed below: Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on chip peripherals remain active. The mode is invoked by Software. The content of the on-chip RAM and all the special functions registers remain unchanged during this Mode. The idle mode can be terminated by any enabled Interrupt or by hardware reset. It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

The aim of this project is

- ▲ Time saving as well as life saving,
- ▲ Easy to use
- ▲ Provided the quality of services

This Project can be used in industries, traffic signals, and Highway's etc.

As a conclusion of our project we declare that our project has been completed successfully and working properly as per problem definition. During the project many problems occurred but using some proper logic those problem are solved.

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