" Design and implementation of five level inverter for reducing THD using PWM "

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***Abstract*- The multilevel inverter utilization has been increased since the last decade. Cascaded H-bridge multilevel inverter is one of the popular converter topologies used in high power medium voltage application. These new type of inverters are suitable in various high voltage and high power applications also due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. This paper presents five level cascaded H-bridge multilevel inverter, using multicarrier pulse width modulation technique. And also comparison is made between multicarrier pulse width modulation and the embedded MATLAB function. The Simulation results are presented to prove that THD is reduced with the multicarrier modulation. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.**

***Keywords*- THD-Total Hormonic Distortion, DF-Distortion Factor.**

I.INTRODUCTION

Demand for high-voltage, high power converters capable of producing high-quality waveforms while utilizing low voltage devices and reduced switching frequencies has led to the multilevel inverter development with regard to semiconductor power switch voltage limits. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.[1] The most attractive features of multilevel inverters are as follows:-

1) They can generate output voltages with extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion.
3) They generate smaller common mode (CM) voltage, thus reducing the stress in the motor. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4) They can operate with a lower switching frequency.

The multilevel inverter has been implemented in various applications ranging from medium to high-power levels, such as motor drives, power conditioning devices, also

conventional or renewable energy generation and distribution. The different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitor multilevel inverter.[2] Among the three topologies, the cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity, a feature that enables the inverter to continue operating at lower power levels after cell failure. Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high-voltage applications. The cascaded multilevel inverter typically comprises several identical single phase H-bridge cells cascaded in series at its output side.[2] This configuration is commonly referred to as a cascaded H-bridge, which can be classified as symmetrical if the dc bus voltages are equal in all the series power cells, or as asymmetrical if otherwise. In an asymmetrical CHB, dc voltages are varied to produce more output levels. In this paper , we are using two modulations , one is the multicarrier phase shifted modulation and other is the embedded MATLAB function and THD level is compared.

II. LITERATURE SURVEY

This paper proposes a multilevel voltage source inverter has been recognized as an important alternative to the normal two level voltage source inverter, especially in high power application. Using multilevel technique, the output voltage amplitude is increased, switching devices stress is reduced and the overall harmonics profile is improved. Three presentable topologies can be considered for multilevel inverter (MLI): diode –clamped, flying capacitor and cascaded H- bridge cells with separate dc sources. This paper focuses on cascaded multilevel inverter. For the cascaded multilevel inverter variety of modulation strategies have been reported, with the most popular being carrier – based and space vector modulation (SVM). This paper investigates and analyses

different multicarrier PWM methods for a five – level cascaded inverter using PSIM simulation. Multicarrier PWM methods can be categorized into two groups: Carrier Disposition methods (CD) and Phase- shifted (PS) PWM methods. [1]

This paper proposed as multilevel inverter is idea for connecting such distributed dc energy sources (solar and fuel cells in addition to rectified output of wind turbines) to a power grid. Multilevel Pulse Width Modulation (PWM) inverters have been gained importance in high performance power applications without requiring high ratings on individual devices. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. In the present paper we introduce a power circuit for single phase five level inverter which contains a very lower number of switches and the technique for the generation of required signals to control the operation of the inverter switches.[2]

This paper introduces a multilevel inverters which are power converter systems composed by an array of power semiconductors sources that when properly connected and controlled can generate a multistep voltage waveform with variable and controllable frequency, phase and amplitude. This study deals a nine level inverter system with different types of loads; the voltage source inverters(VSI) are modeled and simulated using MATLAB simulink and the result are presented. The test results verify the effectiveness of the proposed strategy in terms of computational efficiency as well as the capability of the inverter to produce very low distorted voltage with low switching losses. This research aims to extend the knowledge about the performance of different clamped multilevel inverter through harmonics analysis.[3]

This paper presents a micro controller based control of multilevel inverter for single phase Induction motor. IGBT is used as power element. Pulse width modulation techniques (PWM), introduced three decades ago, are the most used methods to control the voltage and frequency supplied to electrical AC machines. This work proposes a new switching scheme for the cascaded H-Bridge multilevel inverter. Unlike other schemes, the proposed method is based on the symmetric regular sampling PWM with a single carrier and multiple modulating signals. On-transcendental trigonometric equations that define the switching instants of the multilevel inverter are derived . This algorithm is implemented by a low-cost fixed-point microcontroller on an experimental five level cascaded inverter test-rig. Multilevel inverter has gained attention in recent years due to its high power capability associated with lower output harmonics. Several multilevel topologies have been reported in the literature and this paper focuses on asymmetric cascaded PWM technique.[4]

In this paper mainly focused on the design and implementation of new topology in a single phase five level. cascaded H-bridge multilevel inverter by using only a five switches and two DC power source. The main objective of this paper is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit. The main merit of the new topology is to reduce the lower total harmonic distortion, lower electromagnetic interference generation and high output voltage. In this paper, various carrier pulse width modulation techniques are proposed, which can minimize the total harmonic distortion and enhances the output voltages from proposed work of five level inverter.[5]

III. PRPOSED DESIGN AND STRUCTURE OF THE MULTILEVEL INVERTER

A Signal is supplied from single phase grid. It consists of a diode rectifier, DC link filter and an inverter. The rectifier converts supply AC voltage into DC voltage. The DC voltage is filtered by a capacitor in the DC link. The inverter converts the DC to variable voltage, The rectifier section of an block, called the front end, is responsible for generating current harmonics into the power supply system. Therefore, to reduce the total harmonic distortion (THD) of phase current it is necessary to add additional capacitors.

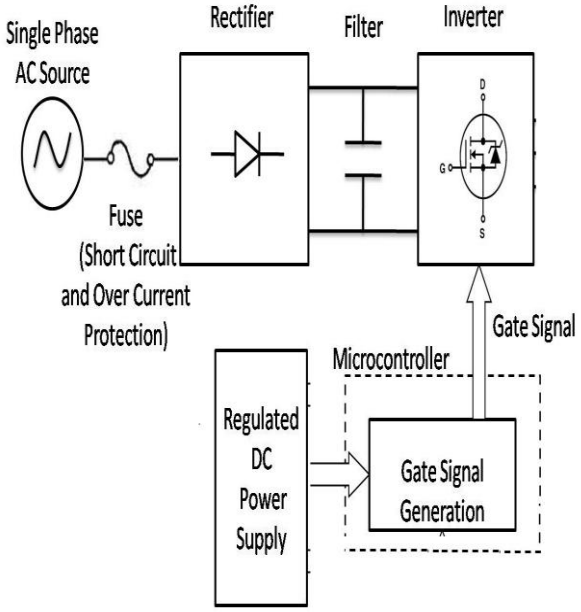

Fig1-Block diagram of Multilevel inverter

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs. Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. The multilevel inverter structures are the main focus of discussion however, the illustrated structures can be implemented for rectifying operation as well. Although each type of multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Operation and structure of some important type of multilevel converters are discussed in the following sections.[3] For multilevel inverter realization we have to use multicarrier Sine PWM technique. In that technique multiple carrier signals of different magnitude are compared with a single modulating sinusoidal signal. A simple formula used for determination of number of carrier (n_c) required is calculated with number of level of voltage (n_1) required is:

- $n_{c=} n_1$-1

So to realize five level inverter, it requires four carrier signals. The amplitude of the four carrier signals is divided in four equal parts of unity.

IV. PROPOSED CONTROL STRATEGY

Cascaded inverter (VSI)

The constant DC voltage by rectifier is delivered the to the input of inverter which fed to controlled transistor switches, converts this voltage to single-phase AC voltage signal with wide range variable voltage amplitude and frequency. This work reports a newly-constructed single-phase multilevel inverter topology that produces a significant reduction in the number of power devices required to implement multilevel output for Distributed Energy resources (DER). The studied inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and THD. Simulation results show the effectiveness of the proposed solution.

Microcontroller Block

This paper focuses on cascaded H-bridge multilevel inverter built to implement the proposed conduction table with five voltage levels. Gating signals are generated using AVR microcontroller. The performance of the inverter has been analyzed and compared with the result obtained from theory. A scheme based on 5-level PWM inverter, which control a high performance 8-bit standard microcontroller with gate driver circuit and additional hardware is used, which allows a referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches

flexible and economical solution. The output voltage can be varied in a large range and with a good resolution.

Regulated Power Supply

For running the microcontroller block fluently, it will need the good regulated 5 V DC power, hence it has got the equal importance in this cascaded multilevel inverter.

V. MULTI-LEVEL TOPOLOGY

Conventional cascaded H-bridge multilevel inverter Fig.2 shows a five level cascaded H-bridge multilevel inverter. The converter consists of two series connected H-bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The output voltage is given by V=V1 +V2. Such a technique is used for analysis of harmonic of output of Three Level Inverter. Here in this analysis has included with resistive load and with RL load Inverter.FFT analysis gives Magnitude of Output Voltage and % Total Harmonic Distortion. Between the capacitors of each inverter, the rotated switching scheme using fundamental frequency switching is used, where the switching patterns are rotated every cycle. The use of reactive loads and power electronics converter based AC/DC drives in industry has drawn nonsinusoidal and non-periodic current from the distribution power system.

$$\mathrm{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}}{V_1}$$

VI. SIMULATION IMPLEMENTATION

Simulation model of a Cascade Connected H Bridge Five Level Inverter is shown in Fig.2. Vs1 and Vs2 are two DC sources, R is a load branch and A1 to A4 & B1 to B4 are eight switches whose switching pattern has been explained. Figure 3 represents the simulation model for the firing of the switches using Pulse Generator. Figure 9 represents the simulation model of a Cascade Connected H Bridge Five Level Inverter using Sinusoidal PWM Technique

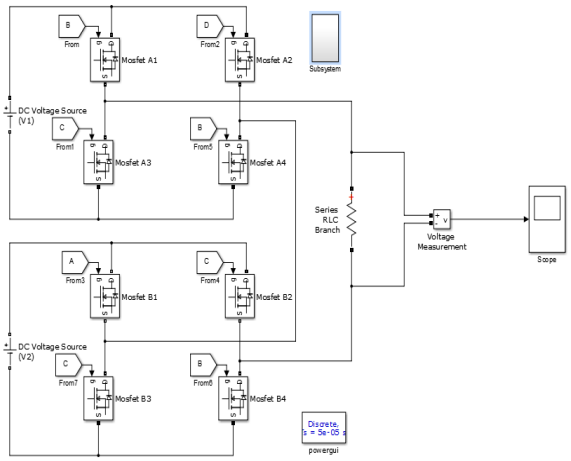

Fig 2. Single-phase 5-level Cascade bridge multilevel inverter

Three different topologies have been proposed for multilevel inverters as diode-clamped (neutral clamped), capacitor-Clamped (flying capacitors) and cascaded multi cell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: Multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination and space-vector modulation (SVM).It can generate output voltage with extremely low distortion. It draws input current with very low distortion. It generates smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, by using sophisticated modulation methods, CM voltages can be eliminated. They can operate with a lower switching frequency.

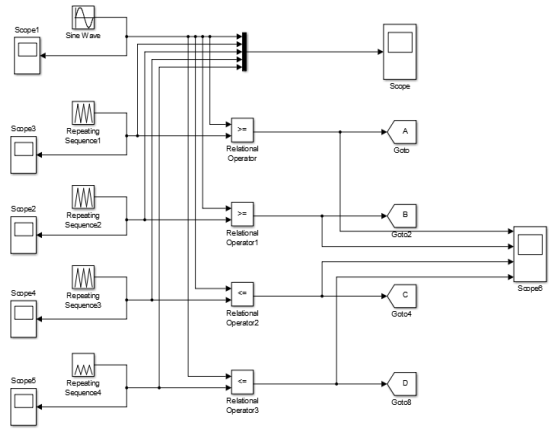

Fig 3. Simulation implementation of firing pulse generation technique using pulse generator

Table I: Switching table for the 5-level Multilevel inverter

V_{op}	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
V_1	1	0	0	1	1	0	0	1
V_2	1	0	0	1	1	0	1	0
V_3	1	0	1	0	1	0	1	0
V_4	1	0	1	0	0	1	1	0
V_5	0	1	1	0	0	1	1	0

Three voltage levels can be obtain using 2 voltage sources and two h bridges. If Vdc is the voltage of first h bride h1 then second h bride h2 is supplied 0.5 of Vdc. appropriate MOSFET are switched on in order to get different voltage level. 0.5 Vdc, Vdc, 1.5 Vdc, 0. Which are repeated continuity and MOSFET sequence is inverted for negative values.

VII. RESULTS AND DISCUSSION

To experimentally validate the proposed cascaded H-bridge multilevel inverter, a prototype single-phase cascaded H-Bridge multilevel converter has been built using MOSFET as switching device. In this paper the hardware is implemented using the AVR microcontroller ATmega16. This gives high performance and low power AVR.it has data retention quality up to 20 years and have advanced RISC Architecture in that 131 powerful instruction,32*8general purpose working registers, fully static operation and non volatile memory also The advantages of RISC processor against CISC processor are RISC instructions are simpler and consequently operate faster A RISC processor takes a single cycle for each instruction , while CISC processor requires multiple clocks per instruction (typically, at least three cycles of the rough put execution time for the simplest

instruction 12 to 24 clock cycles for more complex instructions), which makes decoding a tough task, and the control unit in a CISC is always implemented by a micro-controller which is much slower than the hardware implemented in RISC.

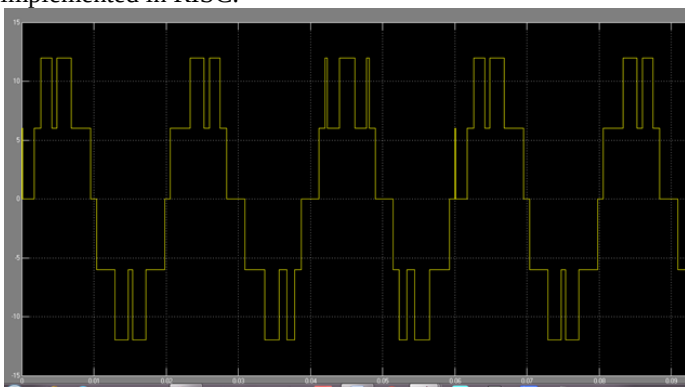

Fig 34Simulation Result of Single phase 5-level Cascade bridge multilevel inverter

Here design of five level cascaded H-bridge and corresponding waveform..

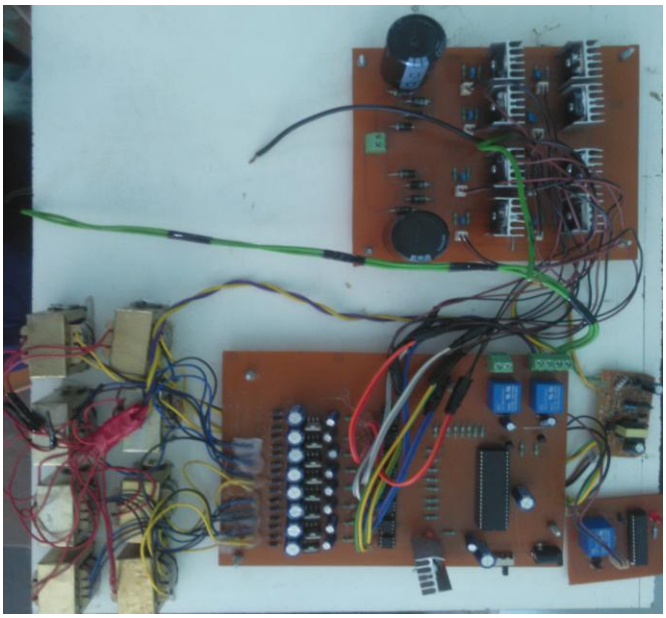

Fig. 5 Experimental setup of five level cascaded H-bridge multilevel inverter

	Simulation Result	**Hardware result**
Resistive load	800Ω	1 Lamp of 60 watt
Vinput	220 V	Rectified 182 V
Voutput	220 V	196 V
Ioutput	0.27 A	0.32 A

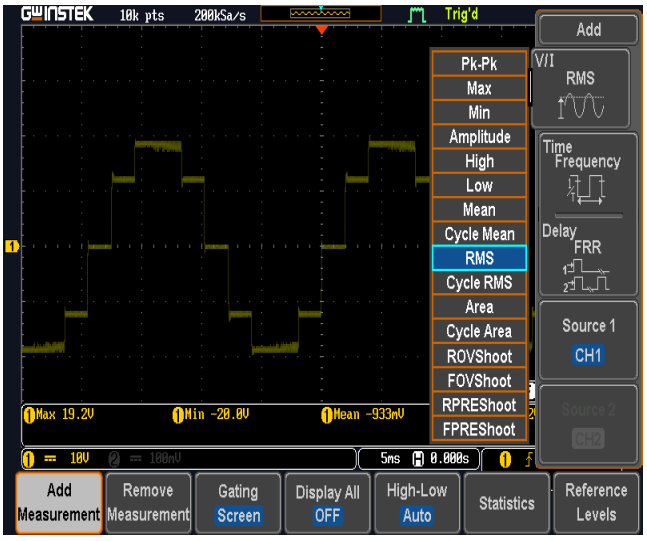

Fig.6 Experimental result of of five level cascaded H-bridge multilevel inverter

VIII. RESULT

Output across Resistive load

For 1 incandescent lamp of 60 watt

Voutput=196 V

Ioutput=0.32 A

For 2 incandescent lamp of 60 watt

Voutput=191 V

Ioutput=0.67A

VIII.CONCLUSION

In this paper, a five level cascaded H-bridge multilevel with multicarrier pulse width modulation and embedded matlab function, is presented. The simulation results show that the total harmonic distortion is low for multicarrier modulation method. The total harmonic distortion can be further reduced by using filter circuit. also hardware implementation done for the comparison of result at different resistive load. It gives a different result of currents and voltages for different resistive loads.

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